Practice Quiz 13

The questions on this quiz pertain to the Simple Computer described in the class notes and featured in Lab 13. Signal names and descriptions are provided in the table below.

1. The following control signal is **not** asserted on a **fetch** cycle:
   (A) MSL
   (B) IRL
   (C) PCC
   (D) POA
   (E) none of the above

2. The following control signal is asserted on every **execute** cycle (except for the **HLT** instruction):
   (A) MSL
   (B) IRL
   (C) PCC
   (D) POA
   (E) none of the above

3. The following ALU control signal is **only** asserted on the execute cycle of a **STA** instruction:
   (A) ALE
   (B) AOE
   (C) ALX
   (D) ALY
   (E) none of the above

Name	Description
START	Asynchronous Machine Reset
MSL	Memory Select
MOE	Memory Output Tri-State Enable
MWE	Memory Write Enable
PCC	Program Counter Count Enable
POA	Program Counter Output on Address Bus Tri-State Enable
PLA	Program Counter Load from Address Bus Enable
POD	Program Counter Output on Data Bus Tri-State Enable
PLD	Program Counter Load from Data Bus Enable
IRL	Instruction Register Load Enable
IRA	Instruction Register Output on Address Bus Tri-State Enable
AOE	A-register Output on Data Bus Tri-State Enable
ALE	ALU Function Enable
ALX	ALU Function Select Line "X"
ALY	ALU Function Select Line "Y"
SPI	Stack Pointer Increment
SPD	Stack Pointer Decrement
SPA	Stack Pointer Output on Address Bus Tri-State Enable
RST	Synchronous State Counter Reset
RUN	Machine Run Enable

4. The expression "**(A) ← (A) + (10110)**" means:
   (A) replace the contents of memory location 10110 with the sum of its current contents plus the contents of the accumulator
   (B) add the constant 10110 to the contents of the accumulator and store the result in memory location 10110
   (C) replace the contents of the accumulator with the sum of its current contents plus the constant 10110
   (D) replace the contents of the accumulator with the sum of its current contents plus the contents of memory location 10110
   (E) none of the above

5. When a set of control signals are said to be **mutually exclusive**, it means that:
   (A) all the control signals may be asserted simultaneously
   (B) each control signal is dependent on the others
   (C) only one control signal may be asserted at a given instant
   (D) any combination of control signals may be asserted at a given instant
   (E) none of the above