Practice Quiz 10

The following Verilog program applies to the questions on this quiz. Complete the PS-NS table and state transition diagram to determine the answers.

```
module myseq(CLK, Q);
  input wire CLK;
  output reg [2:0] Q;

  reg [2:0] next_Q;

   always @ (posedge CLK) begin
    Q <= next_Q;
   end

  always @ (Q) begin
   next_Q[2] =  Q[1];
   next_Q[1] =  Q[0];
   next_Q[0] = ~(Q[1] | Q[0]);
  end
endmodule
```

Q2	Q1	Q0	Q2*	Q1*	Q0*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

1. The number of states in the **periodic sequence** is:
   (A) 1 (B) 3 (C) 6 (D) 8 (E) none of these

2. **Another name** sometime used for the periodic sequence realized here is:
   (A) one hot
   (B) two hot
   (C) switchtail
   (D) twisted ring
   (E) none of the above

3. The **maximum** number of clock cycles needed for **self-correction** is:
   (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

4. The number of **<u>state variables</u>** needed to **uniquely decode** each of the states in the periodic sequence is:
   (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

5. The “mystery sequencer” is a:
   (A) binary UP counter
   (B) Gray code counter
   (C) Johnson counter
   (D) ring counter
   (E) none of the above