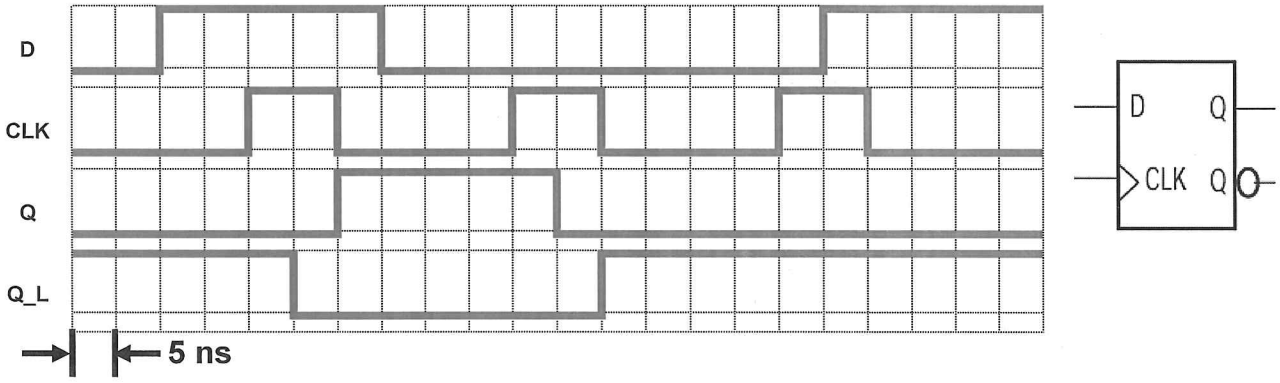
Lab Quiz 9

The following figure applies to questions 1-3:



1. The **nominal setup time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

2. The **nominal hold time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

3. The $t_{PHL(C\rightarrow Q)}$ of the D flip-flop is:

   (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

The following figure applies to questions 4-5:

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assign QM = ~(~(SM&CM) & QM_N);
assign QM_N = ~(~(RM&CM) & QM);
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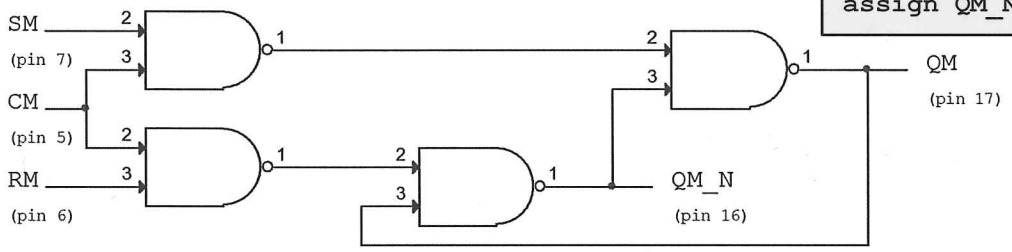

4. The circuit shown above was realized in Lab 8 on a 22V10 using the Verilog assignment statements shown. If the inputs SM, CM, and RM are all set to "1", the outputs QM and QM_N will be:

   (A) QM = 0, QM_N = 0 (B) QM = 0, QM_N = 1 (C) QM = 1, QM_N = 0 (D) QM = 1, QM_N = 1 (E) QM = X, QM_N = X

5. If the inputs SM, CM, and RM are all set to "1" and CM is then changed from "1" to "0", the outputs QM and QM_N will be:

   (A) QM = 0, QM_N = 0 (B) QM = 0, QM_N = 1 (C) QM = 1, QM_N = 0 (D) QM = 1, QM_N = 1 (E) QM = X, QM_N = X

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