

### Lab Quiz 7

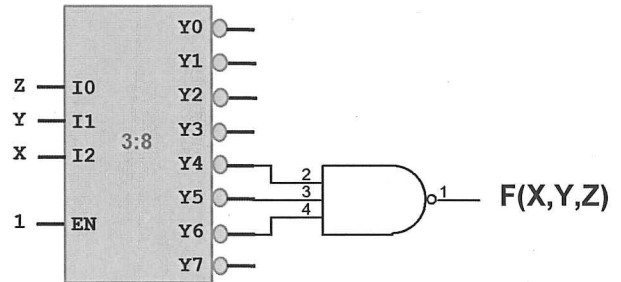
Closed Book and Notes – No Calculators Allowed

1. In Verilog, a wire can not take on the following value:

- (A) 0    (B) 1    (C) X    (D) Z    (E) none of these

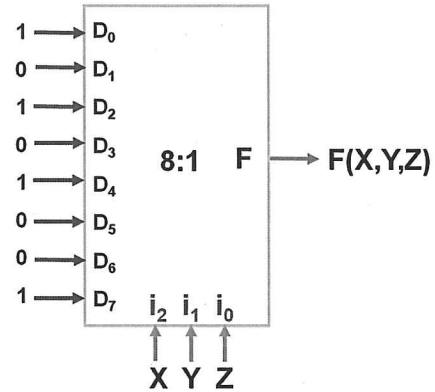
2. The ON set realized by the 3:8 decoder circuit shown is:

- (A)  $\Sigma_{X,Y,Z} (4,5,6)$   
 (B)  $\Sigma_{X,Y,Z} (0,1,2,3,7)$   
 (C)  $\Pi_{X,Y,Z} (4,5,6)$   
 (D)  $\Pi_{X,Y,Z} (0,1,2,3,7)$   
 (E) none of the above



3. The OFF set realized by the 8:1 multiplexer circuit shown is:

- (A)  $\Sigma_{X,Y,Z} (0,2,4,7)$   
 (B)  $\Sigma_{X,Y,Z} (1,3,5,6)$   
 (C)  $\Pi_{X,Y,Z} (0,2,4,7)$   
 (D)  $\Pi_{X,Y,Z} (1,3,5,6)$   
 (E) none of the above



4. For the Verilog program shown, if input I[0] is asserted and all the other inputs are negated, the output produced will be:

- (A) E\_z[1]=0, E\_z[0]=0, G=0  
 (B) E\_z[1]=0, E\_z[0]=0, G=1  
 (C) E\_z[1]=Hi-Z, E\_z[0]=Hi-Z, G=Hi-Z  
 (D) E\_z[1]=Hi-Z, E\_z[0]=Hi-Z, G=1  
 (E) none of the above

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module prienc(I, E_z, G, TEN);
    input wire [3:0] I;
    input wire TEN;
    output tri [1:0] E_z;
    output wire G;
    reg [2:0] EG;
    always @ (I) begin
        casez (I)
            4'b0000: EG = 3'b000;
            4'b0001: EG = 3'b001;
            4'b001?: EG = 3'b011;
            4'b01???: EG = 3'b101;
            4'b1????: EG = 3'b111;
        endcase
    end
    assign G = EG[0];
    assign E_z = TEN ? EG[2:1] : 2'bzz;
endmodule
    
```

5. For the Verilog program shown, if inputs I[1], I[2], and TEN are asserted and all the other inputs are negated, the output produced will be:

- (A) E\_z[1]=0, E\_z[0]=0, G=0  
 (B) E\_z[1]=0, E\_z[0]=1, G=1  
 (C) E\_z[1]=1, E\_z[0]=0, G=1  
 (D) E\_z[1]=Hi-Z, E\_z[0]=Hi-Z, G=1  
 (E) none of the above

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