Lab Quiz 13

The questions on this quiz pertain to the *Personal Simple Computer* featured in Lab 13. Signal names and descriptions are provided in the table below.

Name	*Description*
START	Asynchronous Machine Reset
MWE	Memory Write Enable
PCC	Program Counter Count Enable
POA	Program Counter Output on Address Bus Enable
IRL	Instruction Register Load Enable
IRA	Instruction Register Output on Address Bus Enable
AOE	A-register Output on Data Bus Enable
ALE	ALU Function Enable
ALX	ALU Function Select Line "X"
ALY	ALU Function Select Line "Y"
IPE	Input port read enable
OPE	Output port write enable
RUN	Machine Run Enable

Opcode	*Mnemonic*		*Function Performed*
000	HLT		halt execution
001	LDA	*addr*	(A) ← (*addr*)
010	ADD	*addr*	(A) ← (A) + (*addr*)
011	SUB	*addr*	(A) ← (A) − (*addr*)
100	AND	*addr*	(A) ← (A) ∩ (*addr*)
101	STA	*addr*	(*addr*) ← (A)
110	INA		(A) ← DIP[3:0]
111	OUA		DIS4 ← (A)

1. The following control signal(s) is/are **not asserted** on a **fetch** cycle:
   (A) **IRA**
   (B) **PCC**
   (C) **POA**
   (D) all of the above
   (E) none of the above

2. The following control signal(s) is/are **not asserted** on a **execute** cycle:
   (A) **IRL**
   (B) **PCC**
   (C) **POA**
   (D) all of the above
   (E) none of the above

3. The following ALU control signal **is asserted** on the execute cycle of an **OUA** instruction:
   (A) **ALE**
   (B) **AOE**
   (C) **ALX**
   (D) **ALY**
   (E) none of the above

4. Assuming the **CF** condition code bit is **initially cleared,** a **SUB** followed by an **ADD** (using the same two operands) that could be performed on the **PSC 716** to verify that **CF** was properly **being set and subsequently cleared** is:
   (A) 1111 – 1110 followed by 1111 + 1110
   (B) 0010 – 0011 followed by 0010 + 0011
   (C) 0010 – 0001 followed by 0010 + 0001
   (D) 0001 – 1110 followed by 0001 + 1110
   (E) none of the above

5. Assuming the **VF** condition code bit is **initially cleared,** a **SUB** followed by an **ADD** (using the same two operands) that could be performed on the **PSC 716** to verify that **VF** was properly **being set and subsequently cleared** is:
   (A) 1111 – 1110 followed by 1111 + 1110
   (B) 0111 – 1001 followed by 0111 + 1001
   (C) 0010 – 0011 followed by 0010 + 0011
   (D) 0001 – 1110 followed by 0001 + 1110
   (E) none of the above

Signature: _____ **E-mail:** _ _ _ _ _ _ _ _ _ **@purdue.edu**