

Purdue IM:PACT* Spring 2019 Edition
*Instruction Matters: Purdue Academic Course Transformation

Introduction to Digital System Design

Module 4

Arithmetic and Computer Logic Circuits

Glossary of Common Terms

- **RADIX** – a commonly-used signed number notation (also called 2's complement)
- **OPERAND** – a binary number involved in an arithmetic or logical operation
- **HALF ADDER** – logic circuit that adds two binary bits to produce carry and sum outputs
- **FULL ADDER** – logic circuit that adds three binary bits to produce carry and sum outputs
- **ADDER/SUBTRACTOR** – logic circuit that adds and subtracts pairs of binary operands
- **MAGNITUDE COMPARATOR** – logic circuit that determines which binary operand is greater/less than a second binary operand

Glossary of Common Terms

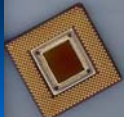
- **CARRY LOOK-AHEAD** – a means of generating the carry functions needed for addition in parallel
- **MULTIPLIER** – logic circuit that multiplies pairs of binary operands
- **COMPUTER** – device that sequentially executes a stored program
- **PROGRAM** – a series of instructions that direct the processing activity of a computer
- **INSTRUCTION** – a unit of processing activity (“line of code”) executed by a computer
- **OPCODE** – the “operation code” field of an instruction

Glossary of Common Terms

- **MEMORY** – array of D latches used to store instructions, operands, and results
- **PROGRAM COUNTER** – register that points to the next instruction to execute
- **INSTRUCTION REGISTER** – register used to “stage” the instruction fetched from memory
- **ALU** – arithmetic logic unit, performs arithmetic and logic operations on binary operands
- **INSTRUCTION DECODER & MICROSEQUENCER** – state machine that orchestrates the activities of a computer's functional blocks

Glossary of Common Terms

- **MICROSEQUENCE** – the “minute” phases of instruction processing by a computer
- **TRANSFER OF CONTROL** – continue execution of program at a location different than the next consecutive instruction
- **I/O** – data input and output operations performed by a computer
- **STACK** – last in, first out data structure used to support expression evaluation and subroutine linkage
- **STACK POINTER** – register used to point to the top stack item (or next available location)



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Introduction to Digital System Design

Module 4-A

Signed Number Notation

Reading Assignment:

DDPP 4th Ed. pp. 34-39, 5th Ed. pp. 44-48

Learning Objectives:

- Compare and contrast three different signed number notations: sign and magnitude, diminished radix, and radix
- Convert a number from one signed notation to another
- Describe how to perform sign extension of a number represented using any of the three notation schemes

Outline

- Overview
- Signed number notation
 - Sign and magnitude
 - Diminished radix
 - Radix
 - Comparison chart
- Simplifications for binary numbers
- Sign extension

Overview

- In order to represent positive and negative numbers as a series of digits without “+” and “-” signs, various *signed number notations* have been devised
- We will discuss the three most commonly used signed number notations:
 - *sign and magnitude* (SM)
 - *diminished radix* (DR)
 - *radix* (R)

Sign and Magnitude

- The original signed number convention employed by “vacuum tube vintage digijocks” was *sign and magnitude* notation
- Here the *left-most digit* (or “sign bit”) indicates whether the number is positive or negative:
 - “0” → positive
 - “R-1” → negative (where R is the *radix* or *base* of the number)

Sign and Magnitude

- Examples:
 - $(+123)_{10} = \text{SM}(0123)_{10}$
 - $(-123)_{10} = \text{SM}(9123)_{10}$
 - $(+144)_5 = \text{SM}(0144)_5$
 - $(-144)_5 = \text{SM}(4144)_5$

SM(0123)₁₀ and SM(9123)₁₀ are referred to as the sign and magnitude complements of one another

Sign and Magnitude

- Negation Method: If N is a number in base R with sign digit n_s , such that
$$(N)_R = n_s n_3 n_2 n_1 n_0$$
then
$$-(N)_R = (R-1-n_s) n_3 n_2 n_1 n_0$$
- Examples:
 - $(+1101)_2 = \text{SM}(01101)_2$
 - $(-1101)_2 = \text{SM}(11101)_2$

Diminished Radix

- The negation (or complement) of a number represented in *diminished radix* (DR) notation can be found by subtracting each digit (including the sign digit) from $(R-1)$, i.e., the "radix minus one" or the "radix diminished by one"
- Examples:
 $(+123)_{10} = DR(0123)_{10}$
 $(-123)_{10} = (9999 - 0123)_{10} = DR(9876)_{10}$

$DR(0123)_{10}$ and $DR(9876)_{10}$ are referred to as the *diminished radix complements* of one another.

Diminished Radix

- Negation Method: If N is a number in base R ,
 $-(N)_R = (R^n - 1)_R - (N)_R$
- Examples:
 $(+1101)_2 = DR(01101)_2$
 $(-1101)_2 = DR(10010)_2$

Note that *positive DR* numbers have the *same* representation as *positive SM* numbers; *negative DR* and *SM* numbers, however, have *different* representations

Radix

- The negation (or complement) of a number represented in *radix* (R) notation can be found by *adding one* to the least significant position of the *diminished radix negation* of that number
- Examples:
 $(+123)_{10} = R(0123)_{10}$
 $(-123)_{10} = (9999 - 0123 + 1)_{10} = R(9877)_{10}$

$R(0123)_{10}$ and $R(9877)_{10}$ are referred to as the *radix complements* of one another

Radix

- Negation Method: If N is a number in base R ,
 $-(N)_R = (R^n)_R - (N)_R$
- Examples:
 $(+1101)_2 = R(01101)_2$
 $(-1101)_2 = R(10011)_2$

Note that *positive R, DR, and SM* numbers all have the *same* representation; *negative R, DR, and SM* numbers, however, all have *different* representations

Comparison of Signed Number Notations

N_{10}	SM	DR	R
+3	011	011	
+2	010	010	
+1	001	001	
+0	000	000	
-0	100	111	
-1	101	110	
-2	110	101	
-3	111	100	
-4	—	—	

Comparison of Signed Number Notations

N_{10}	SM	DR	R
+3	011	011	
+2	010	010	
+1	001	001	
+0	000	000	000
-0	100	111	—
-1	101	110	
-2	110	101	
-3	111	100	
-4	—	—	

Radix has no "negative zero"

Comparison of Signed Number Notations

N_{10}	SM	DR	R
+3	011	011	011
+2	010	010	010
+1	001	001	001
+0	000	000	000
-0	100	111	—
-1	101	110	—
-2	110	101	—
-3	111	100	—
-4	—	—	—

All positive number representations are identical

Radix has no "negative zero"

Comparison of Signed Number Notations

N_{10}	SM	DR	R
+3	011	011	011
+2	010	010	010
+1	001	001	001
+0	000	000	000
-0	100	111	—
-1	101	110	111
-2	110	101	110
-3	111	100	101
-4	—	—	100

All positive number representations are identical

Radix has no "negative zero"

All negative number representations are different

Comparison of Signed Number Notations

N_{10}	SM	DR	R
+3	011	011	011
+2	010	010	010
+1	001	001	001
+0	000	000	000
-0	100	111	—
-1	101	110	111
-2	110	101	110
-3	111	100	101
-4	—	—	100

All positive number representations are identical

Radix has no "negative zero"

All negative number representations are different

Radix has an extra negative number

Simplifications for Binary

- When finding the negations (complements) of binary (base 2) numbers, the methods simplify as follows:
 - SM: complement the sign position
 - DR (also called *1's complement*): complement each position
 - R (also called *2's complement*):
 - add 1 to the DR complement *-or-*
 - scan number from *right to left*; complement each position to the *left* of the first "1" encountered

Practice

- If $(N)_2 = \text{SM}(01100)_2$, find $-(N)_2$ **SM(11100)₂**
- If $(N)_2 = \text{DR}(01100)_2$, find $-(N)_2$ **DR(10011)₂**
- If $(N)_2 = \text{R}(01100)_2$, find $-(N)_2$ **R(10100)₂**

Sign Extension

- Sometimes signed numbers of different length (number of bits) need to be added together – here, the "shorter" number needs to be "padded" with *leading digits* to make it the two numbers the same length
- The rules for padding signed numbers with leading digits are as follows:
 - SM: insert as many zeroes as needed to the *right* of the sign position
 - DR & R: *replicate the sign digit* as many times as needed

Practice

- Extend $SM(09345)_{10}$ to 8 digits **SM(00009345)₁₀**
- Extend $DR(76500)_8$ to 8 digits **DR(77776500)₈**
- Extend $R(01100)_2$ to 8 digits **R(00001100)₂**
- Extend $R(11100)_2$ to 8 digits **R(11111100)₂**

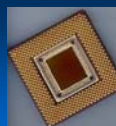
Comparison/Observations

- SM and DR notation have a **balanced set** of positive and negative numbers, and have **two representations** for zero
- R notation has an **unbalanced** set of positive and negative numbers (there is an **“extra negative number”**), and has a **single** representation for zero
- 99% of all computers use **radix** notation; our discussion on addition and subtraction will therefore focus on **radix arithmetic** (we will assume a prefix of “R” on all numbers subsequently used)

Clicker Quiz

1. The five-bit radix number, $R(10101)_2$, converted to sign and magnitude notation, is:
 - A. SM $(10101)_2$
 - B. SM $(01010)_2$
 - C. SM $(11010)_2$
 - D. SM $(11011)_2$
 - E. none of the above

2. The five-bit diminished radix number, $DR(10101)_2$, converted to sign and magnitude notation, is:
 - A. SM $(10101)_2$
 - B. SM $(01010)_2$
 - C. SM $(11010)_2$
 - D. SM $(11011)_2$
 - E. none of the above



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Introduction to Digital System Design

Module 4-B Radix Addition and Subtraction

Reading Assignment:
 DDPP 4th Ed. pp. 39-43, 5th Ed. pp. 48-52

Learning Objectives:

- perform radix addition and subtraction
- describe the various conditions of interest following an arithmetic operation: overflow, carry, negative, zero

Outline

- Radix Addition
- Overflow Detection
- Radix Subtraction

Radix Arithmetic – Addition

- Method:** Add all digits, including the sign digits; *ignore* any carry out of the sign position
- Problem:** Since we are working with numbers of fixed length, the result of an addition can yield a number which is *too large* to represent in the same number of digits – this error condition is called *overflow*
- Important:** When overflow occurs, there is *no valid numeric result*

Overflow Detection

- Summarization:** Overflow occurs if two positive numbers are added and a negative result is obtained, or if two negative numbers are added and a positive result is obtained (or, if numbers of *like sign* are added and a result with the *opposite sign* is obtained)
- Overflow *cannot* occur when adding numbers of the *opposite sign*
- Another way to detect overflow:** If the *carry in* to the sign position is *different* than the *carry out* of the sign position, then overflow has occurred

Radix Arithmetic – Addition

Examples: (all numbers are binary)

$\begin{array}{r} +6 \\ +10 \\ \hline 00110 \\ +01010 \\ \hline 10000 \end{array}$	$\begin{array}{r} 00010 \\ +01010 \\ \hline \end{array}$
--	--

Here, added two positive numbers, but got a negative result → OVERFLOW

Radix Arithmetic – Addition

Examples: (all numbers are binary)

$\begin{array}{r} +6 \\ +10 \\ \hline 00110 \\ +01010 \\ \hline 10000 \end{array}$	$\begin{array}{r} 00010 \\ +01010 \\ \hline 01100 \end{array}$
--	--

Here, added two positive numbers, but got a negative result → OVERFLOW

Here, added two positive numbers, and got a positive result (+12) → OK!

Radix Arithmetic – Addition

- Examples: (all numbers are binary)

$\begin{array}{r} -4 \rightarrow 11100 \\ -10 \rightarrow +10110 \\ \hline \text{ignore} \uparrow 110010 \end{array}$	$\begin{array}{r} 10011 \\ +10001 \\ \hline \end{array}$
---	--

Here, added two *negative* numbers, and got a *negative* result (-14) → OK!

Radix Arithmetic – Addition

- Examples: (all numbers are binary)

$\begin{array}{r} -4 \rightarrow 11100 \\ -10 \rightarrow +10110 \\ \hline \text{ignore} \uparrow 110010 \end{array}$	$\begin{array}{r} 10011 \rightarrow -13 \\ +10001 \rightarrow -15 \\ \hline 00100 \end{array}$
---	--

Here, added two *negative* numbers, and got a *negative* result (-14) → OK!

Here, added two *negative* numbers, but got a *positive* result → OVERFLOW

Radix Arithmetic – Addition

- Examples: (all numbers are binary)

$\begin{array}{r} -13 \rightarrow 10011 \\ +15 \rightarrow +01111 \\ \hline \text{ignore} \uparrow 100010 \end{array}$	$\begin{array}{r} 01111 \\ +10000 \\ \hline \end{array}$
--	--

Here, added numbers of *opposite sign* → overflow *cannot* occur (result is +2)

Radix Arithmetic – Addition

- Examples: (all numbers are binary)

$\begin{array}{r} -13 \rightarrow 10011 \\ +15 \rightarrow +01111 \\ \hline \text{ignore} \uparrow 100010 \end{array}$	$\begin{array}{r} 01111 \rightarrow +15 \\ +10000 \rightarrow -16 \\ \hline 11111 \end{array}$
--	--

Here, added numbers of *opposite sign* → overflow *cannot* occur (result is +2)

Again, added numbers of *opposite sign* → overflow *cannot* occur (result is -1)

Radix Arithmetic – Subtraction

- Method: Take the radix complement of the subtrahend and ADD; the same rules for overflow apply
- Examples:

$\begin{array}{r} 01011 \\ -01100 \\ \hline \end{array}$
--

Why does this work?
 Examples: $5 - (+3) = 5 + (-3) = 2$
 $9 - (-13) = 9 + (+13) = 22$

Radix Arithmetic – Subtraction

- Method: Take the radix complement of the subtrahend and ADD; the same rules for overflow apply
- Examples:

$\begin{array}{r} +11 \rightarrow 01011 \\ +12 \rightarrow -01100 \\ \hline \end{array}$	$\begin{array}{r} 01011 \text{ (minuend)} \\ 10011 \\ + 1 \text{ (Radix complement of subtrahend)} \\ \hline 11111 \end{array}$
--	---

Here, added numbers of *opposite sign* → overflow *cannot* occur (result is -1)

Radix Arithmetic – Subtraction

• Examples:

+11	01011		01011
-16	-10000		01111
			+ 1
			<u>11011</u>

Overflow

Radix Arithmetic – Subtraction

• Examples:

+11	01011		01011
-16	-10000		01111
			+ 1
			<u>11011</u>

Overflow

-15	10001		10001
+2	-00010		11101
			+ 1
			<u>10111</u>

ignore → 1 01111 Overflow

Radix Arithmetic – Subtraction

• Examples:

+11	01011		01011
0	-00000		11111
			+ 1
			<u>101011</u>

ignore → +11

Radix Arithmetic – Subtraction

• Examples:

+11	01011		01011
0	-00000		11111
			+ 1
			<u>01011</u>

ignore → +11

-15	10001		10001
-1	-11111		00000
			+ 1
			<u>10010</u>

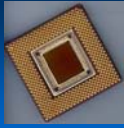
-14

Clicker
Quiz

- When adding the five-bit signed numbers $(10111)_2 + (11001)_2$ using radix arithmetic, the result obtained is:
 - A. $(10000)_2$
 - B. $(110000)_2$
 - C. $(11000)_2$
 - D. overflow (invalid result)
 - E. none of the above

2. When subtracting the five-bit signed numbers $(10111)_2 - (11001)_2$ using radix arithmetic, the result obtained is:

- A. $(10000)_2$
- B. $(11000)_2$
- C. $(11110)_2$
- D. overflow (*invalid result*)
- E. none of the above



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Introduction to Digital System Design

Module 4-C Adder, Subtractor, and Comparator Circuits

Reading Assignment:
 DDPP 4th Ed. pp. 458-466, 469-478; 5th Ed. pp. 331-339, 341-345, 372-375

Learning Objectives:

- Describe the operation of a half-adder and write equations for its sum (S) and carry (C) outputs
- Describe the operation of a full adder and write equations for its sum (S) and carry (C) outputs
- Design a “population counting” or “vote counting” circuit using an array of half-adders and/or full-adders
- Design an N-digit radix adder/subtractor circuit with condition codes
- Design a (signed or unsigned) magnitude comparator circuit that determines if $A=B$, $A<B$, or $A>B$

Outline

- Overview
- Half Adders
- Full Adders
- Radix Adder/Subtractors
- Comparators

Overview

- Addition is the most commonly performed arithmetic operation in digital systems
- An **adder** combines two arithmetic operands using the addition rules described previously
- The same addition rules (and circuits) are used for both **signed** (two’s complement) and **unsigned** numbers
- Subtraction can be performed by taking the **complement** of the subtrahend and adding it to the minuend

Half Adders

- A half adder is used to add two binary digits, X_i and Y_i , to form a sum digit, S_i , and a carry digit, C_i

X_i	Y_i	C_i	S_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S_i = X_i \oplus Y_i$$

$$C_i = X_i \cdot Y_i$$

Full Adders

- A full adder is used to add three binary digits, X_i , Y_i , C_{i-1} (where C_{i-1} is usually the carry **in** from a previous stage), to form a sum digit, S_i , and a carry **out** digit, C_i

Full Adders

X_i	Y_i	C_{i-1}	C_i	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$S_i = X_i \oplus Y_i \oplus C_{i-1}$$

$$C_i = X_i \cdot Y_i + X_i \cdot C_{i-1} + Y_i \cdot C_{i-1}$$

Example – Vote Counting Circuit

- Using only half adders and full adders, design a circuit that finds the (unsigned) sum of five binary digits

Also called a "population" counter

Clicker Quiz

The **Digi-Vota-Matic** is a three-judge score tabulation system that allows each judge to enter a score ranging from "0" (00_2) to "3" (11_2) on a pair of DIP switches, and displays the sum of the three scores (ranging from "0" to "9") on a 7-segment LED.

- Implemented using a CASE statement in Verilog, a circuit that finds the sum of three 2-bit unsigned numbers would require ___ assignments.
 - A. 16
 - B. 32
 - C. 64
 - D. 128
 - E. none of the above

2. Implemented using a 22V10 PLD, a circuit that finds the sum of three 2-bit unsigned numbers would require no more than ___ macrocells.
- A. 2
 - B. 4
 - C. 8
 - D. 16
 - E. none of the above

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Multi-Digit Adder/Subtractor Circuits

- Two binary words, each with n bits, can be added using a *ripple* adder – a cascade of n full-adder stages, each of which handles one bit (also called an *iterative* circuit)
- The word *ripple* describes the flow of the carries from one full adder cell to the next
- Subtraction is performed by taking the *diminished radix* complement of the subtrahend (using XOR gates) and setting the *least significant bit carry-in* (LSB C_{in}) to “1” (effectively forming the *radix* complement of the subtrahend)

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Review of Radix Addition

- Method: Add all digits, including the sign digits; ignore any carry out of the sign position
- Problem: Since we are working with numbers of fixed length, the result of an addition can yield a number which is *too large* to represent in the same number of digits – this error condition is called *overflow*
- Important: When overflow occurs, there is *no valid numeric result*

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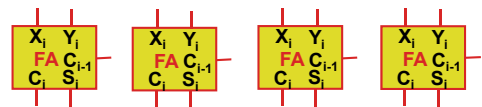
Overflow Detection

- Summarization: Overflow occurs if two positive numbers are added and a negative result is obtained, or if two negative numbers are added and a positive result is obtained (or, if numbers of *like sign* are added and a result with the *opposite sign* is obtained)
- Overflow *cannot* occur when adding numbers of the *opposite sign*
- Another way to detect overflow: If the *carry in* to the sign position is *different* than the *carry out* of the sign position, then overflow has occurred

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Example – 4-bit Ripple Adder/Subtractor

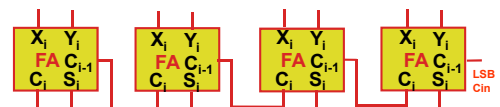
$$\begin{array}{r} A_3 A_2 A_1 A_0 \\ \pm B_3 B_2 B_1 B_0 \\ \hline S_3 S_2 S_1 S_0 \end{array}$$



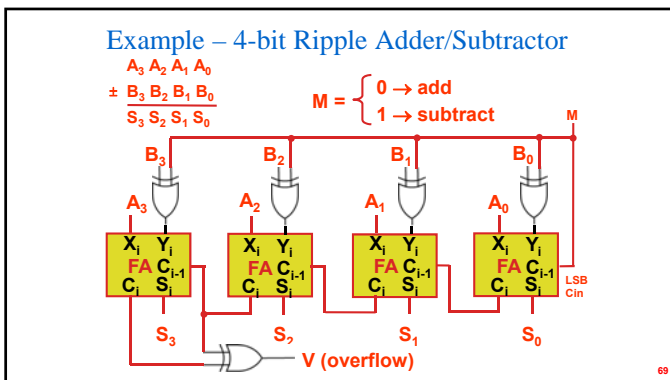
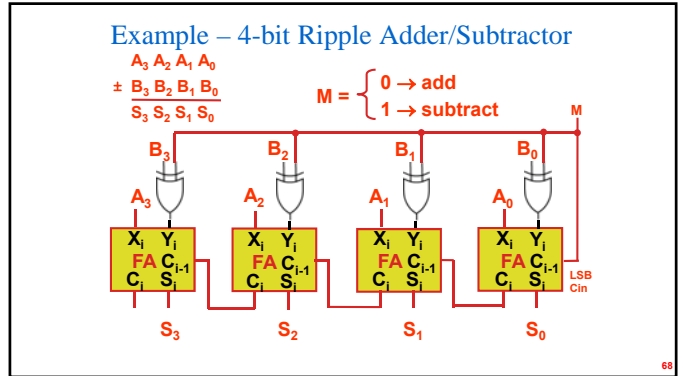
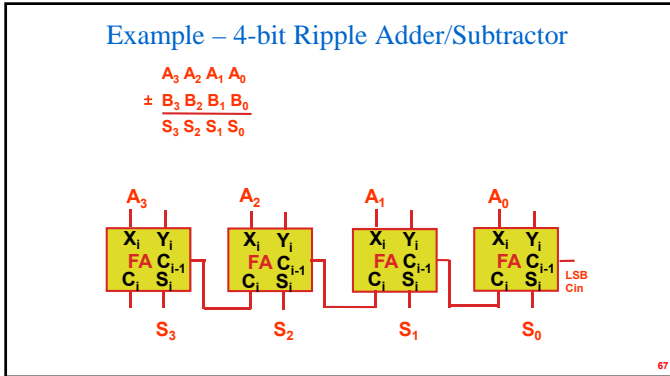
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Example – 4-bit Ripple Adder/Subtractor

$$\begin{array}{r} A_3 A_2 A_1 A_0 \\ \pm B_3 B_2 B_1 B_0 \\ \hline S_3 S_2 S_1 S_0 \end{array}$$



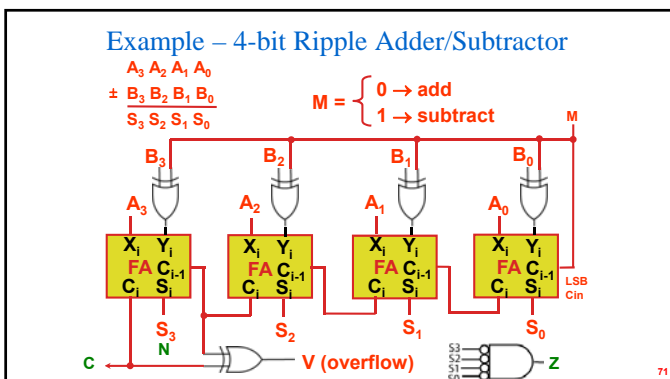
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Other Conditions of Interest

- In addition to overflow, other conditions of interest following an arithmetic operation include the following:
 - ZERO – the result of the computation was **00...0**
 - NEGATIVE – the result of the computation was a **negative number**
 - CARRY – the computation produced a **carry out** of the sign position
- These conditions are sometimes referred to as **“condition codes”** or **“flags”**

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Looking Ahead...

- The “C” (carry) flag serves multiple purposes
 - Extended precision add/subtract (“extended” = integer multiples of 32 bits, if using a 32-bit processor)
 - Add – “C” bit (*being set*) represents the **presence** of a **carry propagated forward** (from least significant word to most significant word of extended number)
 - Subtract – “C” bit (*being set*) represents the **absence** of a **borrow propagated forward** (i.e., the **complement** of a borrow propagated forward, which means that **C=1** indicates that **no borrow** is propagated forward)
 - So...*regardless of whether an add or subtract is performed*, the “C” bit is simply set to the carry out of the sign position
 - Conditional execution (change of flow)
 - Flags set based on **abstract** of operands being compared (e.g. `cmp` instruction)

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Looking Ahead...

- ARM extended precision 64-bit addition using (iterative) ADCS

```

LDR r0, =0xFFFFFFFF ; X_Low ( X = 0x3333FFFFFFFF )
LDR r1, =0x3333FFFF ; X_High
LDR r2, =0x00000001 ; Y_Low ( Y = 0x3333000000000001 )
LDR r3, =0x33330000 ; Y_High
ADDS r0, r0, r2 ; lower 32-bit
ADCS r1, r1, r3 ; upper 32-bit
    
```

$(R1) \leftarrow (R1) + (R3) + (CF)'$

Looking Ahead...

- ARM extended precision 64-bit subtraction using (iterative) SBCS

```

LDR r0, =0x00000001 ; X_Low( X = 0x0000000100000001 )
LDR r1, =0x00000001 ; X_High
LDR r2, =0x00000003 ; Y_Low( Y = 0x0000000000000003 )
LDR r3, =0x00000000 ; Y_High
SUBS r0, r0, r2 ; lower 32-bit
SBCS r1, r1, r3 ; upper 32-bit
    
```

$(R1) \leftarrow (R1) - (R3) - (CF)'$

$(CF)'$ is the borrow propagated forward

which is equivalent to...

$(R1) \leftarrow (R1) - (R3) + (CF)$

Clicker Quiz

- When performing radix addition, the XOR of the carry in to the sign position with the carry out of the sign position provides a means to:
 - generate a carry that is propagated forward
 - generate a borrow that is propagated forward
 - check for a negative result
 - check for an invalid result
 - none of the above

- Following a subtract operation, the carry flag (C) can be used to:
 - generate the *complement of a borrow* that is propagated forward
 - generate a *borrow* that is propagated forward
 - check for a negative result
 - check for an invalid result
 - none of the above

- Following an add operation, the negative flag (N) can be used to:
 - generate a carry that is propagated forward
 - generate a borrow that is propagated forward
 - check for a negative result
 - check for an invalid result
 - none of the above

Comparators

- Comparing two binary words for equality is a commonly used operation in computer systems – a circuit that does this is called a **comparator**
- XOR and XNOR gates may be viewed as **one-bit comparators** (from which larger comparators can be built)
- Circuits that determine an arithmetic relationship between two operands (greater or less than) are called **magnitude comparators**

Example – 4-bit Magnitude Comparator

- Design a 4-bit (**signed**) magnitude comparator that determines if **A=B**, **A<B**, or **A>B**
- Solution:** Calculate **(A-B)** and examine the condition codes produced for each case
 - ZERO (“Z” for zero flag)
 - NEGATIVE (“N” for negative flag)
 - CARRY (“C” for carry/borrow flag)
 - OVERFLOW (“V” for overflow flag)

Need to know how the condition codes are affected for all possible results generated

Example – 4-bit Magnitude Comparator

Step 1: Determine condition codes produced for all possible (2-bit) cases of A-B

A ₁	A ₀	(A)	B ₁	B ₀	(B)	?	C	Z	N	V
0	0	0	0	0	0					
0	0	0	0	1	+1					
0	0	0	1	0	-2					
0	0	0	1	1	-1					
0	1	+1	0	0	0					
0	1	+1	0	1	+1					
0	1	+1	1	0	-2					
0	1	+1	1	1	-1					
1	0	-2	0	0	0					
1	0	-2	0	1	+1					
1	0	-2	1	0	-2					
1	0	-2	1	1	-1					
1	1	-1	0	0	0					
1	1	-1	0	1	+1					
1	1	-1	1	0	-2					
1	1	-1	1	1	-1					

Example – 4-bit Magnitude Comparator

Step 1: Determine condition codes produced for all possible (2-bit) cases of A-B

A ₁	A ₀	(A)	B ₁	B ₀	(B)	?	C	Z	N	V	
0	0	0	0	0	0			1	1	0	0
0	0	0	0	1	+1			0	0	1	0
0	0	0	1	0	-2			0	0	1	1
0	0	0	1	1	-1			0	0	0	0
0	1	+1	0	0	0			1	0	0	0
0	1	+1	0	1	+1			1	1	0	0
0	1	+1	1	0	-2			0	0	1	1
0	1	+1	1	1	-1			0	0	1	1
1	0	-2	0	0	0			1	0	1	0
1	0	-2	0	1	+1			1	0	0	1
1	0	-2	1	0	-2			1	1	0	0
1	0	-2	1	1	-1			0	0	1	0
1	1	-1	0	0	0			1	0	1	0
1	1	-1	0	1	+1			1	0	1	0
1	1	-1	1	0	-2			1	0	0	0
1	1	-1	1	1	-1			1	1	0	0

Example – 4-bit Magnitude Comparator

Step 1: Determine condition codes produced for all possible (2-bit) cases of A-B

A ₁	A ₀	(A)	B ₁	B ₀	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A) = (B)	1	1	0	0
0	0	0	0	1	+1	(A) < (B)	0	0	1	0
0	0	0	1	0	-2	(A) > (B)	0	0	1	1
0	0	0	1	1	-1	(A) > (B)	0	0	0	0
0	1	+1	0	0	0	(A) > (B)	1	0	0	0
0	1	+1	0	1	+1	(A) = (B)	1	1	0	0
0	1	+1	1	0	-2	(A) > (B)	0	0	1	1
0	1	+1	1	1	-1	(A) > (B)	0	0	1	1
1	0	-2	0	0	0	(A) < (B)	1	0	1	0
1	0	-2	0	1	+1	(A) < (B)	1	0	0	1
1	0	-2	1	0	-2	(A) = (B)	1	1	0	0
1	0	-2	1	1	-1	(A) < (B)	0	0	1	0
1	1	-1	0	0	0	(A) < (B)	1	0	1	0
1	1	-1	0	1	+1	(A) < (B)	1	0	1	0
1	1	-1	1	0	-2	(A) > (B)	1	0	0	0
1	1	-1	1	1	-1	(A) = (B)	1	1	0	0

Example – 4-bit Magnitude Comparator

Step 2: Make note of the condition code combinations corresponding to the functions A=B, A<B, and A>B

A ₁	A ₀	(A)	B ₁	B ₀	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A) = (B)	1	1	0	0
0	0	0	0	1	+1	(A) < (B)	0	0	1	0
0	0	0	1	0	-2	(A) > (B)	0	0	1	1
0	0	0	1	1	-1	(A) > (B)	0	0	0	0
0	1	+1	0	0	0	(A) > (B)	1	0	0	0
0	1	+1	0	1	+1	(A) = (B)	1	1	0	0
0	1	+1	1	0	-2	(A) > (B)	0	0	1	1
0	1	+1	1	1	-1	(A) > (B)	0	0	1	1
1	0	-2	0	0	0	(A) < (B)	1	0	1	0
1	0	-2	0	1	+1	(A) < (B)	1	0	0	1
1	0	-2	1	0	-2	(A) = (B)	1	1	0	0
1	0	-2	1	1	-1	(A) < (B)	0	0	1	0
1	1	-1	0	0	0	(A) < (B)	1	0	1	0
1	1	-1	0	1	+1	(A) < (B)	1	0	1	0
1	1	-1	1	0	-2	(A) > (B)	1	0	0	0
1	1	-1	1	1	-1	(A) = (B)	1	1	0	0

Example – 4-bit Magnitude Comparator

Step 2: Make note of the condition code combinations corresponding to the functions $A=B$, $A<B$, and $A>B$

A_3	A_2	(A)	B_3	B_2	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A)=(B)	1	1	0	0
0	0	0	0	1	+1	(A)<(B)	0	0	1	0
0	0	0	1	0	-2	(A)>(B)	0	0	1	1
0	0	0	1	1	-1	(A)>(B)	0	0	0	0
0	1	+1	0	0	0	(A)>(B)	1	0	0	0
0	1	+1	0	1	+1	(A)=(B)	1	1	0	0
0	1	+1	1	0	-2	(A)>(B)	0	0	1	1
0	1	+1	1	1	-1	(A)>(B)	0	0	1	1
1	0	-2	0	0	0	(A)<(B)	1	0	1	0
1	0	-2	0	1	+1	(A)<(B)	1	0	0	1
1	0	-2	1	0	-2	(A)=(B)	1	1	0	0
1	0	-2	1	1	-1	(A)<(B)	0	0	1	0
1	1	-1	0	0	0	(A)<(B)	1	0	1	0
1	1	-1	0	1	+1	(A)<(B)	1	0	1	0
1	1	-1	1	0	-2	(A)>(B)	1	0	0	0
1	1	-1	1	1	-1	(A)=(B)	1	1	0	0

Example – 4-bit Magnitude Comparator

Step 2: Make note of the condition code combinations corresponding to the functions $A=B$, $A<B$, and $A>B$

A_3	A_2	(A)	B_3	B_2	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A)=(B)	1	1	0	0
0	0	0	0	1	+1	(A)<(B)	0	0	1	0
0	0	0	1	0	-2	(A)>(B)	0	0	1	1
0	0	0	1	1	-1	(A)>(B)	0	0	0	0
0	1	+1	0	0	0	(A)>(B)	1	0	0	0
0	1	+1	0	1	+1	(A)=(B)	1	1	0	0
0	1	+1	1	0	-2	(A)>(B)	0	0	1	1
0	1	+1	1	1	-1	(A)>(B)	0	0	1	1
1	0	-2	0	0	0	(A)<(B)	1	0	1	0
1	0	-2	0	1	+1	(A)<(B)	1	0	0	1
1	0	-2	1	0	-2	(A)=(B)	1	1	0	0
1	0	-2	1	1	-1	(A)<(B)	0	0	1	0
1	1	-1	0	0	0	(A)<(B)	1	0	1	0
1	1	-1	0	1	+1	(A)<(B)	1	0	1	0
1	1	-1	1	0	-2	(A)>(B)	1	0	0	0
1	1	-1	1	1	-1	(A)=(B)	1	1	0	0

Example – 4-bit Magnitude Comparator

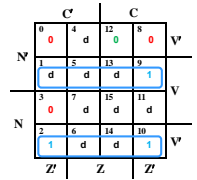
Step 3: Observe that $F_{A=B} = Z$

A_3	A_2	(A)	B_3	B_2	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A)=(B)	1	1	0	0
0	0	0	0	1	+1	(A)<(B)	0	0	1	0
0	0	0	1	0	-2	(A)>(B)	0	0	1	1
0	0	0	1	1	-1	(A)>(B)	0	0	0	0
0	1	+1	0	0	0	(A)>(B)	1	0	0	0
0	1	+1	0	1	+1	(A)=(B)	1	1	0	0
0	1	+1	1	0	-2	(A)>(B)	0	0	1	1
0	1	+1	1	1	-1	(A)>(B)	0	0	1	1
1	0	-2	0	0	0	(A)<(B)	1	0	1	0
1	0	-2	0	1	+1	(A)<(B)	1	0	0	1
1	0	-2	1	0	-2	(A)=(B)	1	1	0	0
1	0	-2	1	1	-1	(A)<(B)	0	0	1	0
1	1	-1	0	0	0	(A)<(B)	1	0	1	0
1	1	-1	0	1	+1	(A)<(B)	1	0	1	0
1	1	-1	1	0	-2	(A)>(B)	1	0	0	0
1	1	-1	1	1	-1	(A)=(B)	1	1	0	0

Example – 4-bit Magnitude Comparator

Step 4: Map and minimize the function for $F_{A<B}$

A_3	A_2	(A)	B_3	B_2	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A)=(B)	1	1	0	0
0	0	0	0	1	+1	(A)<(B)	0	0	1	0
0	0	0	1	0	-2	(A)>(B)	0	0	1	1
0	0	0	1	1	-1	(A)>(B)	0	0	0	0
0	1	+1	0	0	0	(A)>(B)	1	0	0	0
0	1	+1	0	1	+1	(A)=(B)	1	1	0	0
0	1	+1	1	0	-2	(A)>(B)	0	0	1	1
0	1	+1	1	1	-1	(A)>(B)	0	0	1	1
1	0	-2	0	0	0	(A)<(B)	1	0	1	0
1	0	-2	0	1	+1	(A)<(B)	1	0	0	1
1	0	-2	1	0	-2	(A)=(B)	1	1	0	0
1	0	-2	1	1	-1	(A)<(B)	0	0	1	0
1	1	-1	0	0	0	(A)<(B)	1	0	1	0
1	1	-1	0	1	+1	(A)<(B)	1	0	1	0
1	1	-1	1	0	-2	(A)>(B)	1	0	0	0
1	1	-1	1	1	-1	(A)=(B)	1	1	0	0

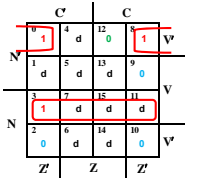


$F_{A<B} = N \oplus V$

Example – 4-bit Magnitude Comparator

Step 5: Map and minimize the function for $F_{A>B}$

A_3	A_2	(A)	B_3	B_2	(B)	?	C	Z	N	V
0	0	0	0	0	0	(A)=(B)	1	1	0	0
0	0	0	0	1	+1	(A)<(B)	0	0	1	0
0	0	0	1	0	-2	(A)>(B)	0	0	1	1
0	0	0	1	1	-1	(A)>(B)	0	0	0	0
0	1	+1	0	0	0	(A)>(B)	1	0	0	0
0	1	+1	0	1	+1	(A)=(B)	1	1	0	0
0	1	+1	1	0	-2	(A)>(B)	0	0	1	1
0	1	+1	1	1	-1	(A)>(B)	0	0	1	1
1	0	-2	0	0	0	(A)<(B)	1	0	1	0
1	0	-2	0	1	+1	(A)<(B)	1	0	0	1
1	0	-2	1	0	-2	(A)=(B)	1	1	0	0
1	0	-2	1	1	-1	(A)<(B)	0	0	1	0
1	1	-1	0	0	0	(A)<(B)	1	0	1	0
1	1	-1	0	1	+1	(A)<(B)	1	0	1	0
1	1	-1	1	0	-2	(A)>(B)	1	0	0	0
1	1	-1	1	1	-1	(A)=(B)	1	1	0	0



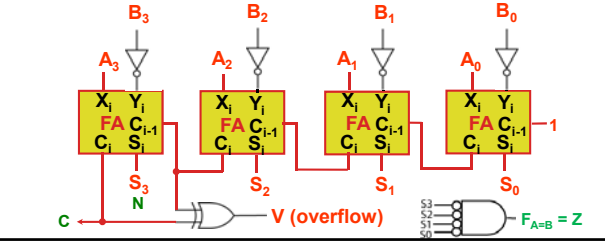
$F_{A>B} = V \cdot N + V' \cdot N' \cdot Z'$

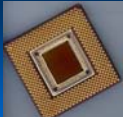
Example – 4-bit Ripple Adder/Subtractor

$A_3 A_2 A_1 A_0$
 $- B_3 B_2 B_1 B_0$
 $S_3 S_2 S_1 S_0$

C
 N
 V
 Z

$F_{A<B} = N \oplus V$
 $F_{A>B} = V \cdot N + V' \cdot N' \cdot Z'$





Purdue IM: PACT* Spring 2019 Edition
 *Instruction Matters: Purdue Academic Course Transformation

Introduction to Digital System Design

Module 4-D Carry Look-Ahead Adder Circuits

Reading Assignment:

DDPP 4th Ed. pp. 478-482, 484-487, 490-491; 5th Ed. pp. 376-383, 384-386

Instructional Objectives:

- Describe the operation of a carry look-ahead (CLA) adder circuit, and compare its performance to that of a ripple adder circuit
- Define the CLA propagate (P) and generate (G) functions, and show how they can be realized using a half-adder
- Write the equation for the carry out function of an arbitrary CLA bit position
- Draw a diagram depicting the overall organization of a CLA
- Determine the worst case propagation delay incurred by a practical (PLD-based) realization of a CLA
- Describe how a "group ripple" adder can be constructed using N-bit CLA blocks

Outline

- Overview
- CLA derivation
- CLA organization
- Sample CLA realization in Verilog
- Observations

Overview

- Previously we looked at one method of constructing an n-digit binary adder from n full adders: connecting the **carry out** from one stage to the **carry in** of the next in a **ripple** fashion
- For large values of n, the propagation delay of a ripple adder can be excessive
- A significant speed-up could be obtained by calculating the carries **in parallel**, rather than **iteratively** – a design that accomplishes this goal is the **carry look-ahead** (CLA) adder circuit (**look-ahead** → **anticipated**)

CLA Derivation

Consider the 4-bit binary adder:

Stage:	3	2	1	0
Augend:	x ₃	x ₂	x ₁	x ₀
Addend:	y ₃	y ₂	y ₁	y ₀
Sum:	s ₃	s ₂	s ₁	s ₀

CLA Derivation

- Definition:** The **generate function** $G_i = 1$ if there is a **carry out** of stage i regardless of whether or not there is a **carry in** to stage i (i.e., both X_i and Y_i are 1)

$$G_i = X_i \cdot Y_i$$
- Definition:** The **propagate function** $P_i = 1$ if a carry in to stage i will cause a carry out of stage i (i.e., **either** $X_i = 0$ and $Y_i = 1$ **or** $X_i = 1$ and $Y_i = 0$)

$$P_i = X_i \oplus Y_i$$

NOTE: Another valid definition of P_i is $X_i + Y_i$ – the "XOR" definition leads to some CLA circuit simplifications, however

CLA Derivation

- Illustration of propagate and generate

Generate from stage 1

Propagated by stage 2

CLA Derivation

- Note that the P_i and G_i functions can be generated using a *half adder*

X_i	Y_i	C_i	S_i
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$P_i = S_i = X_i \oplus Y_i$
 $G_i = C_i = X_i \cdot Y_i$

CLA Derivation

- Next we would like to write our basic full adder equations in terms of propagate and generate functions
- To do this, we will need to reexamine the K-maps for the sum and carry equations of the full adder

Full Adder – Review

X_i	Y_i	C_{i-1}	C_i	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Full Adder – Review

- Map of sum function:

	X'		X	
C_{i-1}'	0	1	0	1
C_{i-1}	1	0	1	0
	Y'	Y	Y'	Y

$S_i = X_i \oplus Y_i \oplus C_{i-1} = P_i \oplus C_{i-1}$

Full Adder – Review

- Map of carry function:

	X'		X	
C_{i-1}'	0	0	1	0
C_{i-1}	1	0	1	1
	Y'	Y	Y'	Y

$C_i = X_i \cdot Y_i + C_{i-1} \cdot (X_i \oplus Y_i) = G_i + C_{i-1} \cdot P_i$

CLA Derivation

- Rewriting the equations for our 4-bit binary adder, we obtain the following:

$$\begin{aligned} C_{-1} &= C_{in} \\ C_0 &= G_0 + C_{in} \cdot P_0 \\ C_1 &= G_1 + C_0 \cdot P_1 \\ C_2 &= G_2 + C_1 \cdot P_2 \\ C_3 &= C_{out} = G_3 + C_2 \cdot P_3 \end{aligned}$$

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CLA Derivation

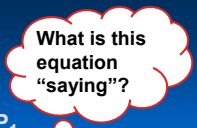
- We would like to write these equations in terms of **available inputs** (P 's, G 's, and C_{in}) rather than the **intermediate carries** (C_0, C_1 , etc.) – the key to doing this is **successive expansion** of the previous equations in terms of the equation for C_0 :

$$\begin{aligned} C_1 &= G_1 + C_0 \cdot P_1 \\ &= G_1 + (G_0 + C_{in} \cdot P_0) \cdot P_1 \end{aligned}$$

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CLA Derivation

$$\begin{aligned} C_1 &= G_1 + C_0 \cdot P_1 \\ &= G_1 + (G_0 + C_{in} \cdot P_0) \cdot P_1 \\ &= G_1 + G_0 \cdot P_1 + C_{in} \cdot P_0 \cdot P_1 \end{aligned}$$



- Each term represents one possibility for obtaining a carry out of stage 1:
 - there is a **generate** in stage 1 ($G_1 = 1$)
 - there is a **generate** in stage 0 ($G_0 = 1$) which is **propagated** by stage 1 ($P_1 = 1$)
 - there is a **carry in** ($C_{in} = 1$) which is **propagated** by stages 0 ($P_0 = 1$) and 1 ($P_1 = 1$)

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CLA Derivation – Exercise

- Write the remaining 4-bit CLA adder carry equations:

$$C_2 =$$

$$C_3 =$$

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CLA Derivation – Exercise

- Write the remaining 4-bit CLA adder carry equations:

$$C_2 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_{in} \cdot P_0 \cdot P_1 \cdot P_2$$

$$C_3 =$$

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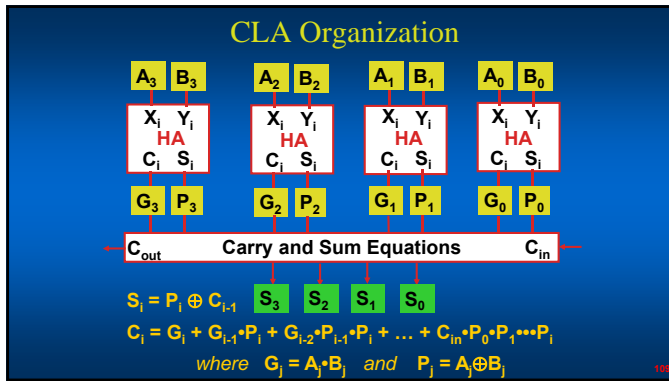
CLA Derivation – Exercise

- Write the remaining 4-bit CLA adder carry equations:

$$C_2 = G_2 + G_1 \cdot P_2 + G_0 \cdot P_1 \cdot P_2 + C_{in} \cdot P_0 \cdot P_1 \cdot P_2$$

$$\begin{aligned} C_3 &= G_3 + G_2 \cdot P_3 + G_1 \cdot P_2 \cdot P_3 + G_0 \cdot P_1 \cdot P_2 \cdot P_3 \\ &\quad + C_{in} \cdot P_0 \cdot P_1 \cdot P_2 \cdot P_3 \end{aligned}$$

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Example – Sample 4-bit CLA Realization (the “hard” way...)

```

/* 4-bit Carry Look-Ahead Adder */
module cla4(X, Y, CIN, S);
    input wire [3:0] X, Y; // Operands
    input wire CIN; // Carry in
    output wire [3:0] S; // Sum outputs

    wire [3:0] C; // Carry equations (C[3] is Cout)
    wire [3:0] P, G;

    assign G = X & Y; // Generate functions G[0] = X[0]&Y[0]; G[1] = .. so on
    assign P = X ^ Y; // Propagate functions P[0] = X[0]^Y[0]; P[1] = .. so on

    // Carry function definitions
    assign C[0] = G[0] | CIN & P[0];
    assign C[1] = G[1] | G[0] & P[1] | CIN & P[0] & P[1];
    assign C[2] = G[2] | G[1] & P[2] | G[0] & P[1] & P[2] | CIN & P[0] & P[1] & P[2];
    assign C[3] = G[3] | G[2] & P[3] | G[1] & P[2] & P[3] | G[0] & P[1] & P[2] & P[3]
                | CIN & P[0] & P[1] & P[2] & P[3];

    assign S[0] = CIN ^ P[0];
    assign S[3:1] = C[2:0] ^ P[3:1];
endmodule
    
```

Example – Sample 4-bit CLA Realization

Timing Analysis for ispMACH 4256ZE 5.8 ns CPLD

Delay	Level	Source	Destination
6.40	1	CIN	S3
6.40	1	X0	S3
6.40	1	Y0	S3
6.35	1	X1	S3
6.35	1	Y1	S3
6.30	1	X2	S3
6.30	1	Y2	S3
6.25	1	Y3	S3
5.95	1	CIN	S0
5.95	1	CIN	S1
5.95	1	CIN	S2
5.95	1	X0	S0
5.95	1	X0	S1
5.95	1	X0	S2
5.95	1	Y0	S0
5.95	1	Y0	S1
5.95	1	Y0	S2

Example – CLA Realization Using + Operator

```

/* 4-bit Carry Look-Ahead Adder Using + Operator */
module cla4p(X, Y, CIN, S);
    input wire [3:0] X, Y; // operands
    input wire CIN; // LSB carry-in
    output wire [3:0] S; // sum outputs

    assign S = X + Y + {3'b000,CIN};
endmodule
    
```

Note: The “+” operator in Verilog synthesizes most suitable adder realization based on optimization constraints (area, fmax, etc.)

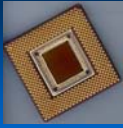
Example – CLA Realization Using + Operator

Timing Analysis for ispMACH 4256ZE 5.8 ns CPLD

Delay	Level	Source	Destination
6.40	1	CIN	S3
6.40	1	X0	S3
6.40	1	Y0	S3
6.35	1	X1	S3
6.35	1	Y1	S3
5.95	1	CIN	S1
5.95	1	CIN	S2
5.95	1	X0	S0
5.95	1	X0	S1
5.95	1	X0	S2
5.95	1	Y0	S0
5.95	1	Y0	S1
5.95	1	Y0	S2

Obtain same timing results as “hand coded” CLA equations!

- ### Observations
- Note that *regardless* of the adder length (n), the time required to produce *any* sum digit is the *same* – i.e., all sum digits are produced *in parallel*
 - Large CLA adders are difficult to build in practice because of the “product term explosion” that occurs as the carry equations are expanded
 - A reasonable compromise is to make a *group ripple adder* by cascading m -bit CLA blocks together to make a $k \times m$ -bit adder (where k is the number of CLA blocks)
 - The “+” operator in Verilog synthesizes most suitable adder realization based on *optimization constraints* (area, fmax, etc.)



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Introduction to Digital System Design

Module 4-E Multiplier Circuits

Reading Assignment:
 DDPP 4th Ed. pp. 45-47, 494-496, 503; 5th Ed. pp. 54-56, 416-419

Learning Objectives:

- Describe the operation of an unsigned multiplier array constructed using full adders
- Determine the full adder arrangement and organization (rows/diagonals) needed to construct an NxM-bit unsigned multiplier array
- Determine the worst case propagation delay incurred by a practical (PLD-based) realization of an NxM-bit unsigned multiplier array

Outline

- Overview
- Product components
- Example circuit
- Critical path analysis
- Generalizations
- Realizations in Verilog

Overview

Consider a 3x3 unsigned binary multiplication:

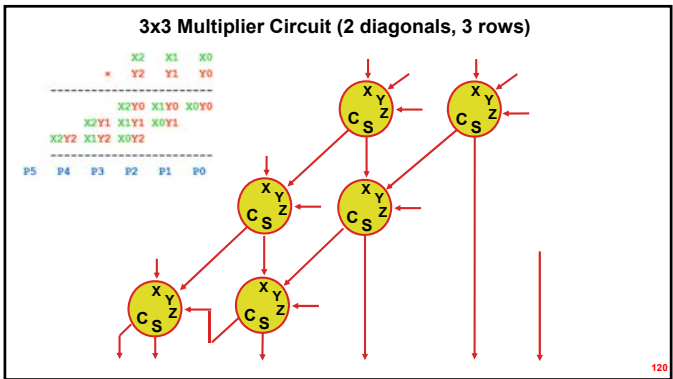
```

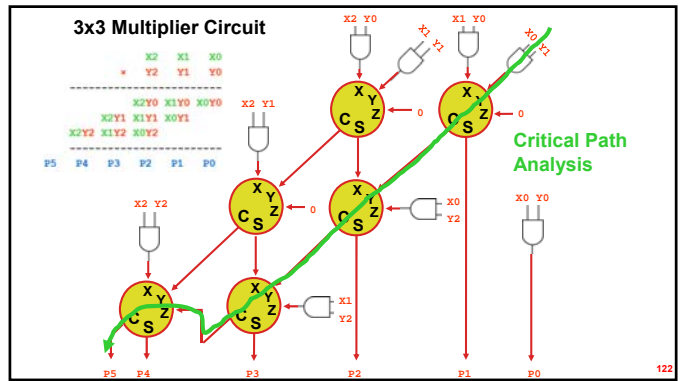
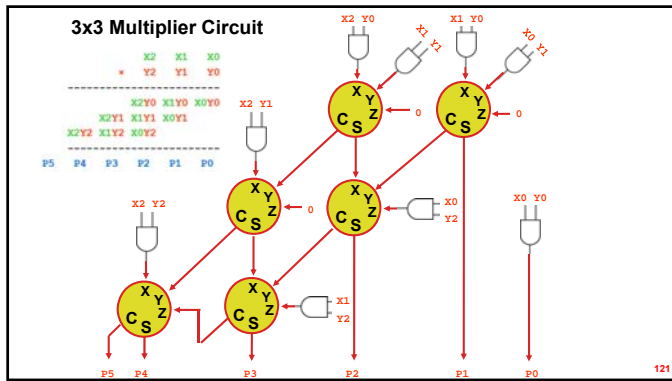
Multiplicand:      X2  X1  X0
Multiplier:      x  Y2  Y1  Y0
-----
                X2Y0 X1Y0 X0Y0
                X2Y1 X1Y1 X0Y1
                X2Y2 X1Y2 X0Y2
-----
P5  P4  P3  P2  P1  P0
    
```

Product

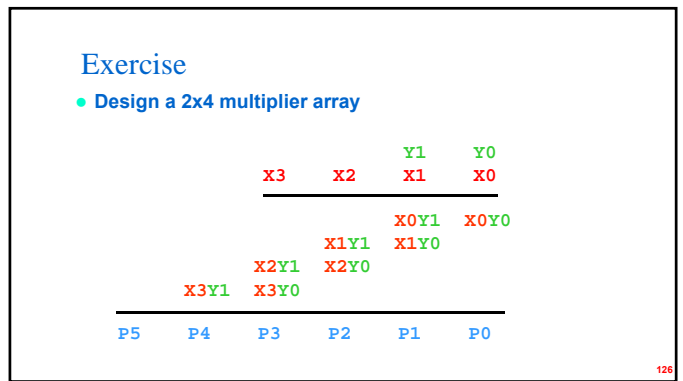
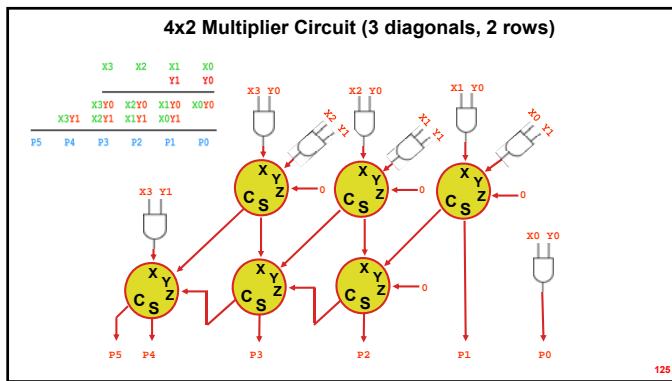
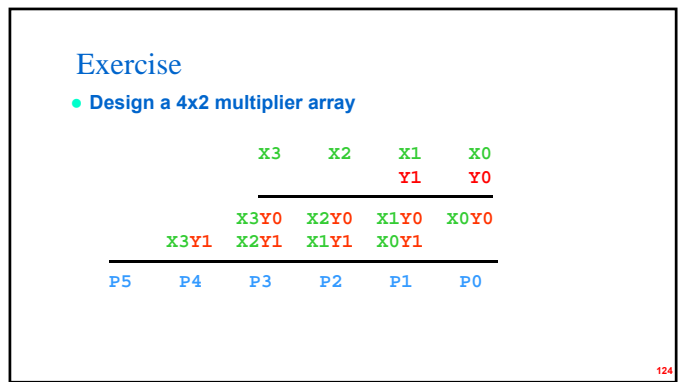
Product Components

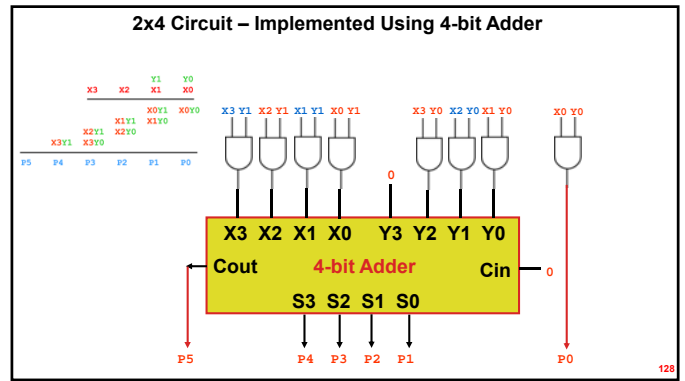
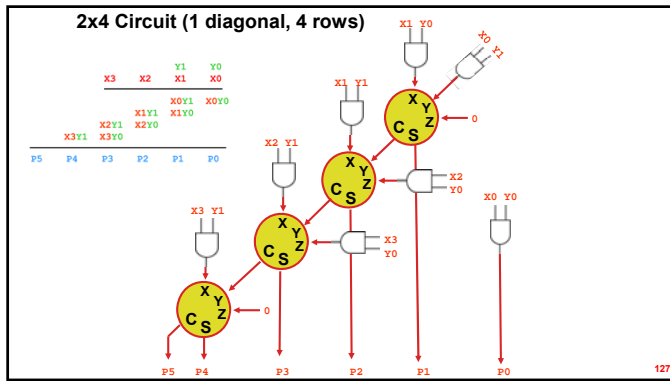
- Most approaches to (unsigned) combinational binary multiplication are based on the “paper-and-pencil” *shift and add* algorithm
- Each row is called a **product component** – a shifted multiplicand that is multiplied by 0 or 1 depending on the corresponding multiplier bit
- Each $x_i y_j$ term represents a **product component bit** (the logical AND of multiplicand bit x_i with multiplier bit y_j)
- The **product** $P = p_5 p_4 p_3 p_2 p_1 p_0$ is obtained by adding together all the product components





- ### Generalizations
- Generalizations for an $N \times M$ multiplier
 - N = number of bits in **multiplicand** (top)
 - M = number of bits in **multiplier** (bottom)
 - produces an $N+M$ digit result
 - requires $N \times M$ AND gates to generate the product components
 - requires $N-1$ **diagonals** of full adders
 - requires M **rows** of full adders
- 123





Clicker
 Quiz

- ### Generalizations – Review
- Generalizations for an $N \times M$ multiplier
 - N = number of bits in **multiplier** (top)
 - M = number of bits in **multiplicand** (bottom)
 - produces an $N+M$ digit result
 - requires $N \times M$ AND gates to generate the product components
 - requires $N-1$ **diagonals** of full adders
 - requires M **rows** of full adders

1. A 6x4 unsigned binary multiplier array would require ___ rows of full adder cells

A. 3
 B. 4
 C. 5
 D. 6
 E. none of the above

2. A 6x4 unsigned binary multiplier array would require ___ “diagonals” of full adder cells

A. 3
 B. 4
 C. 5
 D. 6
 E. none of the above

3. A 6x4 unsigned binary multiplier array would require ___ full adder cells
- A. 10
 - B. 18
 - C. 20
 - D. 24
 - E. none of the above

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4. A 6x4 unsigned binary multiplier array would require ___ AND gates to generate the product component bits
- A. 10
 - B. 18
 - C. 20
 - D. 24
 - E. none of the above

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5. Assuming a large 10 ns PLD was used to generate each product component bit and implement each full adder cell, the worst case propagation delay of a 6x4 unsigned binary multiplier array would be ___ ns
- A. 80
 - B. 90
 - C. 100
 - D. 110
 - E. none of the above

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6. A 4x6 unsigned binary multiplier array would require ___ rows of full adder cells
- A. 3
 - B. 4
 - C. 5
 - D. 6
 - E. none of the above

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7. A 4x6 unsigned binary multiplier array would require ___ "diagonals" of full adder cells
- A. 3
 - B. 4
 - C. 5
 - D. 6
 - E. none of the above

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8. A 4x6 unsigned binary multiplier array would require ___ full adder cells
- A. 10
 - B. 18
 - C. 20
 - D. 24
 - E. none of the above

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9. A 4x6 unsigned binary multiplier array would require ___ AND gates to generate the product component bits
- A. 10
 - B. 18
 - C. 20
 - D. 24
 - E. none of the above

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10. Assuming a large 10 ns PLD was used to generate each product component bit and implement each full adder cell, the worst case propagation delay of a 4x6 unsigned binary multiplier array would be ___ ns
- A. 80
 - B. 90
 - C. 100
 - D. 110
 - E. none of the above

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Realizations in Verilog

- Keys
 - use *expressions* to define product components
 - use the *addition operator (+)* to form unsigned sum of product components (generates CLA adder equations)
- Example: 4x4 multiplier realization

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```

/* 4x4 Combinational Multiplier */
module mul4x4(X, Y, P);

    input wire [3:0] X, Y; // multiplicand, multiplier
    output wire [7:0] P; // product bits

    wire [7:0] PC[3:0]; // four 8-bit variables

    assign PC[0] = {8{Y[0]}} & {4'b0, X}; // 0000X3X2X1X0
    assign PC[1] = {8{Y[1]}} & {3'b0, X, 1'b0}; // 000X3X2X1X00
    assign PC[2] = {8{Y[2]}} & {2'b0, X, 2'b0}; // 00X3X2X1X000
    assign PC[3] = {8{Y[3]}} & {1'b0, X, 3'b0}; // 0X3X2X1X0000

    assign P = PC[0] + PC[1] + PC[2] + PC[3];

endmodule

```

{8{Y[0]}} will extend the 1-bit signal Y[0] to an 8-bit vector

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Timing Analysis for ispMACH 4256ZE 5.8 ns CPLD

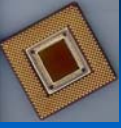
Delay	Level	Source	Destination
6.50	1	X0	P4
6.50	1	X0	P5
6.50	1	X1	P4
6.50	1	X1	P5
6.50	1	X2	P4
6.50	1	X2	P5
6.50	1	Y0	P4
6.50	1	Y0	P5
6.50	1	Y1	P4
6.50	1	Y1	P5
6.50	1	Y2	P4
6.50	1	Y2	P5
6.45	1	X3	P4
6.45	1	X3	P5
6.45	1	Y3	P4
6.45	1	Y3	P5
6.05	1	X0	P0
6.05	1	X0	P1
6.05	1	X0	P2
6.05	1	X0	P3

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Device Resource Summary for ispMACH 4256ZE 5.8 ns CPLD

	Total	Used	Not Used	Utilization
Dedicated Pins				
Clock/Input Pins	4	4	0	100
Input-Only Pins	6	4	2	66
I/O / Enable Pins	2	0	2	0
I/O Pins	62	8	54	12
Logic Functions	256	8	248	3
Input Registers	64	0	64	0
GLB Inputs				
GLB Inputs	576	46	530	7
Logical Product Terms	1280	124	1156	9
Occupied GLBs	16	6	10	37
Macrocells	256	8	248	3
Control Product Terms:				
GLB Clock/Clock Enables	16	0	16	0
GLB Reset/Presets	16	0	16	0
Macrocell Clocks	256	0	256	0
Macrocell Clock Enables	256	0	256	0
Macrocell Enables	256	0	256	0
Macrocell Resets	256	0	256	0
Macrocell Presets	256	0	256	0
Global Routing Pool				
GRP from IFS	324	8	316	2
GRP from input signals	..	4
GRP from output signals	..	4
GRP from bidir signals	..	0
GRP from MPA	..	4

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Introduction to Digital System Design

Module 4-F BCD Adder Circuits

Reading Assignment:
 DDPP 4th Ed. pp. 48-51; 5th Ed. pp. 58-60

Learning Objectives:

- Describe the operation of a binary coded decimal (BCD) "correction circuit"
- Design a BCD full adder circuit
- Design a BCD N-digit radix (base 10) adder/subtractor circuit

Outline

- Overview
- General BCD adder circuit model
- Decimal addition and correction
- Decimal adder circuits
- Nine's complement circuit

Overview

- Even though binary numbers are the most appropriate for the internal computations of a digital system, most people still prefer to deal with decimal numbers
- External interfaces of a digital system may need to read or display decimal numbers, and therefore need to perform arithmetic on decimal numbers directly
- The most commonly used decimal code is *binary-coded decimal* (BCD)
- Some computers place two BCD digits in an 8-bit byte ("packed-BCD format")

Overview

- Consider the problem of adding a pair of BCD digits – the objective is to design a circuit that adds the two 4-bit codes along with a carry in to produce a 4-bit coded sum digit plus a carry out
- We would like to use standard 4-bit binary adder modules (with which we are already familiar) as basic building blocks
- Note that because there are six "unused combinations" in BCD, a *correction* must be performed if the direct sum of the two 4-bit codes exceeds 1001

General BCD Adder Circuit Model

Conventional 4-bit binary adder

Z_4, Z_3, Z_2, Z_1, Z_0 is the *direct sum* obtained from the 4-bit adder

Decimal Addition and Correction

```

    3      0011
  + 4      + 0100
  --      -----
    7      0111
    
```

Result of ADD

Here, direct addition of the 4-bit BCD codes yields the correct 4-bit BCD code for the sum digit

Decimal Addition and Correction

```

    7      0111
  + 8      + 1000
  --      -----
   15      1111
  + 0110
  -----
   1 0101
    
```

Result of ADD
 Since result > 9, add 6 to adjust

Carry out = ten's position

Decimal Addition and Correction

```

    7      0111
  + 9      + 1001
  --      -----
   16      10000
  + 0110
  -----
   1 0110
    
```

Result of ADD
 Since result > 9, add 6 to adjust

Carry out = ten's position

Decimal Adder Circuits

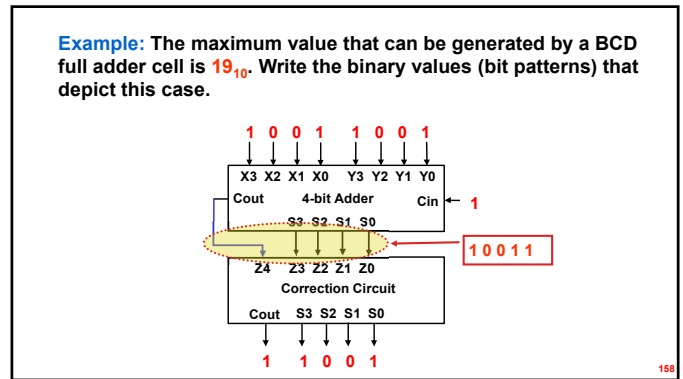
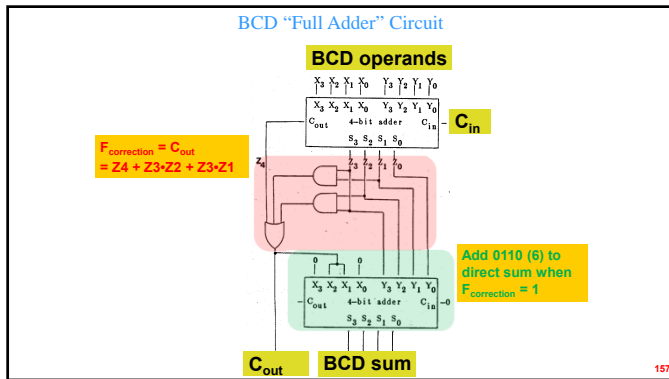
- Summary of rules
 - If the sum of the two BCD digits is less than or equal to nine (1001), **no correction** is needed
 - If the sum is greater than nine, the result obtained directly from the 4-bit adder must be **corrected** in order to represent the proper BCD digit
- Some microprocessors include a "decimal adjust" (DAA) instruction for performing this correction following the addition of BCD operands

Decimal Adder "Correction Function"

N ₁₀	Z ₄ Z ₃ Z ₂ Z ₁ Z ₀	C _{out} S ₃ S ₂ S ₁ S ₀	Correction
0	0 0 0 0 0	0 0 0 0 0	<none>
1	0 0 0 0 1	0 0 0 0 1	<none>
2	0 0 0 1 0	0 0 0 1 0	<none>
3	0 0 0 1 1	0 0 0 1 1	<none>
4	0 0 1 0 0	0 0 1 0 0	<none>
5	0 0 1 0 1	0 0 1 0 1	<none>
6	0 0 1 1 0	0 0 1 1 0	<none>
7	0 0 1 1 1	0 0 1 1 1	<none>
8	0 1 0 0 0	0 1 0 0 0	<none>
9	0 1 0 0 1	0 1 0 0 1	<none>
10	0 1 0 1 0	1 0 0 0 0	<add 6>
11	0 1 0 1 1	1 0 0 0 1	<add 6>
12	0 1 1 0 0	1 0 0 1 0	<add 6>
13	0 1 1 0 1	1 0 0 1 1	<add 6>
14	0 1 1 1 0	1 0 1 0 0	<add 6>
15	0 1 1 1 1	1 0 1 0 1	<add 6>
16	1 0 0 0 0	1 0 1 1 0	<add 6>
17	1 0 0 0 1	1 0 1 1 1	<add 6>
18	1 0 0 1 0	1 1 0 0 0	<add 6>
19	1 0 0 1 1	1 1 0 0 1	<add 6>

Decimal Adder "Correction Function"

$F_{\text{correction}} = C_{\text{out}} = Z_4 + Z_3 \cdot Z_2 + Z_3 \cdot Z_1$



Clicker Quiz

- If the BCD codes for 8 and 5 were added using a decimal full adder cell, with $C_{IN} = 1$, the resulting 5-bit output ($C_{out} S_3 S_2 S_1 S_0$) would be:
 - A. 0 1 1 0 1
 - B. 0 1 1 1 0
 - C. 1 0 0 1 1
 - D. 1 0 1 0 0
 - E. none of the above

- If the BCD codes for 4 and 5 were added using a decimal full adder cell, with $C_{IN} = 1$, the resulting 5-bit output ($C_{out} S_3 S_2 S_1 S_0$) would be:
 - A. 0 1 0 0 1
 - B. 0 1 0 1 0
 - C. 1 0 0 0 0
 - D. 1 0 0 0 1
 - E. none of the above

Decimal Adder Circuits

- Thought questions:
 - How could an n -digit BCD adder be constructed using the "decimal full adder" circuit just designed?
 - How could this n -digit BCD adder be made into an n -digit BCD adder/subtractor?

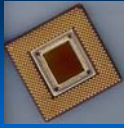
Hint: How could the radix complement of a BCD digit (where the radix or base is 10) be generated?

Example: Verilog program that generates the *diminished radix* (or 9's) complement of a BCD digit

```

module ninescmp(X, Y); // Nine's Complement Box
    input wire [3:0] X; // input code
    output reg [3:0] Y; // output code

    always @ (X) begin
        case (X)
            4'b0000: Y = 4'b1001;
            4'b0001: Y = 4'b1000;
            4'b0010: Y = 4'b0111;
            4'b0011: Y = 4'b0110;
            4'b0100: Y = 4'b0101;
            4'b0101: Y = 4'b0100;
            4'b0110: Y = 4'b0011;
            4'b0111: Y = 4'b0010;
            4'b1000: Y = 4'b0001;
            4'b1001: Y = 4'b0000;
            default: Y = 4'b0000; // used for inputs > 9
        endcase
    end
endmodule
    
```



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Introduction to Digital System Design

Module 4-G
Simple Computer Top-Down Specification

- Reading Assignment:**
 Meyer *Supplemental Text*, pp. 1-18
- Learning Objectives:**
- Define computer architecture, programming model, and instruction set
 - Describe the top-down specification, bottom-up implementation strategy as it pertains to the design of a computer
 - Describe the characteristics of a “two address machine”
 - Describe the contents of memory: program, operands, results of calculations
 - Describe the format and fields of a basic machine instruction (opcode and address)
 - Describe the purpose/function of each basic machine instruction (LDA, STA, ADD, SUB, AND, HLT)
 - Define what is meant by “assembly-level” instruction mnemonics
 - Draw a diagram of a simple computer, showing the arrangement and interconnection of each functional block

- Outline**
- Introduction
 - Top-Down, Bottom-Up Design Methodology
 - Simple Computer “Big Picture”
 - A Simple Instruction Set
 - A Simple Programming Example
 - System Block Diagram

- Introduction**
- The focus thus far has been on a number of digital system “building blocks”
 - state machines
 - latches and flip-flops
 - arithmetic logic circuits
 - decoders, encoders, multiplexers
 - basic gates (NAND, NOR, XOR, etc.)
 - **Question:** What is the primary utility of these building blocks?
- Building a computer or interfacing to an existing one**

- Introduction**
- **Question:** What is a computer?
A device that sequentially executes a stored program (or, a device that stores and manipulates state)
 - **Question:** What is a microprocessor?
A single-chip embodiment of the major functional blocks of a computer
 - **Question:** What is a microcontroller?
A microprocessor with a number of integrated peripherals typically used in control-oriented applications

Introduction


- **Question:** How can we apply what we know about various digital system building blocks to design a simple computer?

We need a **structured approach** that enables us to transform a “word” description of what a computer does into a block diagram

- **Definition:** The **architecture** of a computer is the **arrangement** and **interconnection** of its functional blocks

Introduction

- **Analogy:** Designing and building a house - 1
 – start with the “big picture”...




Introduction

- **Analogy:** Designing and building a house - 2
 – then develop a “floor plan”...



Introduction

- **Analogy:** Designing and building a house - 3
 – then embellish the floor plan with details (outlets, lights, plumbing, HVAC, etc.)



Introduction

- **Analogy:** Designing and building a house - 4
 – When you’re ready to build, how do you proceed?

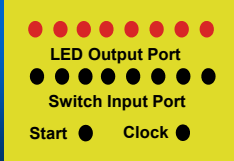
From the **ground-up** – start with the foundation, create basic structure, embellish with finishing details

- **Question:** What would you call the basic procedure we have just described?

Top-down specification of functionality, **bottom-up implementation** of basic blocks

Simple Computer “Big Picture”

- We wish to apply this “top-down, bottom-up” methodology to the design of a simple 8-bit computer (or, microprocessor”)
- **First step:** Draw the **big picture**



Simple Computer "Floor Plan"

- **Question:** In the design of a computer, what is analogous to the *floor plan* of a house?

The computer's **programming model** and **instruction set**

- **Definition:** The **programming model** of a computer is the set of "user" registers available to the programmer
- **Definition:** A collection of two or more flip-flops with a common clock (and generally a common purpose) is called a **register**

In the simple computer designed here, the programming model will contain a single **data register** "where the result accumulates" (the **accumulator**, or "A register" for short), plus **condition codes** or **flags** (C, V, N, Z)

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Simple Computer "Floor Plan"

- **Definition:** The **instruction set** of a computer is the set of operations the computer can be programmed to perform on data
- Instructions typically consist of several fields that indicate the **operation** to be performed ("operation code", or **opcode**) and the **data** on which the operation is to be performed (specified using an **addressing mode**)
- Our 8-bit computer will utilize a 3-bit opcode field (thus allowing 8 different kinds of instructions to be implemented) and a 5-bit address field (thus allowing 32 locations)

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Simple Computer "Floor Plan"

- Instruction format:

XXX YYYYY

XXX – indicates operation to perform ("opcode")

YYYYY – indicates location of operand ("address")

Called a "**two address machine**" since one operand will be the accumulator ("A") register and the other operand will be obtained from the specified location in memory

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Simple Computer "Floor Plan"

- Instruction set:

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	ADD <i>addr</i>	Add contents of <i>addr</i> to contents of A
0 1 1	SUB <i>addr</i>	Subtract contents of <i>addr</i> from contents of A
1 0 0	AND <i>addr</i>	AND contents of <i>addr</i> with contents of A
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>

Note: We will use **parentheses** to denote the **contents** of a register or memory location, e.g., "**(A)**" is read as "the contents of A"

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Simple Programming Example

Addr	Instruction	Comments
00000	LDA 01011	Load A with contents of location 01011
00001	ADD 01100	Add contents of location 01100 to A
00010	STA 01101	Store contents of A at location 01101
00011	LDA 01011	Load A with contents of location 01011
00100	AND 01100	AND contents of 01100 with contents of A
00101	STA 01110	Store contents of A at location 01110
00110	LDA 01011	Load A with contents of location 01011
00111	SUB 01100	Subtract contents of location 01100 from A
01000	STA 01111	Store contents of A at location 01111
01001	HLT	Stop – discontinue execution

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Location	Contents
00000	001 01011
00001	010 01100
00010	101 01101
00011	001 01011
00100	100 01100
00101	101 01110
00110	001 01011
00111	011 01100
01000	101 01111
01001	000 00000
01010	
01011	10101010
01100	01010101
01101	
01110	
01111	

Memory "Snapshot"

Program

Operands

Results

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Location	Contents
00000	001 01011
00001	010 01100
00010	101 01101
00011	001 01011
00100	100 01100
00101	101 01110
00110	001 01011
00111	011 01100
01000	101 01111
01001	000 00000
01010	
01011	10101010
01100	01010101
01101	11111111 ← ADD
01110	
01111	

Add:

```

10101010
+01010101
-----
11111111
    
```

CF = 0
 NF = 1
 VF = 0
 ZF = 0

Location	Contents
00000	001 01011
00001	010 01100
00010	101 01101
00011	001 01011
00100	100 01100
00101	101 01110
00110	001 01011
00111	011 01100
01000	101 01111
01001	000 00000
01010	
01011	10101010
01100	01010101
01101	11111111
01110	00000000 ← AND
01111	

AND:

```

10101010
^01010101
-----
00000000
    
```

CF = <unaffected>
 NF = 0
 VF = <unaffected>
 ZF = 1

Location	Contents
00000	001 01011
00001	010 01100
00010	101 01101
00011	001 01011
00100	100 01100
00101	101 01110
00110	001 01011
00111	011 01100
01000	101 01111
01001	000 00000
01010	
01011	10101010
01100	01010101
01101	11111111
01110	00000000
01111	01010101 ← SUB

Sub:

```

10101010
-01010101
-----
11010101
    
```

CF = 1
 NF = 0
 VF = 1
 ZF = 0

Overflow!

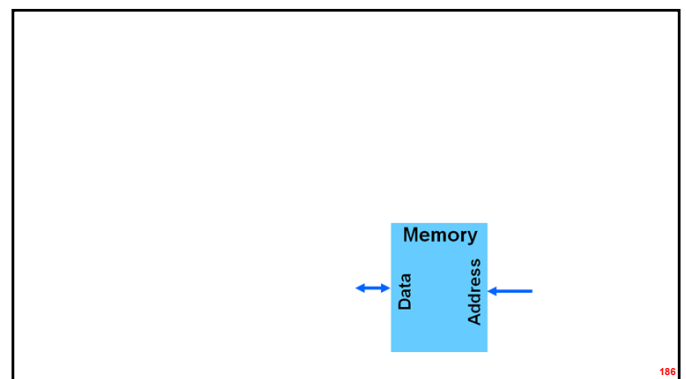
Simple Computer Block Diagram

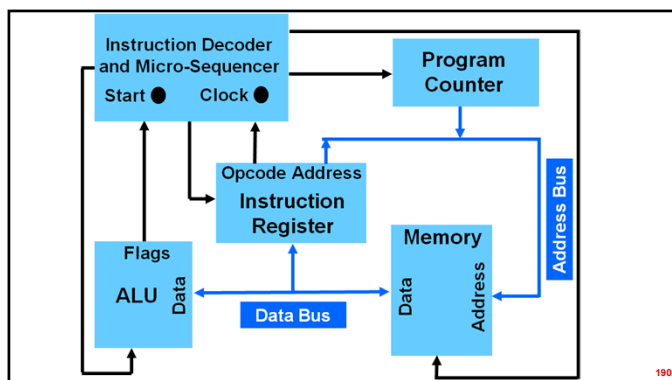
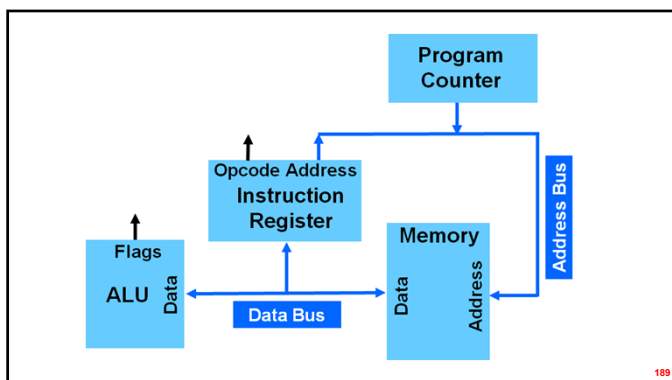
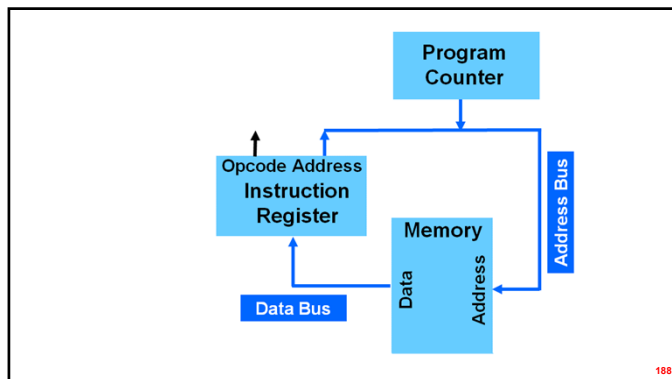
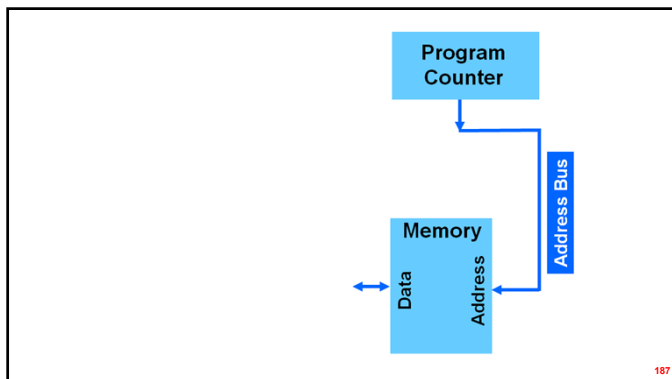
- **Question:** What functional blocks are necessary to implement a computer that executes a stored program consisting of the instructions we have just defined?

Two basic steps are required to perform an instruction: (1) it must be *fetched* from memory, and (2) it must be *decoded and executed*

Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – *memory*
 - a way to keep track of which instruction is to be executed next – *program counter (PC)*
 - a place to temporarily “stage” an instruction while it is being executed – *instruction register (IR)*
 - a way to perform arithmetic and logic operations – *arithmetic logic unit (ALU)*
 - a way to coordinate and sequence the functions of the machine – *instruction decoder and micro-sequencer (IDMS)*





- ### Notes About Block Diagram
- Each functional block is "self-contained" (which means each block can be designed and tested *independently*)
 - Additional instructions can be added by increasing the number of *opcode* bits
 - Additional memory can be added by increasing the number of *address* bits
 - The numeric range can be expanded by increasing the number of *data* bits

Clicker
Quiz

- Q1. The next instruction to fetch from memory is pointed to by the:
- A. accumulator
 - B. program counter
 - C. instruction register
 - D. microsequencer
 - E. none of the above

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- Q2. The place where an instruction fetched from memory is "staged" while it is being decoded and executed is the:
- A. accumulator
 - B. program counter
 - C. instruction register
 - D. microsequencer
 - E. none of the above

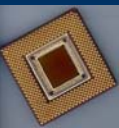
194

- Q3. If two additional address bits were added to the Simple Computer, the *number of memory locations* the machine could access would increase:
- A. by two locations
 - B. by four locations
 - C. by two times the original number of locations
 - D. by four times the original number of locations
 - E. none of the above

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- Q4. The expression $(10110) \leftarrow (A) + (10110)$ means:
- A. replace the contents of the accumulator with the sum of its current contents plus the contents of memory location 10110
 - B. replace the contents of the accumulator with the sum of its current contents plus the constant 10110
 - C. replace the contents of memory location 10110 with the sum of its current contents plus the contents of the accumulator
 - D. add the constant 10110 to the contents of the accumulator and store the result in memory location 10110
 - E. none of the above

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Introduction to Digital System Design

Module 4-H
Simple Computer Instruction Execution Tracing

Reading Assignment:
Meyer Supplemental Text, pp. 18-24

Learning Objectives:

- Trace the execution of a computer program, identifying each step of an instruction's microsequence (fetch and execute cycles)
- Distinguish between synchronous and combinational system control signals

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Outline

- Review of top-down specification phase of design process
 - Big picture
 - Floor plan (instruction set)
 - Block diagram
- Instruction execution tracing

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Simple Computer “Floor Plan”

- Instruction set:

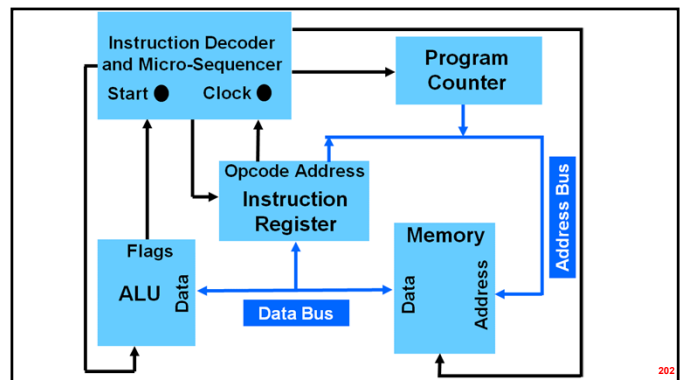
Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	ADD <i>addr</i>	Add contents of <i>addr</i> to contents of A
0 1 1	SUB <i>addr</i>	Subtract contents of <i>addr</i> from contents of A
1 0 0	AND <i>addr</i>	AND contents of <i>addr</i> with contents of A
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>

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Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – *memory*
 - a way to keep track of which instruction is to be executed next – *program counter (PC)*
 - a place to temporarily “stage” an instruction while it is being executed – *instruction register (IR)*
 - a way to perform arithmetic and logic operations – *arithmetic logic unit (ALU)*
 - a way to coordinate and sequence the functions of the machine – *instruction decoder and micro-sequencer (IDMS)*

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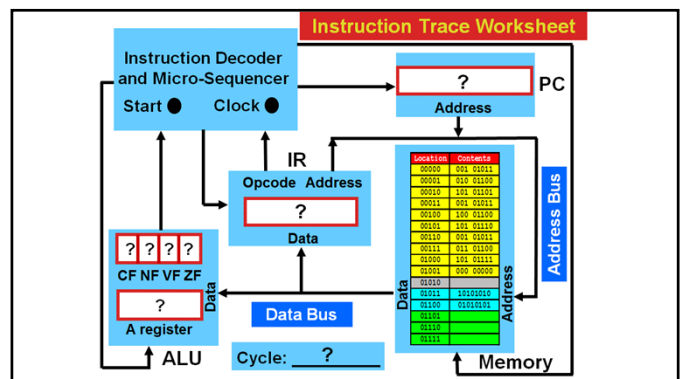


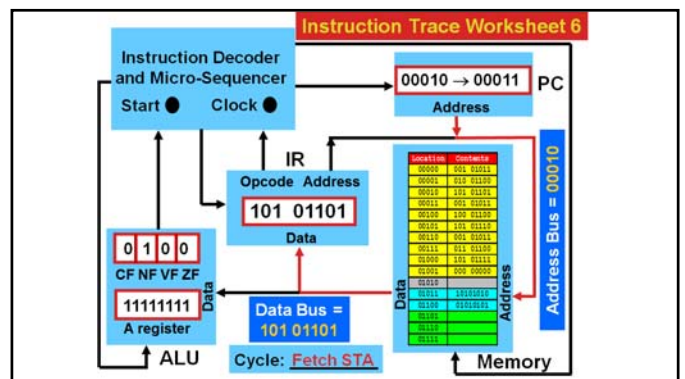
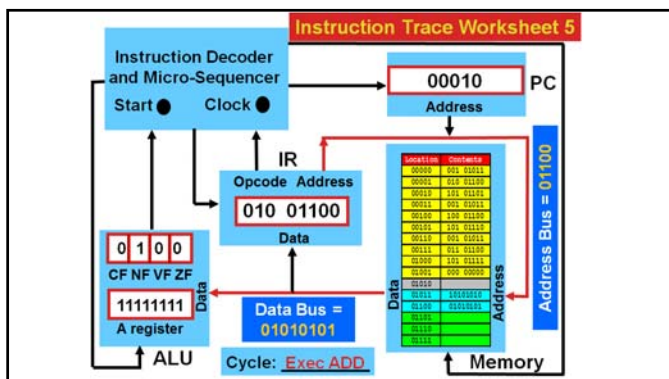
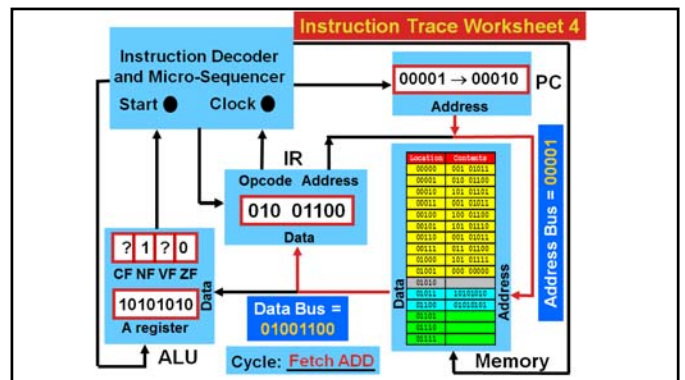
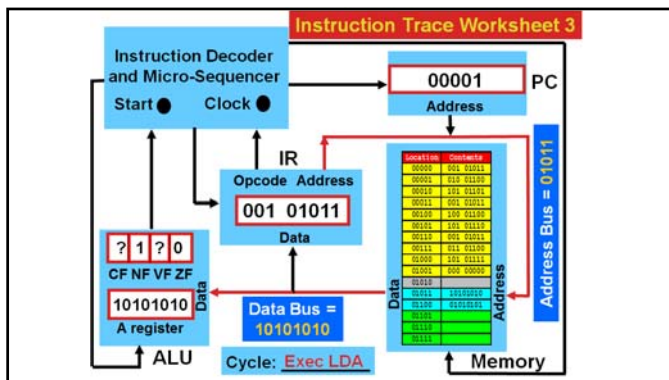
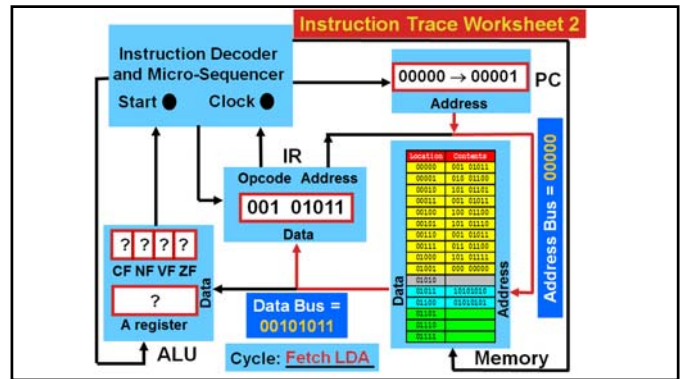
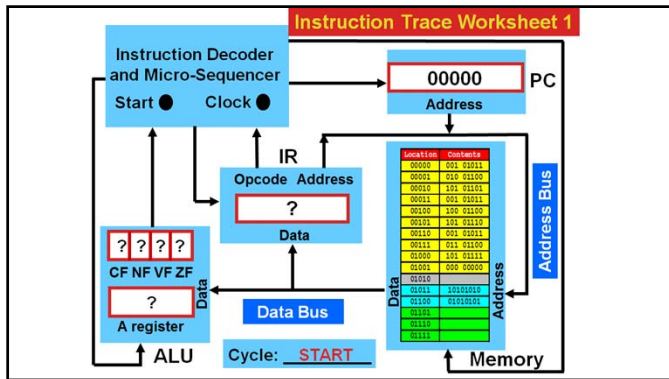
202

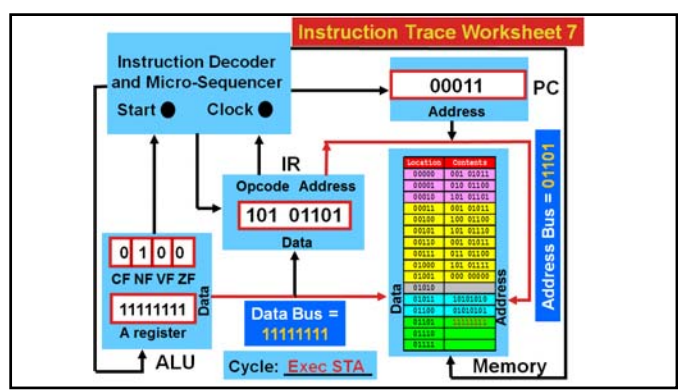
Simple Programming Example

Addr	Instruction	Comments
00000	LDA 01011	Load A with contents of location 01011
00001	ADD 01100	Add contents of location 01100 to A
00010	STA 01101	Store contents of A at location 01101
00011	LDA 01011	Load A with contents of location 01011
00100	AND 01100	AND contents of 01100 with contents of A
00101	STA 01110	Store contents of A at location 01110
00110	LDA 01011	Load A with contents of location 01011
00111	SUB 01100	Subtract contents of location 01100 from A
01000	STA 01111	Store contents of A at location 01111
01001	HLT	Stop – discontinue execution

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Notes About Instruction Tracing

- The clock edges drive the **synchronous** functions of the computer (e.g., increment program counter, load instruction register)
- The decoded states (here, fetch and execute) enable the **combinational** functions of the computer (e.g., turn on tri-state buffers)

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Introduction to Digital System Design

Module 4-I

Simple Computer Bottom-Up Realization

Reading Assignment:

Meyer Supplemental Text, pp. 24-42

Learning Objectives:

- Describe the operation of memory and the function of its control signals: MSL, MOE, and MWE
- Describe the operation of the program counter (PC) and the function of its control signals: ARS, PCC, and POA
- Describe the operation of the instruction register (IR) and the function of its control signals: IRL and IRA
- Describe the operation of the ALU and the function of its control signals: ALE, ALX, ALY, and AOE
- Describe the operation of the instruction decoder/microsequencer and derive the system control table
- Describe the basic hardware-imposed system timing constraints
- Discuss how the instruction register can be loaded with the contents of the memory location pointed to be the program counter *and* the program counter can be incremented on the same clock edge

Outline

- Bottom-up Realization Phase of Design Process
 - Memory
 - Program Counter
 - Instruction Register
 - Arithmetic Logic Unit
 - Instruction Decoder and Microsequencer
- System Data Flow and Timing Analysis

Bottom-Up Implementation

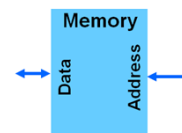
- Having finished the “top-down” **specification** phase of the design process, we are now ready to **implement** each block identified from the “bottom-up”
- Note that, in practice, an important aspect of this process is to **independently test** (and debug) each block (or module) of the system **as it is implemented**
- If each module is independently tested and verified as it is implemented, then – when the modules are assembled together into a system – there is a much higher probability that it will “work the first time”!

Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – **memory**
 - a way to keep track of which instruction is to be executed next – **program counter (PC)**
 - a place to temporarily “stage” an instruction while it is being executed – **instruction register (IR)**
 - a way to perform arithmetic and logic operations – **arithmetic logic unit (ALU)**
 - a way to coordinate and sequence the functions of the machine – **instruction decoder and micro-sequencer (IDMS)**

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Read/Write Memory (RWM)



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Read/Write Memory (RWM)

- The name **read/write memory (RWM)** is given to memory arrays in which we can store and retrieve information at any time
- Most of the RWMs used in digital systems are **random-access memories (RAMs)**, which means that the time it takes to read or write a bit of memory is independent of the bit's location in the RAM
- In a static RAM (SRAM), once data is written to a given location, it remains stored as long as **power** is applied to the chip
- If power is removed, data is lost – this is referred to as a **volatile memory**

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Read/Write Memory (RWM)

- An SRAM has three (typically **active low**) control inputs:
 - a **chip select (CS)** signal that serves as the overall enable for the memory chip
 - an **output enable (OE)** signal that tells the memory chip to drive the data output lines with the contents of the memory location specified on its address lines
 - a **write enable (WE)** signal that tells the memory chip to write the data supplied on its data input lines at the memory location specified on its address lines

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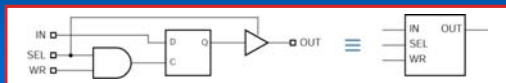
Read/Write Memory (RWM)

- SRAM normally has two **access operations**:
 - **READ**: An address is placed on the address lines while CS and OE are asserted; the latch outputs for the selected location are output on the data lines
 - **WRITE**: An address is placed on the address lines, data is placed on the data lines, then CS and WE are asserted; the latches of the selected location open, and the data is stored

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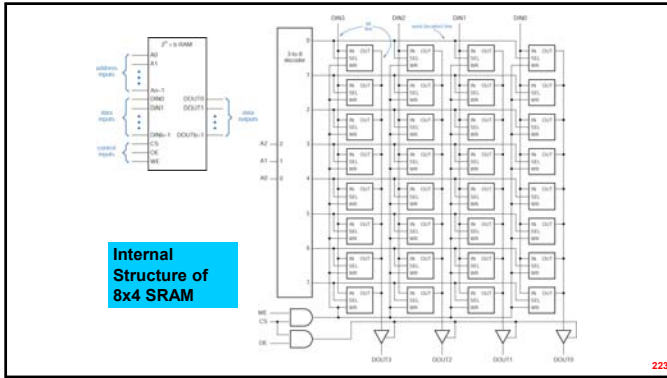
Read/Write Memory (RWM)

- Each bit of memory (or SRAM cell) in a static RAM behaves as the circuit depicted below



- When the SEL input is asserted, the stored data is placed on the cell's output
- When both SEL and WR are asserted, the latch is open and a new data bit is stored
- SRAM cells are combined in an array with additional control logic to form a complete static RAM

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Read/Write Memory (RWM)

- Some things to note:
 - during **read** operations, the output data is a combinational function of the address inputs, so no “harm” is done by changing the address while CS and OE are asserted
 - during **write** operations, data is stored in latches – this means that data must meet certain **setup and hold times** with respect to the **negation** of the WE signal
 - also during **write** operations, the address lines must be stable for a certain setup time **before** WR is asserted internally and for a hold time **after** WR is negated

Read/Write Memory (RWM)

- Most SRAMs utilize a **bi-directional data bus** (i.e., the same data pins are used for reading and writing data)

The diagram shows a bi-directional data bus for an SRAM. It features a 4-bit data bus (D0-D3) and control signals WE, CS, and OE. The data bus is connected to the internal SRAM cells. The WE, CS, and OE signals are connected to the word lines, bit lines, and sense amplifiers respectively.

Simple Computer Memory

- The memory for our simple computer will contain 32 locations (5-bit address), each 8 bits wide (i.e., a “32x8” memory)
- The memory subsystem will have three control signals:
 - MSL: Memory SeLect**
 - MOE: Memory Output Enable**
 - MWE: Memory Write Enable**

NOTE: For simplicity (and clarity) all system control signals as well as address and data bus signals will be assumed to be ACTIVE HIGH

Clicker Quiz

Q1. When a set of control signals are said to be **mutually exclusive**, it means that:

- all the control signals may be asserted simultaneously
- only one control signal may be asserted at a given instant
- each control signal is dependent on the others
- any combination of control signals may be asserted at a given instant
- none of the above

Q2. For the memory subsystem, the set of signals that are mutually exclusive is:

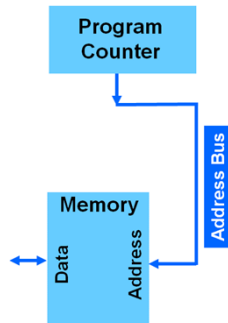
- A. MSL and MOE
- B. MSL and MWE
- C. MOE and MWE
- D. MSL, MOE, and MWE
- E. none of the above

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Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – *memory*
 - a way to keep track of which instruction is to be executed next – *program counter (PC)*
 - a place to temporarily “stage” an instruction while it is being executed – *instruction register (IR)*
 - a way to perform arithmetic and logic operations – *arithmetic logic unit (ALU)*
 - a way to coordinate and sequence the functions of the machine – *instruction decoder and micro-sequencer (IDMS)*

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Program Counter

- The *program counter (PC)* is basically a binary “up” counter with tri-state outputs
- The functions and corresponding control signals required are as follows:
 - **ARS**: **A**synchronous **R**e**S**et
 - **PCC**: **P**rogram **C**ounter **C**ount enable
 - **POA**: **P**rogram counter **O**utput on **A**ddress bus tri-state buffer enable

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```

/* Program Counter Module */
module pc(CLK, PCC, POA, RST, ADRBUS_z);
input wire CLK;
input wire PCC; // PC count enable
input wire POA; // PC output on address bus tri-state enable
input wire RST; // asynchronous reset (connected to START)
output wire [4:0] ADRBUS_z;

wire [4:0] next_PC;
reg [4:0] PC;

assign ADRBUS_z = POA ? PC : 5'bZZZZZ;

always @ (posedge CLK, posedge RST) begin
if (RST == 1'b1)
PC <= 5'b00000;
else
PC <= next_PC;
end

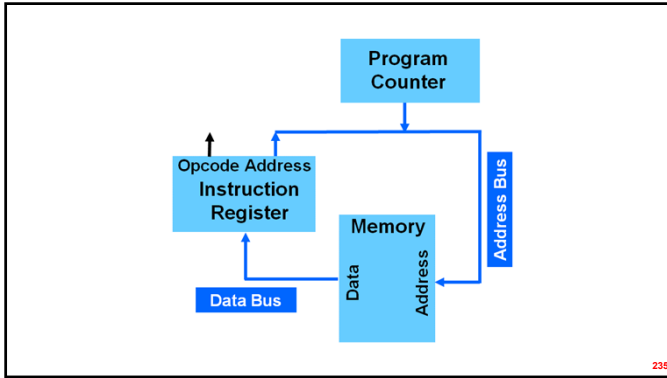
// (PCC) ? count up : retain value;
assign next_PC = (PCC) ? (PC+1) : PC;
endmodule
    
```

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Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – *memory*
 - a way to keep track of which instruction is to be executed next – *program counter (PC)*
 - a place to temporarily “stage” an instruction while it is being executed – *instruction register (IR)*
 - a way to perform arithmetic and logic operations – *arithmetic logic unit (ALU)*
 - a way to coordinate and sequence the functions of the machine – *instruction decoder and micro-sequencer (IDMS)*

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Instruction Register

- The *instruction register* (IR) is basically an 8-bit data register, with tri-state outputs on the lower 5 bits
- Note that the upper 3 bits (opcode field) are output directly to the instruction decoder and micro-sequencer
- The functions and corresponding control signals required are as follows:
 - IRL: Instruction Register Load enable
 - IRA: Instruction Register Address field tri-state output enable

```

/* Instruction Register Module */
module ir(CLK, IR_z, DB_z, IRL, IRA);
    input wire CLK;
    input wire IRL; // IR load enable
    input wire IRA; // IR output on address bus enable
    input wire [7:0] DB_z; // data bus
    output wire [7:0] IR_z; // IR_s[4]..IR_s[0] connected to address bus
                        // IR_s[7]..IR_s[5] supply opcode to IDMS

    reg [7:0] IR;
    wire [7:0] next_IR;

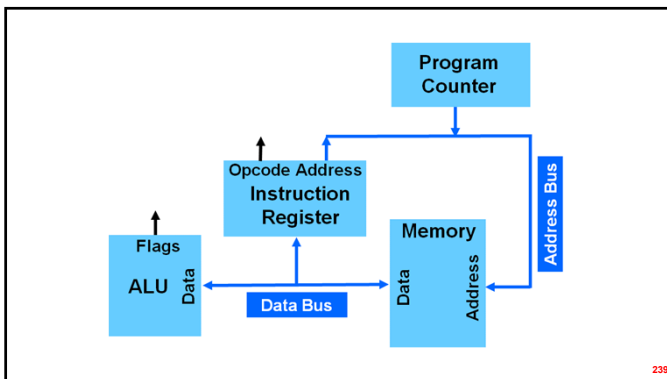
    assign IR_z[4:0] = IRA ? IR[4:0] : 5'bzzzzz;
    assign IR_z[7:5] = IR[7:5];

    always @ (posedge CLK) begin
        IR <= next_IR;
    end

    // (IRL) ? load : retain state (select load or retain state based on IRL)
    assign next_IR = (IRL) ? DB_z : IR;
endmodule
    
```

Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – *memory*
 - a way to keep track of which instruction is to be executed next – *program counter (PC)*
 - a place to temporarily “stage” an instruction while it is being executed – *instruction register (IR)*
 - a way to perform arithmetic and logic operations – *arithmetic logic unit (ALU)*
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Arithmetic Logic Unit

- The *arithmetic logic unit* (ALU) is a multi-function register that performs all the arithmetic and logical (Boolean) operations necessary to implement the instruction set
- The functions and corresponding control signals required are as follows:
 - ALE: ALU Enable
 - ALX: ALU “X” function select
 - ALY: ALU “Y” function select
 - AOE: A register tri-state Output Enable


```

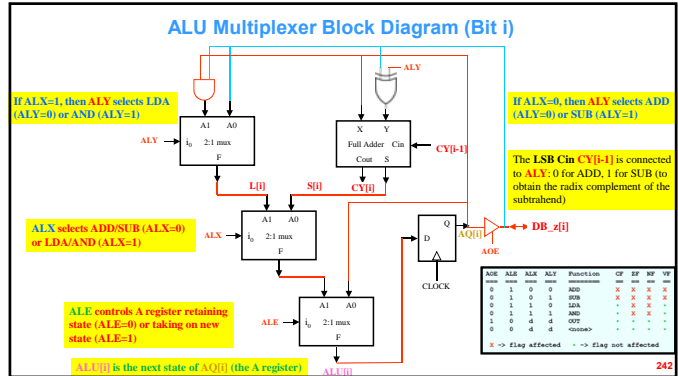
/* ALU Module */
module alu(CLK, ALE, AOE, ALX, ALY, DB_z, CF, VF, NF, ZF);
/* 8-bit, 4-function ALU with bi-directional data bus
Accumulator register is AQ, tri-state data bus is DB_z

ADD: (AQ[7:0]) <- (AQ[7:0]) + DB_z[7:0]
SUB: (AQ[7:0]) <- (AQ[7:0]) - DB_z[7:0]
LDA: (AQ[7:0]) <- DB_z[7:0]
AND: (AQ[7:0]) <- (AQ[7:0]) & DB_z[7:0]
OUT: Value in AQ[7:0] output on data bus DB_z[7:0]

AOE ALE ALX ALY Function CF ZF NF VF
=== === === === =====
0 1 0 0 ADD X X X X
0 1 0 1 SUB X X X X
0 1 1 0 LDA X X X
0 1 1 1 AND X X
1 0 d d OUT o + +
0 0 d d <none> . . . .

X -> flag affected . -> flag not affected

Note: If ALE = 0, the state of all register bits should be retained */
    
```



```

input wire CLK;
// ALU control lines
input wire ALE; // overall ALU enable
input wire AOE; // data bus tri-state output enable
input wire ALX, ALY; // function select
inout wire [7:0] DB_z; // bidirectional 8-bit tri-state data bus
output reg CF, VF, NF, ZF; // condition code register bits (flags)
wire [7:0] S; // Carry, Overflow, Negative, Zero
// Carry equations
wire [7:0] CY;
// Combinational ALU outputs
wire [7:0] ALU; // Adder/subtractor sum
wire [7:0] L; // LDA/AND multiplexer output
reg [7:0] AQ; // A register flip-flops
// Next state variables
reg next_CF, next_VF, next_NF, next_ZF;
reg [7:0] next_AQ;
    
```

```

// Declaration of intermediate equations
// Least significant bit carry in (0 for ADD, 1 for SUB => ALY)
assign CIN = ALY;
// Intermediate equations for adder/subtractor SUM (S) selected when ALX = 0
assign S = AQ ^ (DB_z ^ ALY) ^ {CY[6:0],CIN};
// Ripple carry equations (CY[7] is COUT, DB_z is data from data bus)
assign CY = AQ & (ALY ^ DB_z) | AQ & {CY[6:0],CIN} | ALY & DB_z & {CY[6:0],CIN};
// Intermediate equations for LOAD and AND, selected when ALX = 1
// (ALY)? AND : LDA (select LDA or AND based on ALY)
assign L = ALY ? AQ & DB_z : DB_z;
// Combinational ALU outputs
// (ALX)? L : S (select LDA/AND or ADD/SUB based on ALX)
assign ALU = ALX ? L : S;
    
```

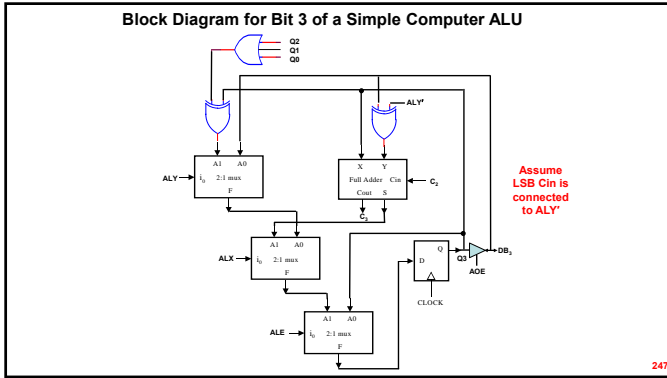
```

// Register bit and data bus control equations
always @(posedge CLK) begin
    AQ <= next_AQ;
end
always @ (AQ, ALE, ALU) begin
    next_AQ = ALE ? ALU : AQ;
end
assign DB_z = AOE ? AQ : 8'bZZZZZZZZ;
// Condition code register state equations
always @(posedge CLK) begin
    CF <= next_CF;
    ZF <= next_ZF;
    NF <= next_NF;
    VF <= next_VF;
end
always @ (CF, NF, ZF, VF, ALE, ALX, ALY, CY) begin
    next_CF = ALE ? (ALX ? CF : (CY[7])) : CF;
    next_ZF = ALE ? (ALU == 0) : ZF;
    next_NF = ALE ? ALU[7] : NF;
    next_VF = ALE ? (ALX ? VF : (CY[7] ^ CY[6])) : VF;
end
endmodule
    
```

AOE	ALE	ALX	ALY	Function	CF	ZF	NF	VF
0	1	0	0	ADD	X	X	X	X
0	1	0	1	SUB	X	X	X	X
0	1	1	0	LDA	.	X	X	.
0	1	1	1	AND	.	X	X	.
1	0	d	d	OUT
0	0	d	d	<none>

X -> flag affected . -> flag not affected

Clicker Quiz



Q1. If the input control combination $AOE=0, ALE=1, ALX=0, ALY=0$ is applied to this circuit, the function performed will be:

A. ADD
B. SUBTRACT
C. LOAD
D. NEGATE
E. none of the above

Assume LSB Cin is connected to ALY*

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Q2. If the input control combination $AOE=0, ALE=1, ALX=1, ALY=0$ is applied to this circuit, the function performed will be:

A. ADD
B. SUBTRACT
C. LOAD
D. NEGATE
E. none of the above

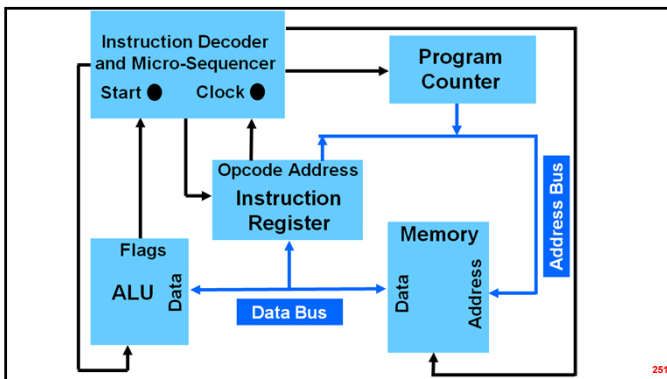
Assume LSB Cin is connected to ALY*

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Simple Computer Block Diagram

- Functional blocks required:
 - a place to store the program, operands, and computation results – **memory**
 - a way to keep track of which instruction is to be executed next – **program counter (PC)**
 - a place to temporarily “stage” an instruction while it is being executed – **instruction register (IR)**
 - a way to perform arithmetic and logic operations – **arithmetic logic unit (ALU)**
 - a way to coordinate and sequence the functions of the machine – **instruction decoder and micro-sequencer (IDMS)**

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Instruction Decoder and Microsequencer

- The **instruction decoder and microsequencer (IDMS)** is a state machine that orchestrates the activity of all the other functional blocks
- There are two basic steps involved in “processing” each instruction of a program (called a **micro-sequence**):
 - **fetching** the instruction from memory (at the location pointed to by the PC), loading it into the IR, and incrementing the PC
 - **executing** the instruction staged in the IR based on the opcode field and the operand address field

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Instruction Decoder and Microsequencer

- Since there are only *two states* (fetch and execute), a single flip-flop can be used to implement the *state counter* ("SQ")
- The control signals that need to be asserted during the *fetch* cycle include:
 - **POA**: turn on PC output buffers
 - **MSL**: select memory
 - **MOE**: turn on memory output buffers
 - **IRL**: enable IR load
 - **PCC**: enable PC count

NOTE: The *synchronous* functions (IRL and PCC) will take place on the clock edge that causes the *state counter* to transition from the **FETCH** state to the **EXECUTE** state

Instruction Decoder and Microsequencer

- The control signals that need to be asserted during an *execute* cycle for the synchronous ALU functions (ADD, SUB, LDA, AND) are:
 - **IRA**: turn on operand address output buffers
 - **MSL**: select memory
 - **MOE**: turn on memory data output buffers
 - **ALE**: enable ALU operation
 - **ALX, ALY**: select ALU function
- The control signals that need to be asserted during an *execute* cycle for STA are:
 - **IRA**: turn on operand address output buffers
 - **MSL**: select memory
 - **MWE**: enable memory write
 - **AOE**: turn on A register output buffers

System Control Signals

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY
S0	–	H	H		H	H	H					
S1	HLT	L		L		L			L			
S1	LDA addr	H	H				H		H	H		
S1	ADD addr	H	H				H		H			
S1	SUB addr	H	H				H		H			
S1	AND addr	H	H				H		H	H		
S1	STA addr	H		H			H	H				

Opcode	Mnemonic	Function Performed	AOE	ALE	ALX	ALY	Function	CF	ZF	NF	VF
0 0 0	HLT	Halt – stop, discontinue execution	0	1	0	0	ADD	X	X	X	X
0 0 1	LDA addr	Load A with contents of location addr	0	1	0	1	SUB	X	X	X	X
0 1 0	ADD addr	Add contents of addr to contents of A	0	1	1	0	IDA	X	X	X	X
0 1 1	SUB addr	Subtract contents of addr from contents of A	0	1	1	1	AND	X	X	X	X
1 0 0	AND addr	AND contents of addr with contents of A	1	0	d	d	OUT	-	-	-	-
1 0 1	STA addr	Store contents of A at location addr	0	0	d	d	<none>	-	-	-	-

X -> flag affected - -> flag not affected

Instruction Decoder and Microsequencer

- In order to *stop* execution (i.e., disable all the functional blocks) when a **HLT** instruction is executed, an additional flip-flop will be used (called "RUN"), as follows:
 - when the **START** pushbutton is pressed, the RUN flip-flop will be *asynchronously set*
 - when a **HLT** instruction is executed, the RUN flip-flop will be *asynchronously cleared*
 - the RUN signal will be **ANDed** with the synchronous system enable signals, thus effectively *halting* execution when a **HLT** instruction is executed

```

/* Instruction Decoder and Microsequencer */
module idms(CLK, START, OP, MSL, MOE, MWE, PCC, POA, ARS, IRL, IRA, ALE, ALX, ALY, AOE);
input wire CLK;
input wire START; // Asynchronous START pushbutton
input wire [2:0] OP; // opcode bits (input from IR5..IR7)
output wire MSL, MOE, MWE; // Memory control signals
output wire PCC, POA, ARS; // PC control signals
output wire IRL, IRA; // IR control signals
output wire ALE, ALX, ALY, AOE; // ALU control signals (without flags)

reg SQ, next_SQ; // State counter
reg RUN, next_RUN; // RUN/HLT state

wire LDA, STA, ADD, SUB, AND, HLT; // Opcode names
wire [1:0] S; // State variables

wire RUN_ar; // Asynchronous reset for RUN
    
```

```

assign HLT = ~OP[2] & ~OP[1] & ~OP[0]; // HLT opcode = 000
assign LDA = ~OP[2] & ~OP[1] & OP[0]; // LDA opcode = 001
assign ADD = ~OP[2] & OP[1] & ~OP[0]; // ADD opcode = 010
assign SUB = ~OP[2] & OP[1] & OP[0]; // SUB opcode = 011
assign AND = OP[2] & ~OP[1] & ~OP[0]; // AND opcode = 100
assign STA = OP[2] & ~OP[1] & OP[0]; // STA opcode = 101

// Decoded state definitions
assign S[0] = ~SQ; // fetch
assign S[1] = SQ; // execute

// State counter
always @ (posedge CLK, posedge START) begin
    if(START == 1'b1) // start in fetch state
        SQ <= 1'b0;
    else // if RUN negated, resets SQ
        SQ <= next_SQ;
end

always @ (SQ, RUN) begin
    next_SQ = RUN & ~SQ;
end

// Run/stop
assign RUN_ar = S[1] & HLT;
always @ (posedge CLK, posedge RUN_ar, posedge START) begin
    if(START == 1'b1) // RUN set to 1 when START asserted
        RUN <= 1'b1;
    else if(RUN_ar == 1'b1) // RUN is cleared when HLT is executed
        RUN <= 1'b0;
end
    
```

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA addr	Load A with contents of location addr
0 1 0	ADD addr	Add contents of addr to contents of A
0 1 1	SUB addr	Subtract contents of addr from contents of A
1 0 0	AND addr	AND contents of addr with contents of A
1 0 1	STA addr	Store contents of A at location addr

A D flip-flop synthesized by an always block will retain its value by default unless otherwise specified

```
// System control equations
assign MSL = RUN & S[0] | S[1] & (LDA | STA | ADD | SUB | AND);
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND);
assign MWE = S[1] & STA;
assign ARS = START;
assign PCC = RUN & S[0];
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND);
assign AOE = S[1] & STA;
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND);
assign ALX = S[1] & (LDA | AND);
assign ALY = S[1] & (SUB | AND);
```

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY
S0	-	H	H									
S1	HLT	L		L	L	L			L			
S1	LDA addr	H	H					H		H	H	
S1	ADD addr	H	H					H		H		
S1	SUB addr	H	H					H		H	H	H
S1	AND addr	H	H					H		H	H	H
S1	STA addr	H		H				H	H			

System Data Flow and Timing Analysis

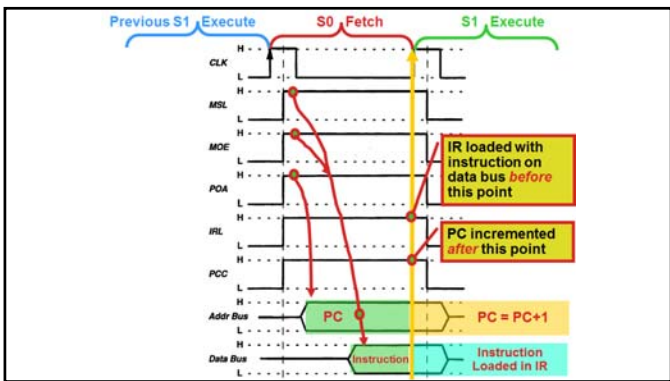
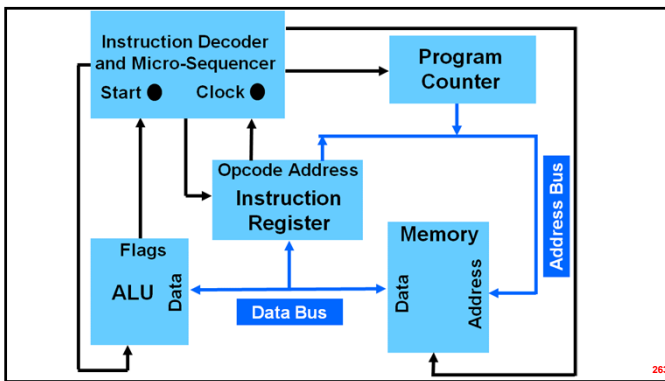
- General procedure
 - Understand operation of individual functional units
 - Memory
 - Program counter
 - Instruction register
 - Arithmetic logic unit
 - Instruction decoder and microsequencer
 - (New functional blocks to be added)

System Data Flow and Timing Analysis

- General procedure
 - Understand function (“data processing”) performed by each instruction
 - Identify address and data flow required to execute each instruction
 - Identify micro-operations required to execute each instruction
 - Identify control signals that need to be asserted to generate the required sequence of micro-operations for each instruction
 - Examine timing relationship of control signals

System Data Flow and Timing Analysis

- Basic hardware-imposed constraints
 - Only **one device** is allowed to drive a bus during any machine cycle (i.e., “bus fighting” must be avoided)
 - Data **cannot** pass through **more than one** (edge-triggered) flip-flop or latch per cycle



Clicker Quiz

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Q1. The increment of the program counter (PC) needs to occur as part of the "fetch" cycle because:

- A. if it occurred on the "execute" cycle, the new value might not be stable in time for the subsequent "fetch" cycle
- B. if it occurred on the "execute" cycle, it would not be possible to execute an "STA" instruction
- C. if it occurred on the "execute" cycle, it would not be possible to read an operand from memory
- D. if it occurred on the "execute" cycle, it would not be possible to read an instruction from memory
- E. none of the above

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Q2. The program counter (PC) can be incremented on the same cycle that its value is used to fetch an instruction from memory because:

- A. the synchronous actions associated with the IRL and PCC control signals occur on different fetch cycle phases
- B. the IRL and PCC control signals are not asserted simultaneously by the IDMS
- C. the load of the instruction register is based on the data bus value prior to the system CLOCK edge, while the increment of the PC occurs after the CLOCK edge
- D. the load of the instruction register occurs on the negative CLOCK edge, while the increment of the PC occurs on the positive CLOCK edge
- E. none of the above

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Q3. Incrementing the program counter (PC) on the same clock edge that loads the instruction register (IR) does not cause a problem because:

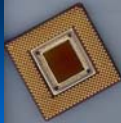
- A. the memory will ignore the new address the PC places on the address bus
- B. the output buffers in the PC will not allow the new PC value to affect the address bus until the next fetch cycle
- C. the IR will be loaded with the value on the data bus prior to the clock edge while the contents of the PC will increment after the clock edge
- D. the value in the PC will change in time for the correct value to be output on the address bus (and fetch the correct instruction), before the IR load occurs
- E. none of the above

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Q4. The hardware constraint that "data cannot pass through more than one edge-triggered flip-flop per clock cycle" is based on the fact that:

- A. only a single entity can drive a bus on a given clock cycle
- B. the system clock has limited driving capability
- C. the flip-flops that comprise a register do not change state simultaneously, so additional time must be provided before the register's output can be used
- D. for a D flip-flop with clocking period Δ , $Q(t+\Delta)=D(t)$
- E. none of the above

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Purdue IM:PACT* Spring 2019 Edition
*Instruction Matters: Purdue Academic Course Transformation

Introduction to Digital System Design

Module 4-J

Simple Computer Basic Extensions

Reading Assignment:
Meyer Supplemental Text, pp. 42-50

Learning Objectives:

- Modify a reference ALU design to perform different functions (e.g., shift and rotate)
- Describe how input/output (IN/OUT) instructions can be added to the base machine architecture
- Describe the operation of the I/O block and the function of its control signals: IOR and IOW
- Compare and contrast the operation of OUT instructions with and without a transparent latch as an integral part of the I/O block
- Compare and contrast “jump” and “branch” transfer-of-control instructions along with the architectural features needed to support them
- Distinguish between conditional and unconditional branches
- Describe the basis for which a conditional branch is “taken” or “not taken”

Outline

- Overview
- Adding shift instructions
- Adding input/output (I/O) instructions
- Adding transfer of control instructions

Overview

- We will use the two available opcodes (110 and 111) to add new instructions to the basic machine, a pair at a time

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	ADD <i>addr</i>	Add contents of <i>addr</i> to contents of A
0 1 1	SUB <i>addr</i>	Subtract contents of <i>addr</i> from contents of A
1 0 0	AND <i>addr</i>	AND contents of <i>addr</i> with contents of A
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>
1 1 0		
1 1 1		

Overview

- We will add **rows** to the system control table to add the new instructions and add **columns** to add new control signals

Decoded State	Instruction Mnemonic	MS	MCE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY		
S0	-	H	H		H	H	H							
S1	HLT	L		L		L								
S1	LDA <i>addr</i>	H	H				H	H	H	H				
S1	ADD <i>addr</i>	H	H					H	H					
S1	SUB <i>addr</i>	H	H					H	H					
S1	AND <i>addr</i>	H	H					H	H	H	H			
S1	STA <i>addr</i>	H		H				H	H					
S1														
S1														

Adding Shift Instructions

- **Definition:** A shift instruction **translates** the bits in a register (here, the “A” register) one place to the **left** or to the **right**
- **Definition:** An **end off** shift discards the bit that gets shifted out
- **Definition:** A **preserving** shift retains the bit shifted out (typically in the CF condition code bit)
- **Definition:** A **logical** shift is a “zero fill” shift
- **Definition:** An **arithmetic** shift is a “sign preserving” shift (i.e., the sign bit gets replicated as the data is shifted right)

Shift Instruction Examples

- **Given:** (A) = 10011010
- After **logical shift left:** 00110100 CF=1
- After **logical shift right:** 01001101 CF=0
- After **arithmetic shift left:** 00110100 CF=1
- After **arithmetic shift right:** 11001101 CF=0

Note: An **arithmetic left shift** is **identical** to a **logical left shift**

Adding Shift Instructions

- Modify the ALU to function as follows:

ALX	ALY	Function Performed
0	0	Load
0	1	Logical Shift Right
1	0	Arithmetic/Logical Shift Left
1	1	Arithmetic Shift Right

The CF condition code bit can be used to preserve the bit that gets shifted out

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Modified Instruction Set

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	LSR	Logically shift contents of A right
0 1 1	ASL	Arithmetically/Logically shift contents of A left
1 0 0	ASR	Arithmetically shift contents of A right
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>
1 1 0		
1 1 1		

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Modified System Control Table

Decoded State	Instruction Mnemonic	MEL	MGE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY				
S0	-	H	H		H	H	H									
S1	HLT	L			L		L				L					
S1	LDA <i>addr</i>	H	H					H		H						
S1	LSR									H		H				
S1	ASL									H		H				
S1	ASR									H		H				
S1	STA <i>addr</i>	H		H				H	H							
S1																
S1																

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```

/* ALU Module Version 2 */
module alu(CLK, ALE, AOE, ALX, ALY, DB_z, CF, VF, NF, ZF);

/* 8-bit, 4-function ALU with bi-directional data bus

LDA: (AQ[7:0]) <- DB_z[7:0]
LSR: (AQ[7:0]) <- 0 AQ7 AQ6 AQ5 AQ4 AQ3 AQ2 AQ1, CF <- AQ0
ASL: (AQ[7:0]) <- AQ6 AQ5 AQ4 AQ3 AQ2 AQ1 AQ0 0, CF <- AQ7
ASR: (AQ[7:0]) <- AQ7 AQ6 AQ5 AQ4 AQ3 AQ2 AQ1, CF <- AQ0
OUT: Value in AQ[7:0] output on data bus DB_z[7:0]

AOE ALE ALX ALY Function CF ZF NF VF
--- --- --- --- ----- -- -- --
0 1 0 0 LDA      * X X *
0 1 0 1 LSR     X X X *
0 1 1 0 ASL     X X X *
0 1 1 1 ASR     X X X *
1 0 d d  OUT    * * * *
0 0 d d <none> * * * *

X -> flag affected * -> flag not affected

Note: If ALE = 0, the state of all register bits should be retained */
    
```

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```

input wire CLK;

// ALU control lines
input wire ALE; // Overall ALU enable
input wire AOE; // Data bus tri-state output enable
input wire ALX, ALY; // Function select

inout wire [7:0] DB_z; // Bidirectional 8-bit data bus

output reg CF, VF, NF, ZF; // Condition code bits (flags)
// Carry, Overflow, Negative, Zero

// Combinational ALU outputs
reg [7:0] ALU;

// Accumulator (A) register
reg [7:0] AQ;

// Next state variables
reg next_CF, next_VF, next_NF, next_ZF;
reg [7:0] next_AQ;
    
```

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```

// Combinational ALU outputs
always @ (ALX, ALY, DB_z) begin
    case ({ALX,ALY})
        2'b00: ALU = DB_z; // LDA
        2'b01: ALU = {1'b0,AQ[7:1]}; // LSR
        2'b10: ALU = {AQ[6:0],1'b0}; // ASL
        2'b11: ALU = {AQ[7],AQ[7:1]}; // ASR
    endcase
end

// Register bit and data bus control equations
always @(posedge CLK) begin
    AQ <= next_AQ;
end

always @ (ALE, ALU, AQ) begin
    next_AQ = ALE ? ALU : AQ;
end

assign DB_z = AOE ? AQ : 8'bZZZZZZZZ;
    
```

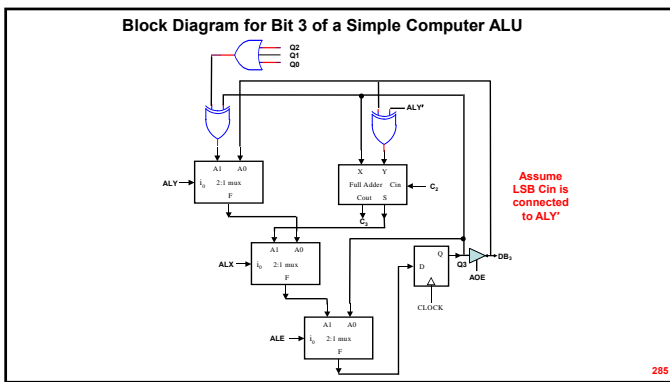
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```

// Flag register state equations
always @ (posedge CLK) begin
    CF <= next_CF;
    ZF <= next_ZF;
    NF <= next_NF;
    VF <= next_VF;
end

always @ (ALE, ALX, ALY, CF, ZF, NF, VF, ALU, AQ) begin
    casez ({ALE,ALX,ALY})
        3'b0?? : next_CF = 1'b0;
        3'b100 : next_CF = CF; // LDA (not affected)
        3'b101 : next_CF = AQ[0]; // LSR
        3'b110 : next_CF = AQ[7]; // ASL
        3'b111 : next_CF = AQ[0]; // ASR
    endcase
    next_ZF = ALE ? (ALU == 0) : ZF;
    next_NF = ALE ? ALU[7] : NF;
    next_VF = VF; // NOTE: NOT AFFECTED
end
endmodule
    
```

Clicker
Quiz



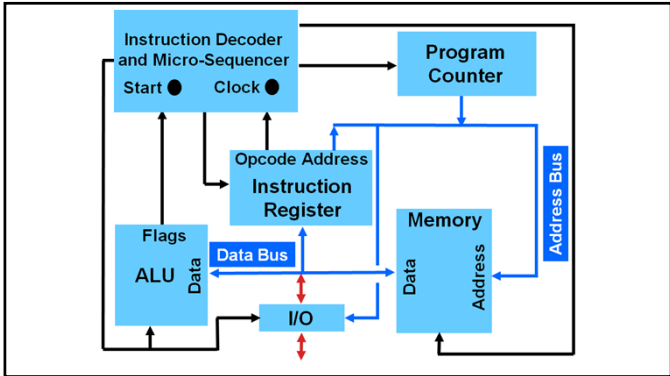
Q1. If the input control combination $AOE=1, ALE=1, ALX=1, ALY=1$ is applied to this circuit, the function (inadvertently) performed on (A) will be equivalent to:

- logical left shift
- logical right shift
- rotate left
- rotate right
- none of the above

Adding I/O Instructions

- When we first drew the “big picture” of our simple computer, we included a switch “input port” and an LED “output port”

● ● ● ● ● ● ● ●
 LED Output Port
● ● ● ● ● ● ● ●
 Switch Input Port
 Start ● Clock ●



Adding I/O Instructions

- Need two new instructions:
 - IN *addr*** – input data from port *addr* and load into the A register
 - OUT *addr*** – output data in A register to port *addr*

Here, the **address field** of the instruction is used to specify a **port address (or, I/O device ID)**

- Also need two new control signals:
 - IOR** – asserted when IN (“I/O read”) occurs
 - IOW** – asserted when OUT (“I/O write”) occurs

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```
/* Input/Output Port 00000 */
```

```
module io(ADRBUS_z, IN, OUT, IOR, IOW, DB_z);

input wire [4:0] ADRBUS_z; // address bus
input wire [7:0] IN; // input port
input wire IOR; // input port read
input wire IOW; // input port write
output wire [7:0] OUT; // output port
inout wire [7:0] DB_z; // bidirectional data bus

wire PS;

// Port select equation for port address 00000
assign PS = (ADRBUS_z == 5'b00000);

assign DB_z = IOR & PS ? IN : 8'bZZZZZZZZ;
assign OUT = IOW & PS ? DB_z : 8'bZZZZZZZZ;

endmodule
```

Issue: Output port bits are valid only as long as IOW&PS is asserted (Hi-Z otherwise)

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```
/* Input/Output Port 00000 - with Output Latch */
```

```
module io(ADRBUS_z, IN, OUT, IOR, IOW, DB_z);

input wire [4:0] ADRBUS_z; // address bus
input wire [7:0] IN; // input port
input wire IOR; // input port read
input wire IOW; // input port write
output reg [7:0] OUT; // output port
inout wire [7:0] DB_z; // bidirectional data bus
wire PS;

// Port select equation for port address 00000
assign PS = (ADRBUS_z == 5'b00000);

assign DB_z = IOR & PS ? IN : 8'bZZZZZZZZ;

// Transparent latch for output port
always @ (IOW, PS, DB_z) begin
    if((IOW & PS) == 1'b1)
        OUT = DB_z;
end

endmodule
```

The if construct without an else creates an **inferred latch**

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Adding I/O Instructions

- Modified system control table:

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY	IOR	IOW
S0	-	H	H		H	H	H							
S1	HLT	L	L		L	L								
S1	LDA <i>addr</i>	H	H					H		H	H			
S1	ADD <i>addr</i>	H	H					H		H		H		
S1	SUB <i>addr</i>	H	H					H		H		H		
S1	AND <i>addr</i>	H	H					H		H		H		
S1	STA <i>addr</i>	H		H				H	H					
S1	IN port									H	H	H	H	
S1	OUT port									H	H			H

- Equations that need to be updated: IRA, AOE, ALE, ALX
- Equations that need to be added: IOR, IOW

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```
// System control equations
assign MSL = RUN & (S[0] | S[1] & (LDA | STA | ADD | SUB | AND));
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND);
assign MWE = S[1] & STA;
assign ARG = START;
assign PCC = RUN & S[0];
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND | IN | OUT);
assign AOE = S[1] & (STA | OUT);
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND | IN);
assign ALX = S[1] & (LDA | AND);
assign ALY = S[1] & (SUB | AND);

assign IOR = S[1] & IN;
assign IOW = S[1] & OUT;

endmodule
```

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY	IOR	IOW
S0	-	H	H		H	H	H							
S1	HLT	L	L		L	L								
S1	LDA <i>addr</i>	H	H					H		H	H			
S1	ADD <i>addr</i>	H	H					H		H		H		
S1	SUB <i>addr</i>	H	H					H		H		H		
S1	AND <i>addr</i>	H	H					H		H		H		
S1	STA <i>addr</i>	H		H				H	H					
S1	IN port									H	H	H	H	
S1	OUT port									H	H			H

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Clicker Quiz

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Q1. If the output port pins are latched, data written to the port will remain on its pins:

- A. only during the execute cycle of the OUT instruction
- B. only when the clock signal is high
- C. until another OUT instruction writes different data to the port
- D. until the next instruction is executed
- E. none of the above

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Q2. If the output port pins are not latched, data written to the port will remain on its pins:

- A. only during the execute cycle of the OUT instruction
- B. only when the clock signal is high
- C. until another OUT instruction writes different data to the port
- D. until the next instruction is executed
- E. none of the above

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Adding Transfer of Control Instructions

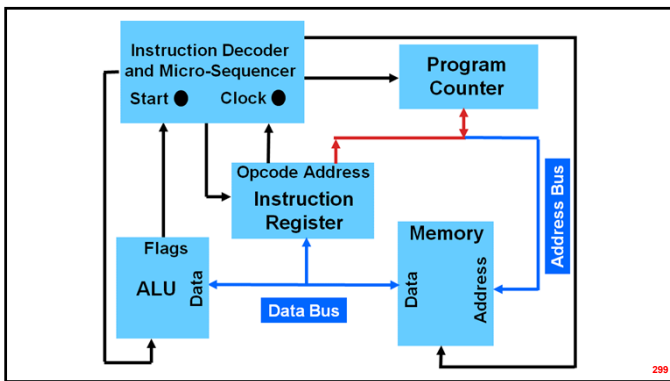
- There are two basic types of **transfer-of-control** instructions:
 - **absolute**: the operand field contains the address in memory at which execution should continue (“**jump**”)
 - **relative**: the operand field contains the signed offset that should be added to the PC to determine the location at which execution should continue (“**branch**”)
- Jumps or branches can be **unconditional** (“always happen”) or **conditional** (“happen only when a specified condition is met” – which is usually a function of the **condition codes**)

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Adding Transfer of Control Instructions

- For the purpose of illustration, we will add an **unconditional jump** (“**JMP**”) instruction to our simple computer along with a single **conditional jump** (“**Jcond**”)
- The conditional jump illustrated will be a **jump if ZF set** (“**JZF**”) instruction
- To execute a jump instruction, the operand field (from the IR) will be loaded into the PC via the **address bus** when **PLA** is asserted
- Note that, for the conditional jump instruction, that if the condition is not met, the execute cycle will be a “**no-operation**” (or, “**NOP**”) cycle

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```

/** Modified Program Counter with Load Capability */
module pc(CLK, PCC, POA, ADDRUS_s, PLA, RST);
    input wire CLK;
    input wire PCC; // PC count enable
    input wire POA; // PC output on address bus tri-state enable
    input wire PLA; // PC load from address bus enable
    input wire RST; // Asynchronous reset (connected to START)

    inout wire [4:0] ADDRUS_s; // address bus

    // NOTE: Assume PCC and PLA are mutually exclusive
    reg [4:0] PC, next_PC;
    assign ADDRUS_s = POA ? PC : 5'b22222;

    always @ (posedge CLK, posedge RST) begin
        if (RST == 1'b1)
            PC <= 5'b00000;
        else
            PC <= next_PC;
        end

    always @ (PCC, PC) begin
        if (PLA == 1'b1) // load
            next_PC = ADDRUS_s;
        else if (PCC == 1'b1) // count up by 1
            next_PC = PC + 1;
        else // retain state
            next_PC = PC;
        end
    endmodule
    
```

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Adding Transfer of Control Instructions

- Modified system control table:

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY	PLA
S0	-	H	H										
S1	HLT	L	H		L	H	L						
S1	LDA addr	H	H					H		H	H		
S1	ADD addr	H	H					H		H	H		
S1	SUB addr	H	H					H		H	H	H	
S1	AND addr	H	H					H		H	H	H	
S1	STA addr	H		H				H	H				
S1	JMP addr							H					H
S1	JZF addr							ZF					ZF

- Equation that needs to be updated: **IRA**
- Equation that needs to be added: **PLA**

```
// System control equations
assign MSL = RUN & (S[0] | S[1] & (LDA | STA | ADD | SUB | AND));
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND);
assign MWE = S[1] & STA;
assign ARS = START;
assign FCC = RUN & S[0];
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND | JMP | JZF&ZP);
assign ALE = S[1] & STA;
assign AOE = RUN & S[1] & (LDA | ADD | SUB | AND);
assign ALX = S[1] & (LDA | AND);
assign ALY = S[1] & (SUB | AND);

assign PLA = S[1] & (JMP | JZF & ZP);
```

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	AOE	ALE	ALX	ALY	PLA
S0	-	H	H										
S1	HLT	L	H		L	H	L						
S1	LDA addr	H	H					H		H	H		
S1	ADD addr	H	H					H		H	H		
S1	SUB addr	H	H					H		H	H	H	
S1	AND addr	H	H					H		H	H	H	
S1	STA addr	H		H				H	H				
S1	JMP addr							H					H
S1	JZF addr							ZF					ZF

Clicker Quiz

Q1. Implementation of "branch" instructions (that perform a *relative* transfer of control) requires the following **modification** to the program counter:

- add a bi-directional path to the data bus
- use the ALU to compute the address of the next instruction
- make it an up/down counter
- add a two's complement N-bit adder circuit (where N is the address bus width)
- none of the above

Q2. Whether or not a conditional branch is *taken* or *not taken* depends on:

- the value of the program counter
- the state of the condition code bits
- the cycle of the state counter
- the value in the accumulator
- none of the above

Thought Questions

- What would be required to add a **jump if less than** ("JLT") or a **jump if greater than or equal to** ("JGE") instruction?

These jump conditions can be determined based on the ALU flags (N, C, Z, V)

A _n	A _{n-1}	(A) _{n-1}	B _n	B _{n-1}	(B) _{n-1}	?	C	Z	N	V
0	0	0	0	0	0	(A) = (B)	1	1	0	0
0	0	0	0	1	+1	(A) < (B)	0	0	1	0
0	0	0	1	0	-2	(A) > (B)	0	0	1	1
0	0	0	1	1	-1	(A) > (B)	0	0	1	1
0	1	+1	0	0	0	(A) > (B)	1	0	0	0
0	1	-1	0	1	+1	(A) = (B)	1	1	0	0
0	1	+1	1	0	-2	(A) > (B)	0	0	1	1
0	1	-1	1	1	-1	(A) > (B)	0	0	1	1
1	0	-2	0	0	0	(A) < (B)	1	0	1	0
1	0	-2	0	1	+1	(A) < (B)	1	0	0	1
1	0	-2	1	0	-2	(A) = (B)	1	1	0	0
1	0	-2	1	1	-1	(A) < (B)	0	0	1	0
1	1	-1	0	0	0	(A) < (B)	1	0	1	0
1	1	-1	0	1	+1	(A) < (B)	1	0	1	0
1	1	-1	1	0	-2	(A) > (B)	1	0	0	0
1	1	-1	1	1	-1	(A) = (B)	1	1	0	0

	C'	C	
0	4	12	8
1	d	d	1
2	d	d	d
3	d	d	d
4	d	d	11
5	d	d	d
6	d	d	10
7	d	d	1

JLT condition
= N' ⊕ V + N ⊕ V'
= N ⊕ V

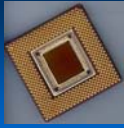
JGE condition
= JLT'
= (N ⊕ V)'

Thought Questions

- How could a **compare** (“CMP”) instruction be implemented? How is this different than a **subtract** (“SUB”)?

A “CMP” works the same as “SUB” **except** that the result of (A) – (addr) is **not stored** in the A register (i.e., **only the flags** are affected)

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Introduction to Digital System Design

Module 4-K Simple Computer Advanced Extensions

Reading Assignment:

Meyer Supplemental Text, pp. 50-64

Learning Objectives:

- describe** the changes needed to the instruction decoder/microsequencer in order to dynamically change the number of instruction execute cycles based on the opcode
- compare and contrast** the machine’s asynchronous reset (“START”) with the synchronous state counter reset (“RST”)
- describe** the operation of a stack mechanism (LIFO queue)
- describe** the operation of the stack pointer (SP) register and the function of its control signals: ARS, SPI, SPD, SPA
- compare and contrast** the two possible stack conventions: SP pointing to the top stack item vs. SP pointing to the top stack item
- describe** how stack manipulation instructions (PSH/POP) can be added to the base machine architecture
- discuss** the consequences of having an unbalanced set of PSH and POP instructions in a given program

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Reading Assignment:

Meyer Supplemental Text, pp. 50-64

Learning Objectives, continued:

- discuss** the reasons for using a stack as a subroutine linkage mechanism: arbitrary nesting of subroutine calls, passing parameters to subroutines, recursion, and reentrancy
- describe** how subroutine linkage instructions (JSR/RTS) can be added to the base machine architecture
- analyze** the effect of changing the stack convention utilized (SP points to top stack item vs. next available location) on instruction cycle counts

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Outline

- Modifications to state counter and instruction decoder to accommodate instructions with multiple execute cycles
- Introduction of a stack mechanism
- Use of a stack to implement “push” (PSH) and “pop” (POP) instructions
- Identification of micro-operations that can be overlapped
- Modifications to the system architecture necessary to implement subroutine linkage instructions
- Implementation of subroutine “call” (JSR) and “return” (RTS) instructions

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State Counter Modifications

- All of the “simple computer” instructions discussed thus far have required **only two** states: a fetch cycle followed by a **single** execute cycle
- Many “real world” instructions require more than a single execute state to achieve their desired functionality
- We wish to extend the state counter (and the instruction decoder) to accommodate instructions that require **multiple** execute cycles (here, up to **three**)

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State Counter Modifications

- In the process of adding this capability, we want to make sure our original “shorter” instructions do not incur a “penalty” (i.e., execute *slower*)
- To accomplish this, we need to design the state counter so that the number of execute cycles can be *dynamically changed* based on the opcode of the instruction being executed
- To provide up to three execute cycles, we will replace the state counter flip-flop with a *two-bit binary counter* that has a *synchronous reset* input (in addition to an asynchronous clear)

State Counter Modifications

- The “state names” will now be:
 - S0 (fetch)
 - S1 (first execute)
 - S2 (second execute)
 - S3 (third execute)
- We will also add a new system control signal “RST” (connected to the synchronous reset of the binary counter) that will be asserted on the *last execute state* of each instruction, thereby *synchronously resetting* the state counter to zero (so that the next cycle will be a “fetch”)

```

/* Instruction Decoder and Microsequencer with Multi-Execution States */
module idmsr(CLK, START, OP, MSL, MOE, MWE, PCC, POA, ARS, IRL, IRA, ALE, ALX, ALY, AOE);

input wire CLK;
input wire START; // Asynchronous START pushbutton
input wire [2:0] OP; // opcode bits (input from IRS..IR7)
output wire MSL, MOE, MWE; // Memory control signals
output wire PCC, POA, ARS; // PC control signals
output wire IRL, IRA; // IR control signals
output wire ALE, ALX, ALY, AOE; // ALU control signals

reg SQA, SQB; // State counter low bit, high bit
reg RUN; // RUN/HLT state
wire RST; // Synchronous state counter reset

wire LDA, STA, ADD, SUB, AND, HLT;
wire [3:0] S;

reg next_SQA, next_SQB;
wire RUN_ar; // Asynchronous reset for RUN
    
```

```

// Decoded opcode definitions
assign HLT = ~OP[2] & ~OP[1] & ~OP[0]; // HLT opcode = 000
assign LDA = ~OP[2] & ~OP[1] & OP[0]; // LDA opcode = 001
assign ADD = ~OP[2] & OP[1] & ~OP[0]; // ADD opcode = 010
assign SUB = ~OP[2] & OP[1] & OP[0]; // SUB opcode = 011
assign AND = OP[2] & ~OP[1] & ~OP[0]; // AND opcode = 100
assign STA = OP[2] & ~OP[1] & OP[0]; // STA opcode = 101

// Decoded state definitions
assign S[0] = ~SQB & ~SQA; // fetch state
assign S[1] = ~SQB & SQA; // first execute state
assign S[2] = SQB & ~SQA; // second execute state
assign S[3] = SQB & SQA; // third execute state

// State counter
always @ (posedge CLK, posedge START) begin
if(START == 1'b1) begin // start in fetch state
SQA <= 1'b0;
SQB <= 1'b0;
end else begin
SQA <= next_SQA;
SQB <= next_SQB;
end
end

always @ (RST, RUN, SQA, SQB) begin
next_SQA = ~RST & RUN & ~SQA; // if RUN negated or RST asserted,
next_SQB = ~RST & RUN & (SQA ^ SQB); // state counter is reset
end
    
```

```

assign RUN_ar = S[1] & HLT;

// Run/stop
always @ (posedge CLK, posedge RUN_ar, posedge START) begin
if(START == 1'b1) // start with RUN set to 1
RUN <= 1'b1;
else if(RUN_ar == 1'b1) // RUN is cleared when HLT is executed
RUN <= 1'b0;
end

// System control equations
assign MSL = RUN & (S[0] | S[1] & (LDA | STA | ADD | SUB | AND));
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND);
assign MWE = S[1] & STA;
assign ARS = START;
assign PCC = RUN & S[0];
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND);
assign AOE = S[1] & STA;
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND);
assign ALX = S[1] & (LDA | AND);
assign ALY = S[1] & (SUB | AND);
assign RST = S[1] & (LDA | STA | ADD | SUB | AND);

endmodule
    
```

Clicker Quiz

Q1. The state counter in the "extended" machine's instruction decoder and micro-sequencer needs both a synchronous reset (RST) and an asynchronous reset (ARS) because:

- A. we want to make sure the state counter gets reset
- B. the ARS signal allows the state counter to be reset to the "fetch" state when START is pressed, while the RST allows the state counter to be reset when the last execute cycle of an instruction is reached
- C. the RST signal allows the state counter to be reset to the "fetch" state when START is pressed, while ARS allows the state counter to be reset when the last execute cycle of an instruction is reached
- D. the state counter is not always clocked
- E. none of the above

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Q2. Adding a **third bit** to the state counter would allow up to ___ execute states:

- A. 3
- B. 5
- C. 7
- D. 8
- E. none of the above

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Stack Mechanism

- **Definition:** A *stack* is a *last-in, first-out* (LIFO) data structure
- Primary uses of stacks in computers:
 - subroutine linkage
 - *saving return address*
 - *parameter passing*
 - saving machine *context* (or *state*) – especially when processing *interrupts* or *exceptions*
 - expression evaluation

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Stack Mechanism

- Conventions:
 - the stack area is generally placed at the "top" of memory (i.e., starting at the *highest address* in memory)
 - a stack pointer (SP) register is used to indicate the address of the *top stack item*
 - stack *growth* is toward *decreasing* addresses (note that this is in contrast to *program growth*, which is toward *increasing* addresses)

Note: An *alternate* convention for the stack could also be used, namely, to have the SP register point to the *next available location*

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Illustration of Stack Growth

- Initial condition (stack empty):

SP Register: 00000

	11100
	11101
	11110
	11111

Addr }
"Top" of Memory

Illustration of Stack Growth

- After first item pushed onto stack:

SP Register: 11111

	11100
	11101
	11110
<item #1>	11111

Addr }
"Top" of Memory

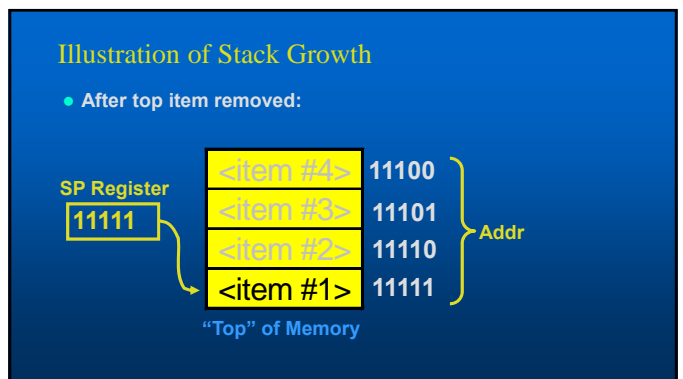
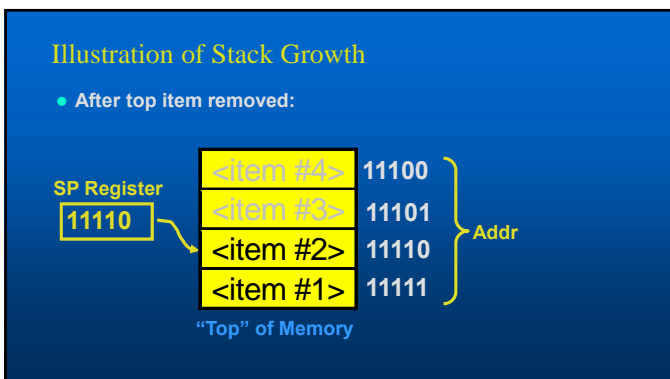
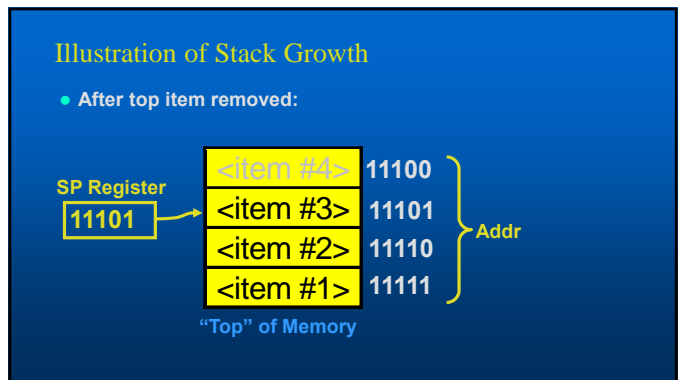
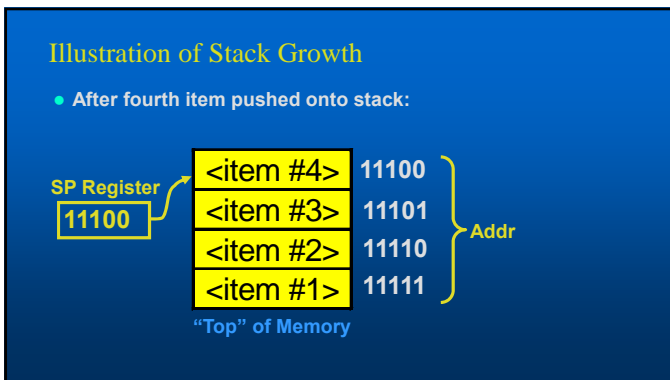
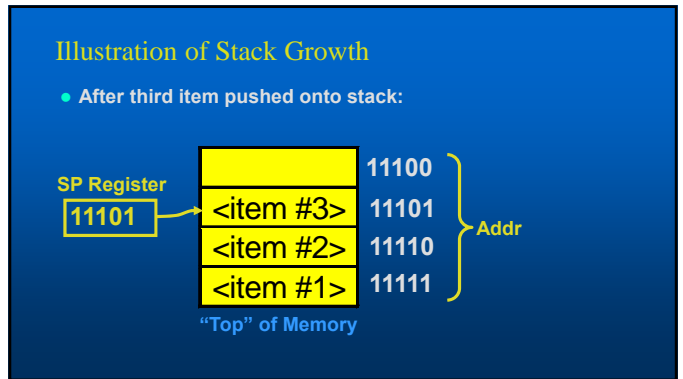
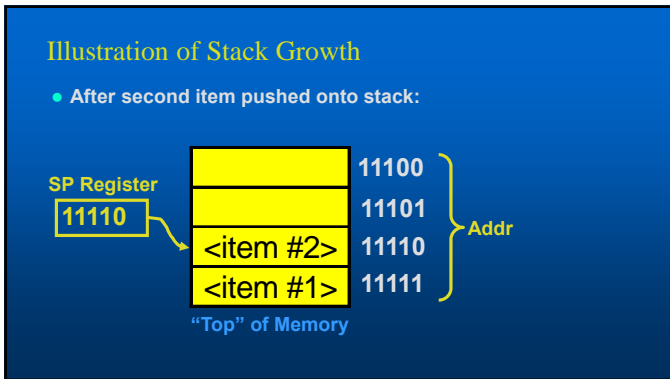


Illustration of Stack Growth

- After top item removed (stack empty):

Stack Mechanism

- To add a stack mechanism to our simple computer, we need a Stack Pointer (SP) register connected to the address bus that has the following control signals:
 - SPI: Stack Pointer Increment
 - SPD: Stack Pointer Decrement
 - SPA: Stack Pointer output on Address bus
 - ARS: Asynchronous ReSet

Note: The *stack empty* condition corresponds to the SP register being cleared to “00000”

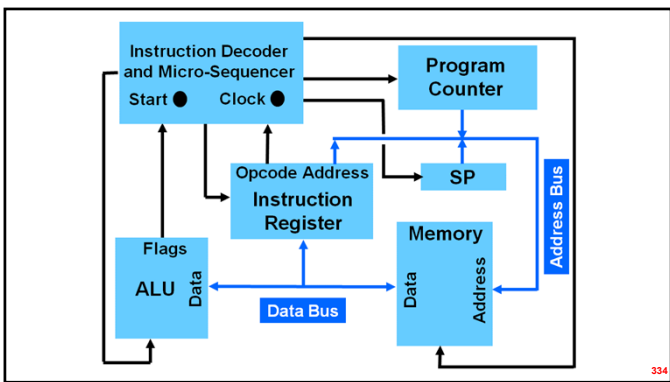
```

/* Stack Pointer */
module sp(CLK, SPI, SPD, SPA, ARS, ADRBUS_n);
// NOTE: Assume SPI and SPD are mutually exclusive
input wire CLK;
input wire SPI, SPD; // SP increment, decrement
input wire SPA; // SP output on address but tri-state enable
input wire ARS; // asynchronous reset (connected to START)
output wire [4:0] ADRBUS_n; // address bus
reg [4:0] SP, next_SP;

assign ADRBUS_n = SPA ? SP : 5'bZZZZZ;

always @ (posedge CLK, posedge ARS) begin
    if (ARS == 1'b1)
        SP <= 5'b00000;
    else
        SP <= next_SP;
end

always @ (SPI, SPD, SP) begin
    if (SPI == 1'b1) // increment
        next_SP = SP + 1;
    else if (SPD == 1'b1) // decrement
        next_SP = SP - 1;
    else // retain state
        next_SP = SP;
end
endmodule
    
```



Adding Stack Manipulation Instructions

- The most common stack operations are “push” and “pop” – here, the value that will be *pushed* and *popped* is the A register
- PSH – save value in A register on stack
 - Step 1: *Decrement SP register*
 - Step 2: Store value in A register at the location pointed to by SP register
- POP – load A with value on stack
 - Step 1: Load A register from memory location pointed to by SP register
 - Step 2: *Increment SP register*

Note: The PSH and POP instructions can be used to implement *expression evaluation*

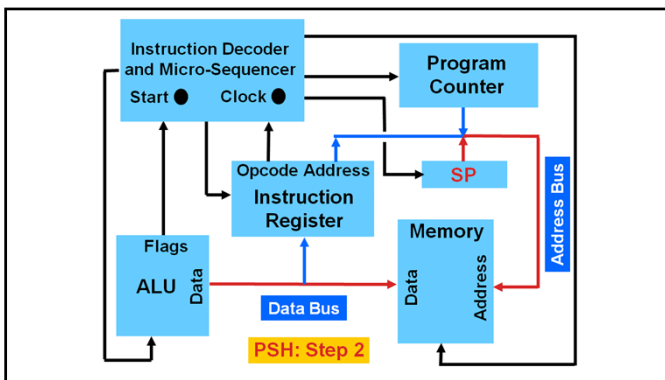
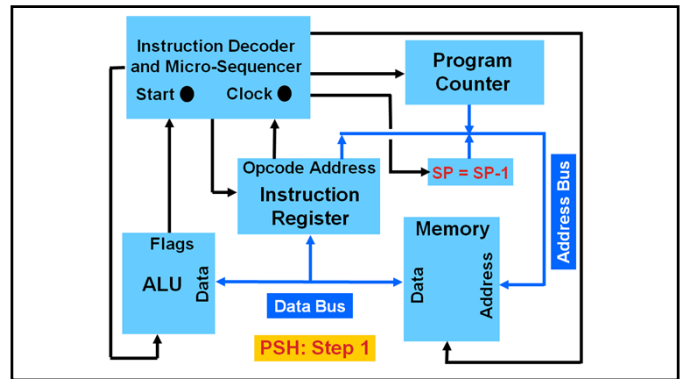
Adding Stack Manipulation Instructions

- The opcodes that will be used for PSH and POP are as follows:

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	ADD <i>addr</i>	Add contents of <i>addr</i> to contents of A
0 1 1	SUB <i>addr</i>	Subtract contents of <i>addr</i> from contents of A
1 0 0	AND <i>addr</i>	AND contents of <i>addr</i> with contents of A
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>
1 1 0	PSH	Save (A) on stack
1 1 1	POP	Restore (A) from stack

Adding Stack Manipulation Instructions

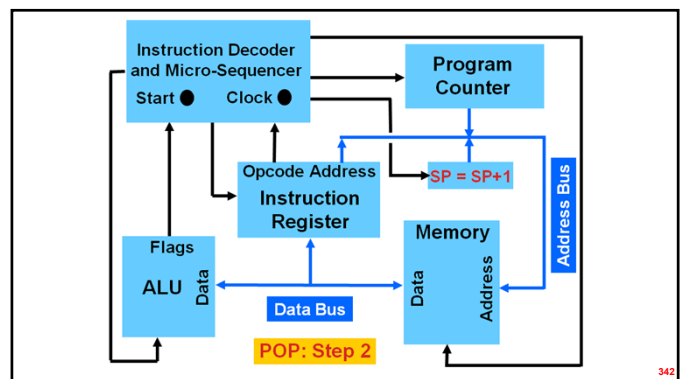
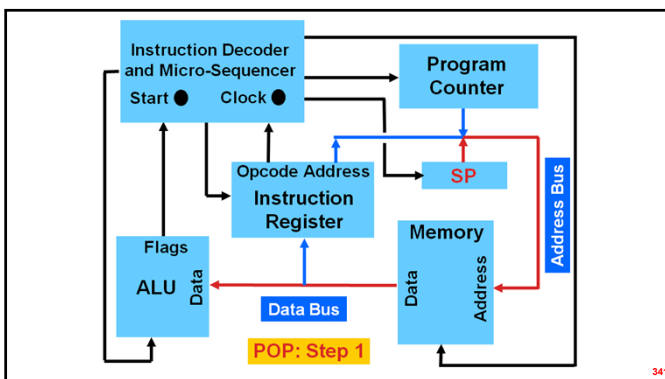
- At first glance, it would appear that **two execute cycles** are required to implement both the PSH and POP instructions
- As **astute computer engineers**, however, we always need to be on the lookout for operations that can be **overlapped** (subject, of course, to the "rules" we learned earlier):
 - Only one device is allowed to drive a bus during any machine cycle (i.e., "bus fighting" must be avoided)
 - Data cannot pass through more than one (edge-triggered) flip-flop or latch per cycle



Adding Stack Manipulation Instructions

- Implementation of PSH requires **two execute cycles**:
 - first execute cycle**: decrement SP register (**SPD**)
 - second execute cycle**: output "new" value of SP on address bus (**SPA**), enable a memory write operation (**MSL** and **MWE**), and tell the ALU to output value in the A register on the data bus (**AOE**)

***Note:** The "new" value of SP must be available (and stable) **before** it can be used to address memory



Adding Stack Manipulation Instructions

- Implementation of POP requires only **one** execute cycle:
 - first execute cycle:** output value of SP on address bus (SPA), enable a memory read operation (MSL and MOE), tell the ALU to load the A register with the value on the data bus (ALE and ALX), and tell the SP register to increment* (SPI)

***Note:** The SP register will be incremented *after* the A register is loaded with the contents of the location pointed to by the SP register, i.e., the SP increment is *overlapped* with the fetch of the next instruction

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Adding Stack Manipulation Instructions

- Modified system control table:

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	IRL	IRA	ADE	ALE	ALX	ALY	SPI	SPD	SPA	RST
S0	-	H	H		H	H	H									
S1	HLT	L		L	L	L	H		L							
S1	LDA addr	H	H					H		H	H					H
S1	ADD addr	H	H					H		H						H
S1	SUB addr	H	H					H		H		H				H
S1	AND addr	H	H					H		H	H	H				H
S1	STA addr	H		H				H	H							H
S1	PSH															H
S1	POP	H	H						H	H	H	H	H			H
S2	PSH	H	H	H												H

Note: Recall that the RST signal is used to *synchronously reset* the state counter on the *final execute cycle* of each instruction

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```
// System control equations
assign MSL = RUN & (S[0] | S[1] & (LDA | STA | ADD | SUB | AND | POP) | S[2] & PSH);
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND);
assign MWE = S[1] & STA | S[2] & PSH;
assign ARS = START;
assign PCC = RUN & S[0];
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND);
assign AOE = S[1] & STA;
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND);
assign ALX = S[1] & (LDA | AND | POP);
assign ALY = S[1] & (SUB | AND);

assign SPI = S[1] & POP;
assign SPD = S[1] & PSH;
assign SPA = S[1] & POP | S[2] & PSH;

assign RST = S[1] & (LDA | STA | ADD | SUB | AND | POP) | S[2] & PSH;
```

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Clicker
Quiz

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Q1. If a program contains **more POP instructions than PSH instructions**, the following is likely to occur:

- stack overflow (stack collides with end of program space)
- stack underflow (stack collides with beginning of program space)
- program counter overflow (program counter wraps to beginning of program space)
- program counter underflow (program counter wraps to end of program space)
- none of the above

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Q2. If a program contains **more PSH instructions than POP instructions**, the following is likely to occur:

- stack overflow (stack collides with end of program space)
- stack underflow (stack collides with beginning of program space)
- program counter overflow (program counter wraps to beginning of program space)
- program counter underflow (program counter wraps to end of program space)
- none of the above

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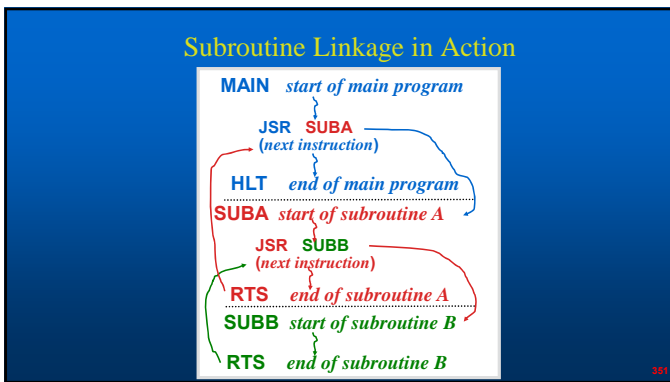
Adding Subroutine Linkage Instructions

- Why use a stack as a subroutine linkage mechanism?
 There are several important capabilities that a stack affords:
 - arbitrary nesting of subroutine calls
 - passing parameters to subroutines
 - recursion (the ability of a subroutine to call itself) – made possible by passing parameters via the stack
 - reentrancy (the ability of a code module to be shared among quasi-simultaneously executing tasks) – made possible by storing temporary local variables on the stack

Adding Subroutine Linkage Instructions

- The opcodes that will be used for JSR (“jump to subroutine”) and RTS (“return from subroutine”) are as follows:

Opcode	Mnemonic	Function Performed
0 0 0	HLT	Halt – stop, discontinue execution
0 0 1	LDA <i>addr</i>	Load A with contents of location <i>addr</i>
0 1 0	ADD <i>addr</i>	Add contents of <i>addr</i> to contents of A
0 1 1	SUB <i>addr</i>	Subtract contents of <i>addr</i> from contents of A
1 0 0	AND <i>addr</i>	AND contents of <i>addr</i> with contents of A
1 0 1	STA <i>addr</i>	Store contents of A at location <i>addr</i>
1 1 0	JSR <i>addr</i>	Jump to subroutine at location <i>addr</i>
1 1 1	RTS	Return from subroutine



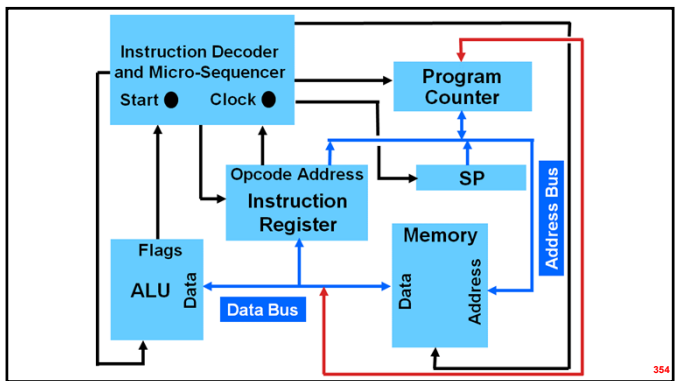
Adding Subroutine Linkage Instructions

- Subroutine “CALL” and “RETURN”
 - JSR *addr* – jump to subroutine at memory location *addr*
 - Step 1: Decrement SP register
 - Step 2: Store return address* at location pointed to by SP register
 - Step 3: Load PC with value in IR address field
 - RTS – return from subroutine
 - Step 1: Load PC from memory location pointed to by SP register
 - Step 2: Increment SP register

*current value in PC, which was incremented during the fetch cycle (points to next instruction)

Adding Subroutine Linkage Instructions

- The astute student will realize at this point that the program counter needs to be modified – a way to save its value on the stack, and subsequently restore it, must be provided
- Two new PC control signals need to be implemented:
 - POD: output value of PC on data bus
 - PLD: load PC with value on data bus



```

/* Program Counter with Data Bus interface */
module pc(CLK, PCC, PLA, POA, RST, ADRBUS_z, DB_z, PLD, POD, PC);

input wire CLK;
input wire PCC; // PC count enable
input wire PLA; // PC load from address bus enable
input wire POA; // PC output on address bus tri-state enable
input wire RST; // Asynchronous reset (connected to START)
input wire PLD; // PC load from data bus enable
input wire POD; // PC output on data bus tri-state enable
inout wire [4:0] ADRBUS_z; // address bus (5-bits wide)
inout wire [7:0] DB_z; // data bus (8-bits wide)
output reg [4:0] PC;

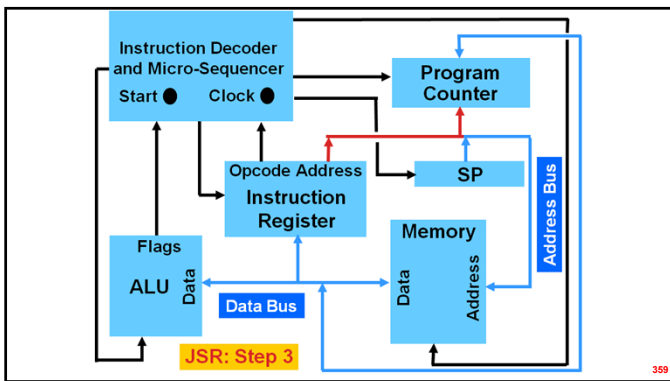
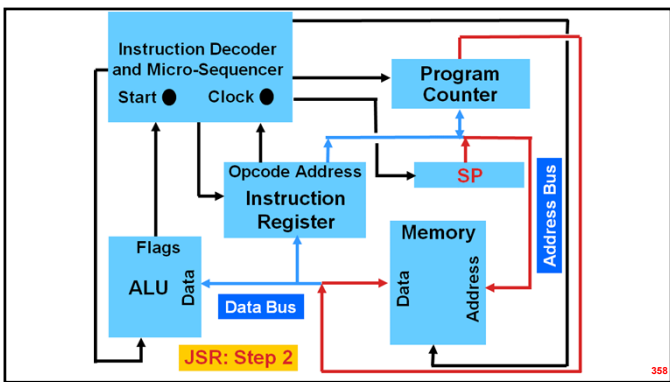
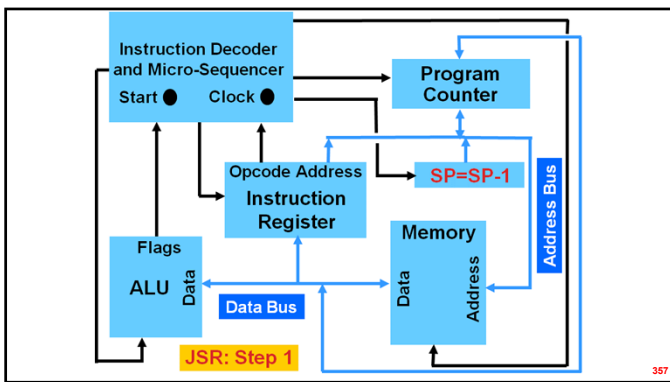
reg [4:0] next_PC;

always @ (posedge CLK, posedge RST) begin
    if (RST == 1'b1)
        PC <= 5'b00000;
    else
        PC <= next_PC;
    end
    
```

```

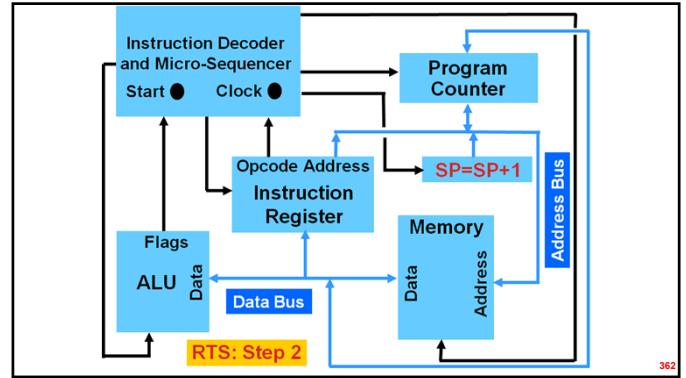
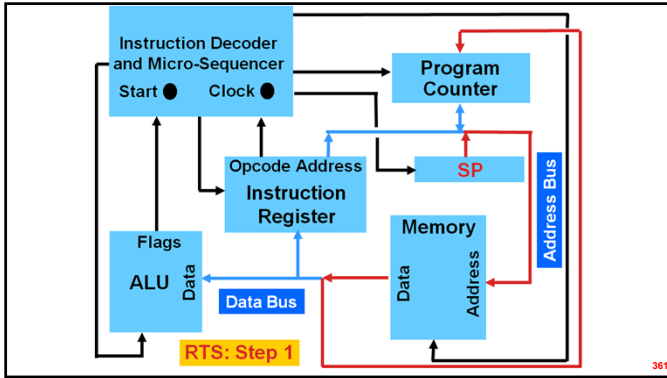
always @ (PLA, PLD, PCC, ADRBUS_z, DB_z, PC) begin
    // synchronous control signals PLA, PLD, and PCC are mutually exclusive
    if (PLA == 1'b1) // load PC from address bus
        next_PC = ADRBUS_z;
    else if (PLD == 1'b1) // load PC from data bus
        next_PC = DB_z;
    else if (PCC == 1'b1) // increment PC
        next_PC = PC + 1;
    else // retain state
        next_PC = PC;
    end

    assign ADRBUS_z = POA ? PC[4:0] : 5'bZZZZZ;
    assign DB_z = POD ? {3'b000, PC[4:0]} : 8'bZZZZZZZZ; // pad upper 3 bits of DB w/ 0
endmodule
    
```



Adding Subroutine Linkage Instructions

- Implementation of JSR requires **three** execute cycles:
 - **first execute cycle:** decrement SP register (**SPD**)
 - **second execute cycle:** output “new” value of SP on address bus (**SPA**), enable a memory write operation (**MSL** and **MWE**), and tell the PC register to output its value on the data bus (**POD**)
 - **third execute cycle:** tell IR register to output its operand field on the address bus (**IRA**), and tell the PC register to load the value on the address bus (**PLA**)



Adding Subroutine Linkage Instructions

- At first glance, it would appear that *two execute cycles* are required to implement the RTS instruction
- As *astute* students, however, we always need to be on the lookout for operations that can be *overlapped* (subject, of course, to the “rules” we learned earlier):
 - Only one device is allowed to drive a bus during any machine cycle (i.e., “bus fighting” must be avoided)
 - Data cannot pass through more than one (edge-triggered) flip-flop or latch per cycle

Adding Subroutine Linkage Instructions

- Implementation of RTS requires only *one* execute cycle:
 - first execute cycle: output value of SP on address bus (SPA), enable a memory read operation (MSL and MOE), tell the PC to load the value on the data bus (PLD), and tell the SP register to increment* (SPI)

***Note:** The SP register will be incremented *after* the PC register is loaded with the contents of the location pointed to by the SP register, i.e., the SP increment is *overlapped* with the fetch of the next instruction

Adding Subroutine Linkage Instructions

Modified system control table:

Decoded State	Instruction Mnemonic	MSL	MOE	MWE	PCC	POA	PLA	POD	IRL	IRA	AOE	ALE	ALX	ALY	SPI	SPD	SPA	RST
S0	-	H	H															
S1	HLT	L			L				L		L							
S1	LDA addr	H	H						H	H	H						H	
S1	ADD addr	H	H						H	H	H						H	
S1	SUB addr	H	H						H	H	H						H	
S1	AND addr	H	H						H	H	H						H	
S1	STA addr	H		H					H	H							H	
S1	JSR addr																H	
S1	RTS	H	H					H								H	H	H
S2	JSR addr	H		H			H										H	
S3	JSR addr					H			H									H

Note: Recall that the RST signal is used to *synchronously reset* the state counter on the *final execute cycle* of each instruction

```
// System control equations
assign MSL = RUN & (S[0] | S[1] & (LDA | STA | ADD | SUB | AND | RTS) | S[2] & JSR);
assign MOE = S[0] | S[1] & (LDA | ADD | SUB | AND | RTS);
assign MWE = S[1] & STA | S[2] & JSR;
assign ARS = START;
assign PCC = RUN & S[0];
assign POA = S[0];

assign PLA = S[3] & JSR;
assign POD = S[2] & JSR;
assign PLD = S[1] & RTS;

assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND);
assign AOE = S[1] & STA;
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND);
assign ALX = S[1] & (LDA | AND);
assign ALY = S[1] & (SUB | AND);

assign SPI = S[1] & RTS;
assign SPD = S[2] & JSR;
assign SPA = S[1] & RTS | S[2] & JSR;

assign RST = S[1] & (LDA | STA | ADD | SUB | AND | RTS) | S[3] & JSR;

endmodule
```

Clicker Quiz

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Q1. If a program contains **more JRS instructions than RTS instructions**, the following is likely to occur:

- A. stack overflow (stack collides with end of program space)
- B. stack underflow (stack collides with beginning of program space)
- C. program counter overflow (program counter wraps to beginning of program space)
- D. program counter underflow (program counter wraps to end of program space)
- E. none of the above

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Q2. If a program contains **more RTS instructions than JSR instructions**, the following is likely to occur:

- A. stack overflow (stack collides with end of program space)
- B. stack underflow (stack collides with beginning of program space)
- C. program counter overflow (program counter wraps to beginning of program space)
- D. program counter underflow (program counter wraps to end of program space)
- E. none of the above

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Fun Things to Think About...

- What kinds of new instructions would be useful in writing “real” programs?
- What new kinds of registers would be good to add to the machine?
- What new kinds of addressing modes would be nice to have?
- What would we have to change if we wanted “branch” transfer-of-control instructions instead of “jump” instructions?

These are all good reasons to “continue your ‘digital life’ beyond this course”!

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