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Little Bits Lab Manual

Spring 2019 Edition

A Series of Lab Experiments and Exercises
for ECE 270
Introduction to Digital System Design
by
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Designed to Accompany the Text
Digital Design Principles and Practices
by
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Preface

The experiments in this *Lab Manual* are based on use of the Purdue "DK-2" Parts Kit, which consists of the following components:

Qty	*Description*	*Qty*	*Description*
1	74HC00 DIP quad 2-input NAND	1	10KΩ potentiometer
1	74HC02 DIP quad 2-input NOR	10	150Ω ¼ watt resistor
1	74HC04 DIP hex Inverter	10	1KΩ ¼ watt resistor
1	74HC08 DIP quad 2-input AND	1	10KΩ X 9 SIP
1	74HC10 DIP triple 3-input AND	1	20 MHz oscillator module
1	74HC14 DIP hex Schmitt-trigger Inverter	1	common-anode 7-segment red LED display
1	74HC74 DIP dual edge-trig D flip-flop	2	S.P.D.T. pushbutton switch
1	74HC86 DIP quad 2-input XOR (CMOS)	1	S.P.S.T. X 8 DIP switch
1	74HC03 DIP quad O.D. 2-input NAND	10	RED resistor LED
1	GAL22V10 electronically-erasable PLD	2	GREEN non-resistor LED
		2	YELLOW non-resistor LED

In addition to the components listed above, a small breadboard (approximately 2.5" X 6.5"), a regulated 5-volt DC power supply, and a wire kit is required along with some basic tools: nominally, a small screwdriver, a wire stripper, and needle-nose pliers.

All items are available on-line at http://www.elexp.com/pur_ece270_362.htm.

Learning Outcome: ***an ability to realize, test, and debug practical digital circuits***

Learning Objectives:

5-1. draw a logic circuit schematic using computer-aided design software (OrCAD)
5-2. construct a circuit consisting of discrete CMOS logic gates (NOT, NAND, NOR, XOR) and verify its operation
5-3. measure the output voltage swing (V_{OL}-V_{OH}) of a logic gate
5-4. measure the input voltage thresholds (V_{IL}-V_{IH}) of a logic gate
5-5. measure the input voltage thresholds (V_{IL}-V_{IH}) of a Schmitt trigger and compare them to the switching threshold of a standard CMOS gate
5-6. test the response of a logic gate to a "floating" input
5-7. measure the output current sourcing (I_{OH}) and sinking (I_{OL}) capability of a logic gate
5-8. measure the rise and fall propagation delays (t_{PLH} and t_{PHL}) of a logic gate
5-9. measure the rise and fall transition times (t_{TLH} and t_{THL}) of a logic gate
5-10. construct a clock generation circuit and measure its frequency of operation
5-11. verify the existence of a logic hazard in a combinational circuit and modify the circuit to eliminate it
5-12. create a hardware description language (Verilog) program that realizes a prescribed logic function (digital system) and test it on a programmable logic platform
5-13. diagnose and correct logic errors in a hardware description language (HDL) program