ECE 270 Lab Verification / Evaluation Form

Experiment 7

Evaluation:

IMPORTANT! You must complete this experiment during your scheduled lab period. All work for this experiment must be demonstrated to and verified by your lab instructor *before the end* of your scheduled lab period.

STEP	DESCRIPTION	MAX	SCORE
Pre-Lab 1	Build Circuit on Breadboard	4	
Pre-Lab 2	Calculate Current/Power Dissipation	2	
Step 1	Test and Verify Circuit	2	
Step 2	Create Verilog Module for Alphanumeric Display	6	
Step 3	Measure Voltages and Currents Using DMM	3	
Step 4	Create Verilog Module to implement "Dorm Alarm"	6	
Step 5	Thought Questions	2	
	TOTAL	25	

Signature of Evaluator: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. ***You will not receive credit for this lab experiment unless this statement is signed in the presence of your lab instructor.***

"In signing this statement, I hereby certify that the work on this experiment is my own and that I have not copied the work of any other student (past or present) while completing this experiment. I understand that if I fail to honor this agreement, I will receive a score of ZERO for this experiment and be subject to possible disciplinary action."

Last Name (Printed): _____ **Lab Div:** _____ **Date:** _____

E-mail: _ _ _ _ _ _ _ _ _ _ **@**purdue.edu **Signature:** _____

7-Segment Display PLD Exercises

Instructional Objectives:

- To review how to create a Verilog Module that specifies the design of a combinational logic circuit for implementation on a programmable logic device (PLD)
- To review how to use ispLEVER™ to synthesize a Verilog module and "fit" the design into a specific PLD and how to use a Universal Programmer to "burn" a fuse map (JEDEC file) produced by a compiler into a PLD

Pre-lab Preparation:

- Read this document in its entirety
- Review the ATF22V10C data sheets (available the course web site under References)
- Complete the **Pre-lab Steps**

Lecture/Demonstration:

Your lab instructor will give a brief presentation that includes the following:

- A review of how to program a PLD using the Universal Programmer
- A demonstration of the completed experiment

Experiment Description:

For this experiment you will use the 7-segment LED in your parts kit in conjunction with your GAL22V10C (ATF22V10C) to realize two different functions. The first function that will be realized is an alphanumeric decoder. The second function realized will be a "dorm room" alarm featuring prioritized sensors. The display device will be a *common anode* 7-segment LED, illustrated in Figure 1. (*Common anode* means that the LED anodes are all tied together, and the LED cathodes are available individually – this means that current must be *sunk* by the PLD for each LED segment.) The active low PLD outputs will be connected, via 150 ohm (brown-green-brown) current limiting resistors, to the individual LED cathodes, and the *common anode* pins of the 7-segment display will be connected to +5 VDC.

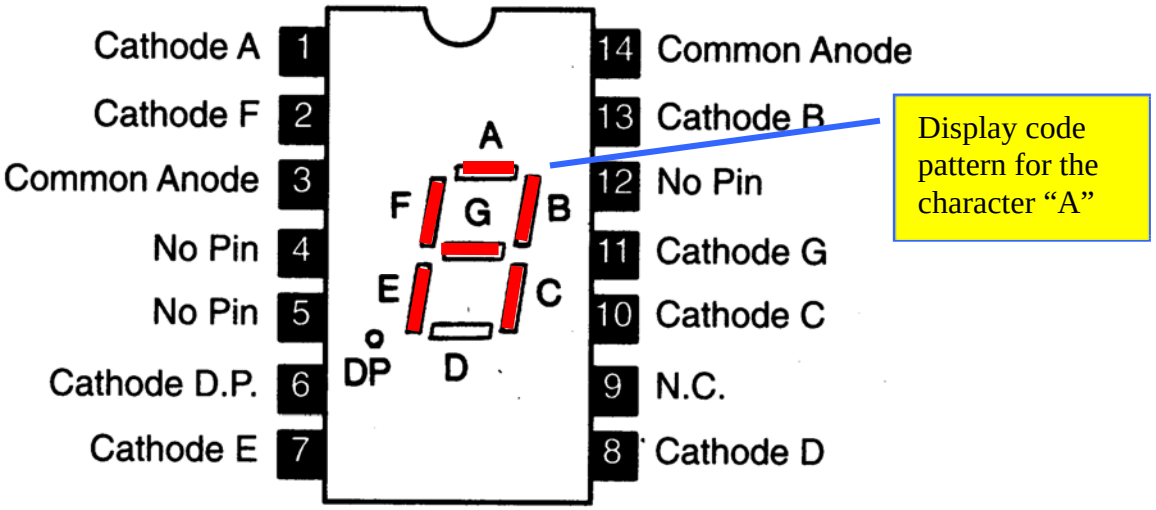
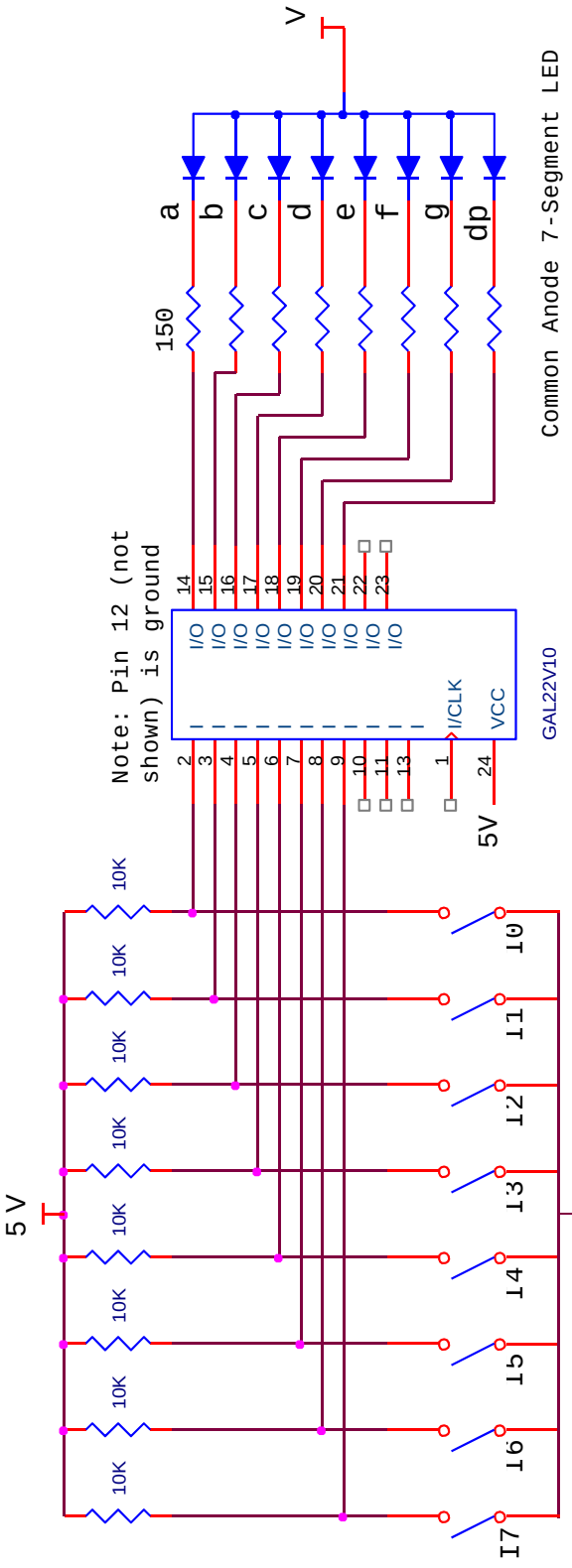
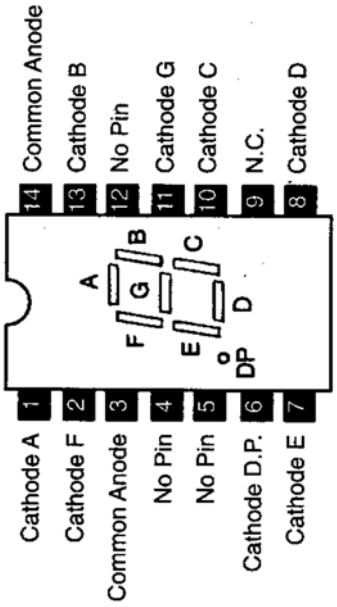


Figure 1. Common Anode 7-Segment LED Pinout.

Pre-lab Step (1):

Build the following circuit using your DIP switch, 7-segment common anode LED, and ATF22V10C, leaving ample room around the PLD to easily remove it from the breadboard for reprogramming. Use a 150 Ω resistor in series with each LED segment.





Pre-lab Step (2):

Given that each LED segment exhibits a forward voltage drop (V_{LED}) of approximately 2.0 volts, that a 150 ohm current limiting resistor is being used, and that the V_{OL} of an ATF22V10C output pin is at most 0.5 volts (at an I_{OL} of 16 mA – see data sheets available on the course web site), calculate I_{LED} (the amount of current that flows through each LED segment, which is also the amount of current sunk by each ATF22V10C output pin). Also, calculate the amount of power dissipated by each LED current limiting resistor.

Show calculations:

Experiment Step (1):

Write a Verilog module that routes the data read from the DIP switch to the corresponding LED segment (`I0` to LED segment `a`, `I1` to LED segment `b`, etc.). Note that the LED segment outputs should be ***active low***. Synthesize your Verilog description using ispLEVER™, targeting it for a **GAL22V10C** device, and use the Universal Programmer at your lab station to "burn" your design (JEDEC file) into your ATF22V10C PLD. Test and verify the operation of your circuit, and demonstrate it to your lab instructor.

CAUTION: Be sure to select the correct ***part number*** (e.g., **ATF22V10C-25**) on the Universal Programmer. (The suffix tells the programmer which algorithm to use; choosing the wrong algorithm can ***permanently damage*** your PLD.)

Experiment Step (2):

Create a second Verilog module to realize an alphanumeric decoder that functions as follows:

(a) If the mode selector `I7`=0, the decoder should function as an **alphabetic display decoder** for all the (non-BCD) alphabetic characters that can be *meaningfully* displayed, i.e., `A, b, C, d, E, F, g, H, J, L, n, o, P, r, U, y` (*note case*) should be displayed in response to 4-bit input codes `0000` – `1111`, respectively.

(b) If the mode selector `I7`=1, the decoder should function as a **hexadecimal display decoder**, i.e., the alphanumeric characters `0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, b, C, d, E, F` (*note case*) should be displayed in response to 4-bit input codes `0000` – `1111`, respectively.

The mode control signal `I7` and the 4-bit code (`I3,I2,I1,I0`) will be input using the DIP switch. Visually indicate the mode of operation on the "DP" LED segment (off = alphabetic mode, on = hexadecimal mode). Synthesize your Verilog module using ispLEVER™, targeting it for a **GAL22V10C** device, and use the Universal Programmer at your lab station to "burn" your design (JEDEC file) into your ATF22V10C PLD. Test and verify the operation of your circuit, and demonstrate it to your lab instructor.

Experiment Step (3):

Once your alphabetic character display circuit is working, measure the LED forward voltage and forward current (any active LED segment can be used). Also, measure the actual V_{OL} obtained from one of the PLD output pins while driving an LED segment.

V_{LED} =_____volts I_{LED} =_____mA V_{OL} =_____volts

Experiment Step (4):

Create a third Verilog module that realizes a "Dorm Room" alarm system that has 7 (sensor) inputs and an "Arm" switch. The 7-segment LED will be used to indicate the alarm status. If the alarm is *not armed*, the 7-segment LED should display an upper-case "U" (for "unarmed"). If the alarm is *armed*, but *none* of the sensors has been tripped, the 7-segment LED should display an upper-case "A" (for "Armed"). If one or more of the sensors has been tripped, the 7-segment LED should indicate the number (1 – 7) of the *highest numbered* sensor that has been tripped. The seven sensors will be "simulated" using DIP switches `I1` through `I7`; DIP switch `I0` will be used to provide the "Arm" input signal.

Synthesize your Verilog module using ispLEVER™, targeting it for a **GAL22V10C** device, and use the Universal Programmer at your lab station to "burn" your design (JEDEC file) into your ATF22V10C PLD. Test and verify the operation of your circuit, and demonstrate it to your lab instructor.

Experiment Step (5):

Place your answers to the following "thought questions" in the space provided below:

(a) Based on the DC characteristics of the ATF22V10C listed in the data sheets, as well as what you learned in Module 1 of the course, which type of 7-segment display would be preferable to use with this PLD: a *common anode* display or a *common cathode* display? Explain why.

_____

_____

_____

(b) How many LED segments would be needed to *meaningfully* display some of the key "missing characters" (i.e., K, M, T, V, W, X, and Z)? Draw a picture of your proposed display device to illustrate your answer.

Number of segments required: _____ Illustration: