ECE 270 Lab Verification / Evaluation Form

Experiment 5

Evaluation:

IMPORTANT! You must complete this experiment during your scheduled lab period. All work for this experiment must be demonstrated to and verified by your lab instructor *before the end* of your scheduled lab period.

STEP	DESCRIPTION	MAX	SCORE
Pre-Lab 1	Schematic	2	
Pre-Lab 2	Timing Diagram	3	
1	Truth Table	2	
2	Observing a Glitch Using the Oscilloscope	5	
3	Resolving the Glitch with a Consensus Term	5	
4	Observing a Glitch Using the Oscilloscope	5	
5	Thought Questions	3	
	TOTAL	25	

Signature of Evaluator: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. *You will not receive credit for this lab experiment unless this statement is signed in the presence of your lab instructor.*

"In signing this statement, I hereby certify that the work on this experiment is my own and that I have not copied the work of any other student (past or present) while completing this experiment. I understand that if I fail to honor this agreement, I will receive a score of ZERO for this experiment and be subject to possible disciplinary action."

Last Name (Printed): _____ **Lab Div:** _____ **Date:** _____

E-mail: __ __ __ __ __ __ __ __ **@**purdue.edu **Signature:** _____

Investigation of Timing Hazards

Instructional Objectives:

- To learn what causes timing hazards in combinational logic circuits, how hazards due to single input changes can be eliminated, and what happens if more than one input is allowed to change simultaneously
- To review how to implement a simple logic function using discrete CMOS ICs

Pre-lab Preparation:

- Read this document in its entirety
- Read pp. 224-229 in *Digital Design Principles and Practices (DDPP)*
- Complete the **Pre-lab Steps**

Lecture/Demonstration:

Your lab instructor will give a brief presentation that includes the following:

- An overview of timing hazards and their cause
- A demonstration of how to capture the oscilloscope display and obtain a printed copy
- A demonstration of the completed experiment

Pre-lab Step (1):

Using OrCAD Capture, draw a complete schematic for the **2:1 multiplexer** depicted in Figure 3-26 (*DDPP 5th Ed.*, p. 123) or Figure 4-38 (*DDPP 4th Ed.*, p. 225), shown below. Note that a **2:1 multiplexer** is basically an electronically-controlled "selector switch" that routes either the "X" input or the "Y" input to the output (F) based on the "select line" signal (Z). Your circuit realization should based on a circuit realization consisting only of a 74HC00 (quad 2-input NAND, designated "U1") and a 74HC10 (triple 3-input NAND, designated "U2"). Be sure to label all inputs and outputs, and include the DIP switches, pull-up SIP, and LEDs. Have a printed copy of your schematic available for your lab instructor to check.

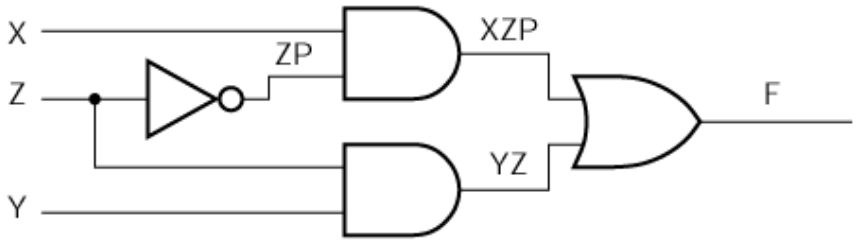
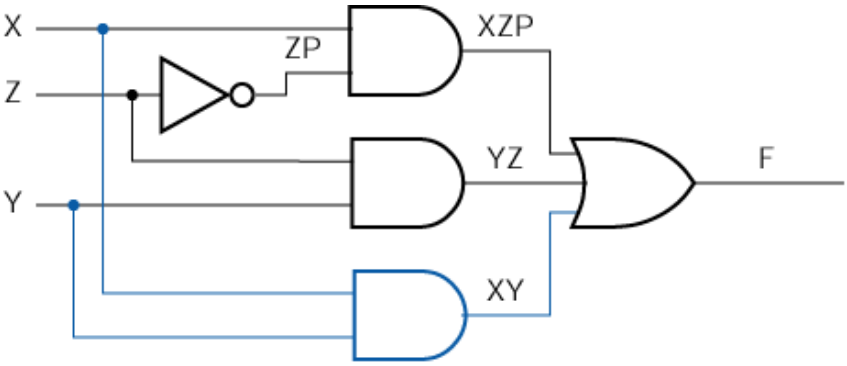
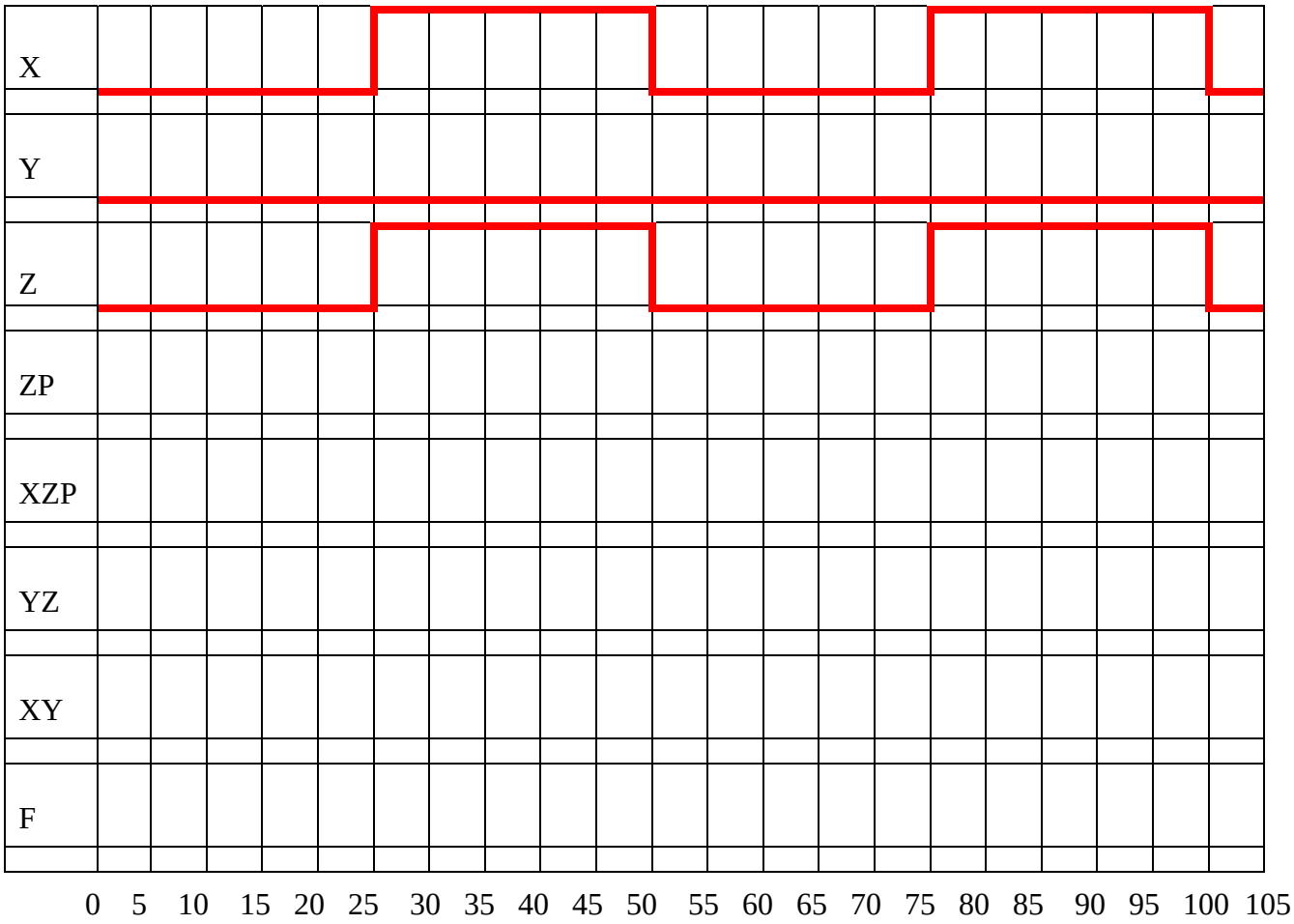


Figure 3-26 from *DDPP 5th Ed*.

Pre-lab Step (2):

Sketch a timing diagram, similar to that depicted in Figure 3-26 (*DDPP 5th Ed.*, p. 123) or Figure 4-38 (*DDPP 4th Ed.*, p. 225), for the input configuration described in **Experiment Step (4).** For the purpose of analysis, assume each gate has a t_{PLH} and a t_{PHL} of 5 ns. **Note:** Each "tick" on the grid below corresponds to 5 ns. Have the completed chart available for your lab instructor to check.





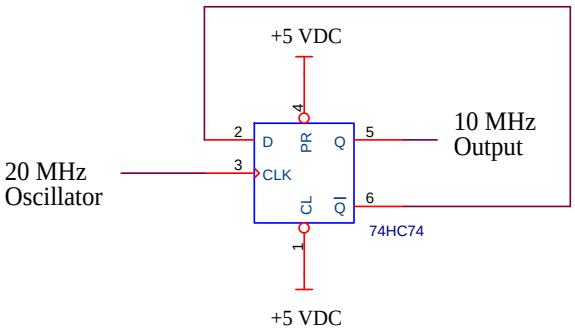
Experiment Step (1):

Implement the circuit drawn for Pre-lab Step (1), and verify that it functions as anticipated. Document the operation of your circuit by completing the following truth table.

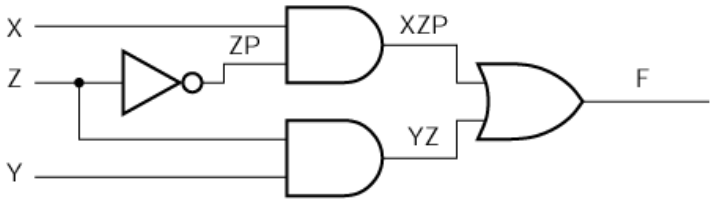
X	Y	Z	F(X,Y,Z)
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

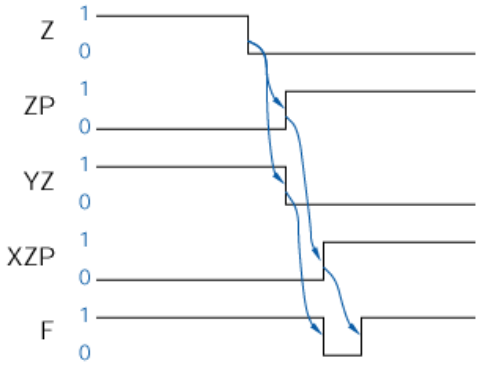
Experiment Step (2):

After verifying the basic multiplexer functionality, connect the input labeled "Z" (the multiplexer select line) to the frequency divider circuit shown below, and set inputs X and Y to logic "1". Display the 10 MHz output of the frequency divider on Channel 1 of the oscilloscope, and display the multiplexer output (F) on Channel 2 of the oscilloscope. Verify the existence of a static-1 hazard (i.e., a momentary "glitch" of the output to logic "0" when the multiplexer switches inputs). Capture the display using the PC at your workstation, print it, and have it available for your lab instructor to check.



NOTE: Also, be sure to connect pin 7 of the 74HC74 to GROUND and pin 14 to POWER (+5 VDC).

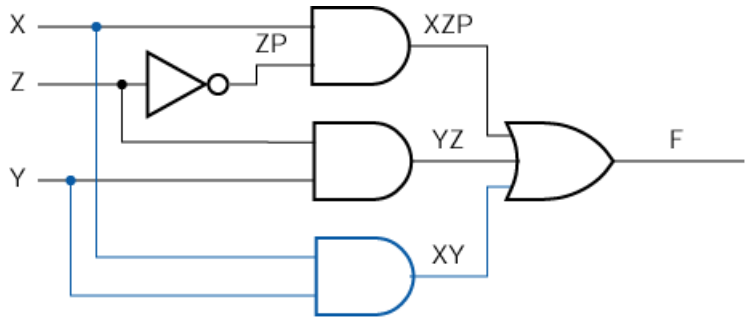




NOTE: If a glitch is not observed, use *three* inverters in place of the *single* inverter shown. Recall that an inverter can be implemented using a NAND gate by simply tying all of its inputs together.

Experiment Step (3):

Modify the circuit to include the consensus term depicted in Figure 4-41 (page 227) of *DDPP*. Connect the input labeled "Z" (the multiplexer select line) to the 10 MHz frequency divider and set inputs X and Y to logic "1". Display the output of the frequency divider on Channel 1 of the oscilloscope, and display the multiplexer output (F) on Channel 2 of the oscilloscope. Verify that the static-1 hazard observed in Step (2) is eliminated. Capture the display using the PC at your workstation, print it, and have it available for your lab instructor to check.



Experiment Step (4):

Using the circuit of Step (3), set input Y to logic "0" and connect inputs X and Z to the 10 MHz frequency divider. Display the output of the frequency divider on Channel 1 of the oscilloscope, and display the multiplexer output (F) on Channel 2 of the oscilloscope. Capture the display using the PC at your workstation, print it, and have it available for your lab instructor to check.

Experiment Step (5):

Place your answers to the following "thought questions" in the space provided below:

(a) Describe what a multiplexer *is* and what it *does* – in your *own words.*

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_____

(b) How "wide" was the glitch observed in Step (2)? Does this agree with what you might expect based on measurements you made in Lab Experiment 2?

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(c) What happened in Step (4) and why? What would you call the waveform observed?

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