ECE 270 Lab Verification / Evaluation Form

Experiment 4

Evaluation:

IMPORTANT! You must complete this experiment during your scheduled lab period. All work for this experiment must be demonstrated to and verified by your lab instructor *before the end* of your scheduled lab period.

STEP	DESCRIPTION	MAX	SCORE
Pre-lab	Rmin and Rmax Calculations	3	
1	Circuit Construction and Function Verification	4	
2	Measuring Static (DC) Characteristics Based on Rmin	4	
3	Measuring Static (DC) Characteristics Based on Rmax	4	
4	Circuit Modification for Timing Measurements	1	
5	Measuring Dynamic (AC) Characteristics Based on Rmin	2	
6	Measuring Dynamic (AC) Characteristics Based on Rmax	2	
7	Thought Questions	5	
	TOTAL	25	

Signature of Evaluator: _____

Academic Honesty Statement:

IMPORTANT! Please carefully read and sign the Academic Honesty Statement, below. *You will not receive credit for this lab experiment unless this statement is signed in the presence of your lab instructor.*

"In signing this statement, I hereby certify that the work on this experiment is my own and that I have not copied the work of any other student (past or present) while completing this experiment. I understand that if I fail to honor this agreement, I will receive a score of ZERO for this experiment and be subject to possible disciplinary action."

Last Name (Printed): _____ **Lab Div:** _____ **Date:** _____

E-mail: __ __ __ __ __ __ __ __ @purdue.edu **Signature:** _____

Investigation of Open-Drain Gate Characteristics

Instructional Objectives:

- To better understand open-drain gate static and dynamic behavior
- To effectively choose the proper value of pull-up resistor for an open-drain circuit

Prelab Preparation:

- Read this document in its entirety
- Review the material referenced in Module 1-J
- Complete the pre-lab calculations
- **Construct the circuit on your breadboard prior to your scheduled lab period**

Lecture/Demonstration:

Your lab instructor will give a brief presentation that includes the following:

- A review of voltage and current measurement techniques
- A review of transition time and propagation delay measurement techniques

Experiment Description:

So-called "open-drain" gates – like the quad 2-input open-drain NAND chip (74HC03) included in your DK-2 kit – differ from "regular" gates in that they only contain N-channel ("pull down") transistors. Recall that a normal CMOS gate uses a P-channel MOSFET as an "active pull-up" to source current in the high state. An open-drain gate, having no such P-channel device, has to rely on an *external* pull-up resistor ("passive pull-up") in order to produce a logic high voltage. The "side-effects" of replacing an active pull-up with an external resistor are not immediately obvious, nor is the proper choice of pull-up resistor value.

In this experiment you will investigate the characteristics of open-drain gates and practice utilizing information provided in a device data sheet. In particular, you will examine the tradeoffs between use of the "minimum" and "maximum" values of pull-up resistors allowable, as well as review how to calculate these values. You will see "first hand" how choice of pull-up resistor affects the static (DC) and dynamic (AC) performance of an open-drain circuit.

Pre-lab Step: Rmin and Rmax Calculations

Access the 74HC03 device data sheet posted under Reference Documents → IC Data Sheets on the course web site to answer the following questions. Use the values listed for the SN74HC03 when operated at a supply voltage of Vcc = 4.5 V.

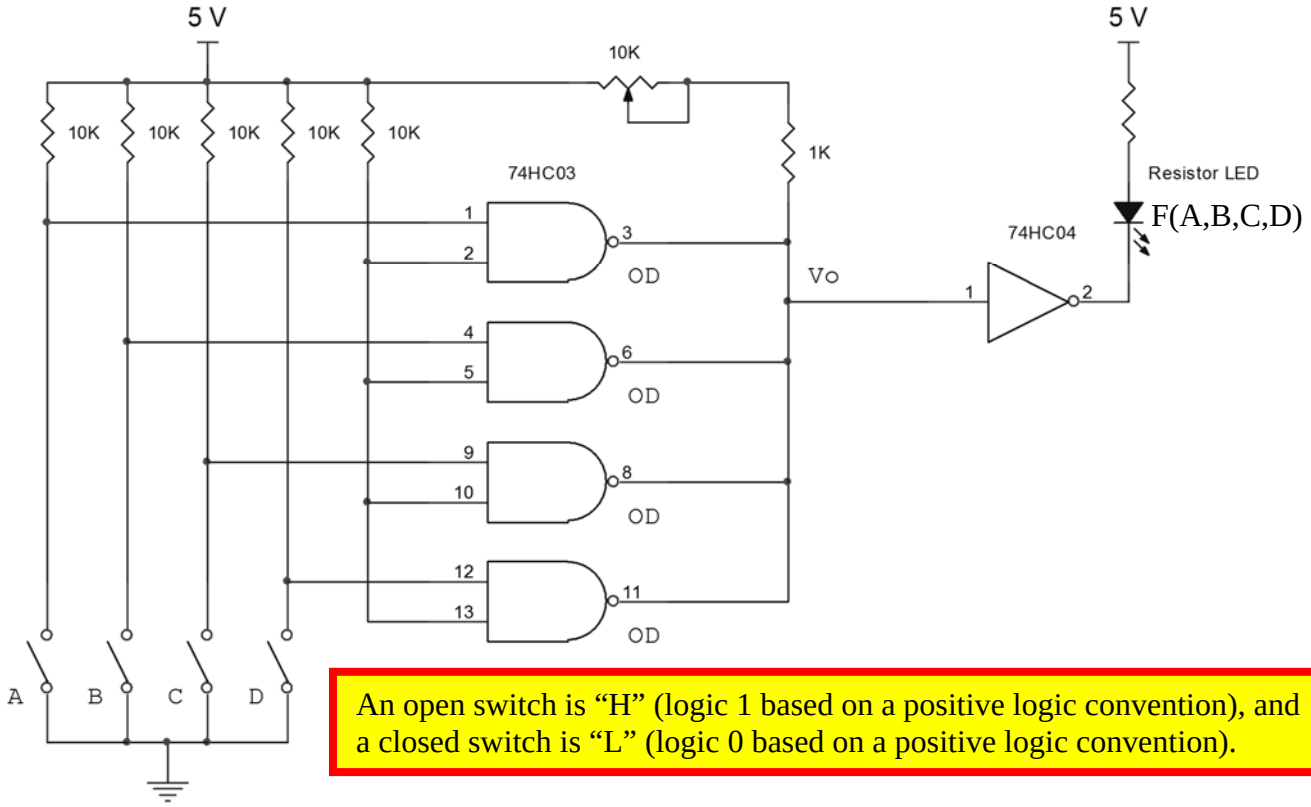
1. Calculate the "on" resistance (when the open-drain output is pulled low) based on the V_{OLmax} specified @ I_{OLmax} = 4 mA for the SN74HC03 when operated at Vcc = 4.5 V. *Show work.*

2. Based on a desired V_{IHmin} = 4.77V @ I_{IH} = 1 μA, calculate the maximum value pull-up resistor (Rmax) as outlined on page 33 of the Module 1 Lecture Summary notes (for four O.D. gates, per the circuit shown in Experiment Step 1). *Show work.*

3. Based on the "worst-case" scenario outlined on page 33 of the Module 1 Lecture Summary notes and the values for the SN74HC03 noted in question 1, above, calculate Rmin. *Show work*

Step (1): Circuit Construction and Function Verification

Construct the circuit illustrated below and set the potentiometer approximately mid-position. Complete the truth table by entering "H" for combinations that cause the LED to illuminate and "L" for those that do not. Determine the logic function realized.



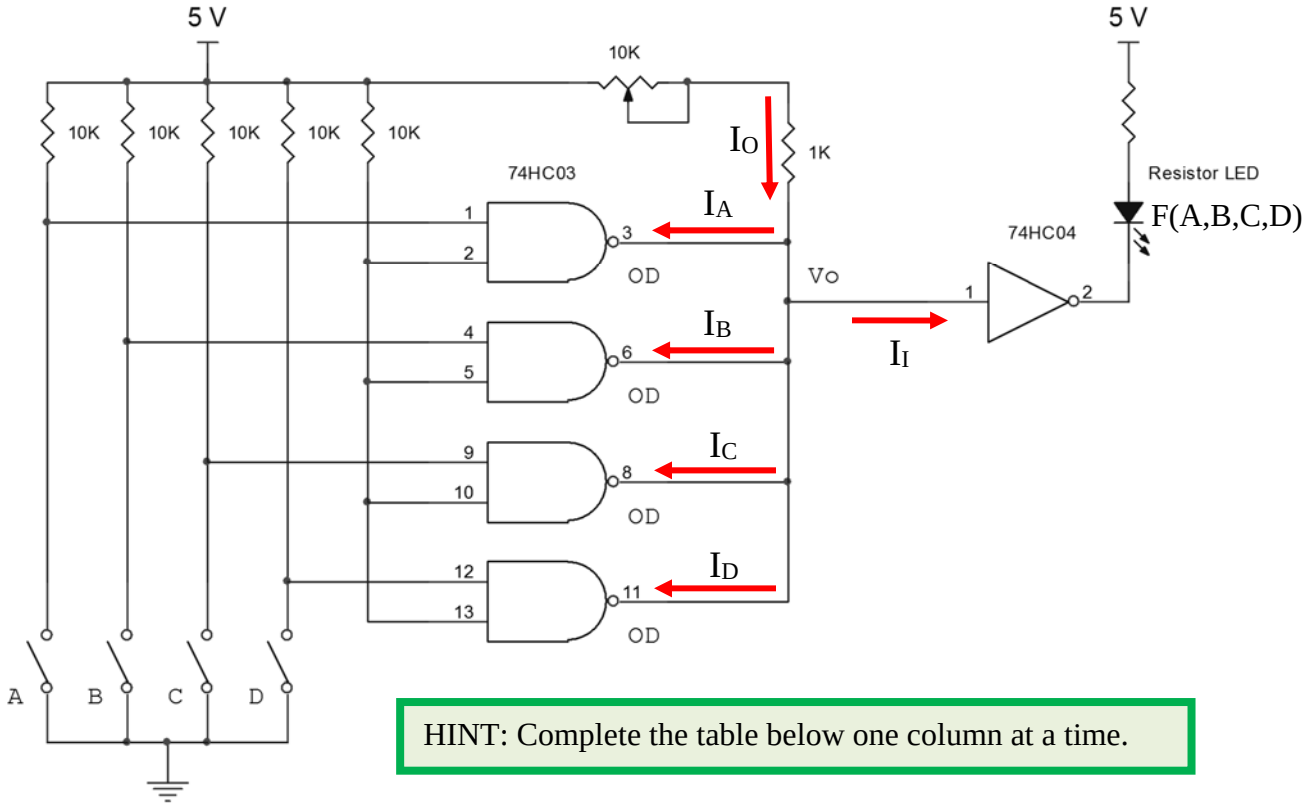
An open switch is "H" (logic 1 based on a positive logic convention), and a closed switch is "L" (logic 0 based on a positive logic convention).

A	B	C	D	F(A,B,C,D)
L	L	L	L	
L	L	L	H	
L	L	H	L	
L	L	H	H	
L	H	L	L	
L	H	L	H	
L	H	H	L	
L	H	H	H	
H	L	L	L	
H	L	L	H	
H	L	H	L	
H	L	H	H	
H	H	L	L	
H	H	L	H	
H	H	H	L	
H	H	H	H	

F(A,B,C,D) = _____

Step (2): Measuring Static (DC) Characteristics Based on Rmin

Setting the potentiometer to its ***minimum*** resistance setting will create a pull-up resistor for the open-drain gates approximately equal to **Rmin**. Complete the voltage/current chart for each case indicated, being careful to measure Vo with respect to ground and currents (I) ***in series.***



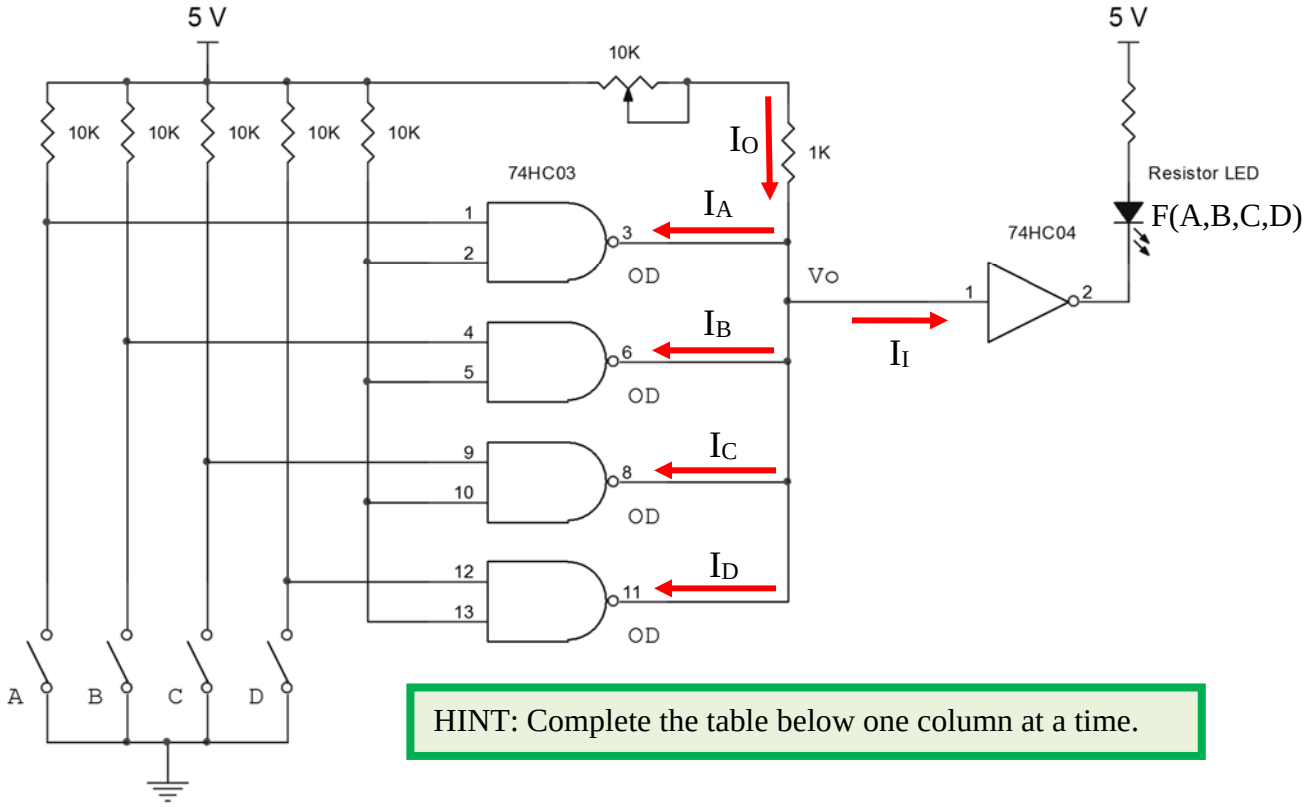
HINT: Complete the table below one column at a time.

A	B	C	D	V_O	I_O	I_A	I_B	I_C	I_D	I_I
L	L	L	L							
H	L	L	L							
H	H	L	L							
H	H	H	L							
H	H	H	H							

Note that some of the currents may be too small to measure reliably.

Step (3): Measuring Static (DC) Characteristics Based on Rmax

Setting the potentiometer to its ***maximum*** resistance setting will create a pull-up resistor for the open-drain gates approximately equal to **Rmax**. Complete the voltage/current chart for each case indicated, being careful to measure Vo with respect to ground and currents (I) ***in series.***



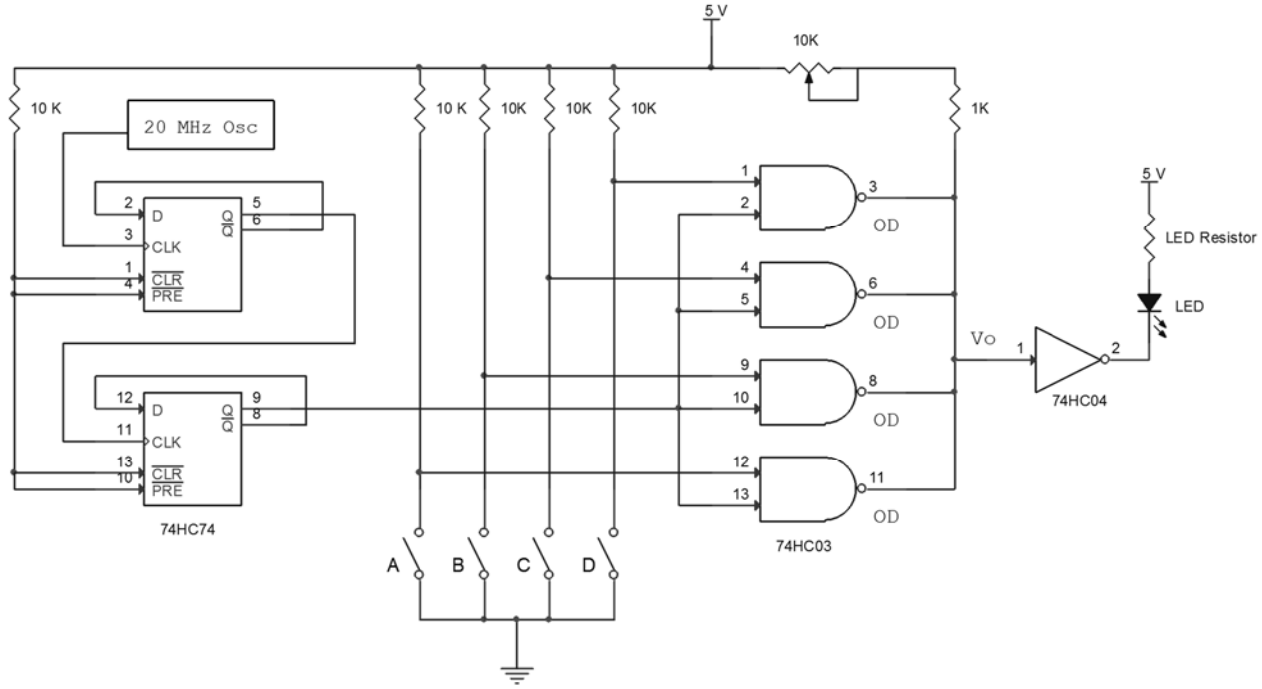
HINT: Complete the table below one column at a time.

A	B	C	D	V_O	I_O	I_A	I_B	I_C	I_D	I_I
L	L	L	L							
H	L	L	L							
H	H	L	L							
H	H	H	L							
H	H	H	H							

Note that some of the currents may be too small to measure reliably.

Step (4): Circuit Modification for Timing Measurements

Modify the circuit as illustrated below, using two "T" flip-flops to divide the 20 MHz oscillator output down to 5 MHz. Note that the resistor formerly connected to pins 2, 5, 10, and 13 of the 74HC03 should be removed. Set the potentiometer approximately mid-position and verify that the LED glows ***brightly*** when all the switches are closed (L) and glows ***somewhat less brightly*** when any combination of switches is open (H).



Step (5): Measuring Dynamic Characteristics Based on Rmin

Setting the potentiometer to its ***minimum*** resistance setting will create a pull-up resistor for the open-drain gates approximately equal to **Rmin**. Measure the propagation delay and rise/fall times for each case indicated. Note that propagation delays should be measured between pin 9 of the 74HC74 and the point labeled Vo; transition times should be measured at node Vo.

A	B	C	D	t_{PLH}	t_{PHL}	t_{TLH}	t_{THL}
H	L	L	L				
H	H	H	H				

Step (6): Observing Dynamic Characteristics Based on R > Rmin

Slowly advance the potentiometer from its ***minimum*** resistance setting to its ***maximum*** setting, and record your observations concerning the changes in rise/fall times and propagation delays that occur as a function of the pull-up resistor value.

Step (7): Thought Questions
Place your answers to the following "thought questions" in the space provided below.

(a) Summarize your findings regarding the static (DC) characteristics of open-drain gate outputs. Describe (in your own words) how the output voltage and current (Vo and Io) are affected by the choice of Rmin vs. Rmax as a pull-up resistor.

(b) Did the chart you completed for Steps (2) and (3) of the experiment confirm the "worst case proof" described in Module 1-J of the lecture notes? Did the voltages and currents you measured agree with those predicted? Why or why not?

(c) Summarize your findings regarding the dynamic (AC) characteristics of open-drain gate outputs. Describe (in your own words) how the transition times and propagation delays are affected by the choice of Rmin vs. Rmax as a pull-up resistor.

(d) Did the chart you completed for Step (5) and the observations you recorded for Step (6) of the experiment confirm the timing measurement (propagation delay and transition time) variations you expected based on the discussion in Module 1-J? Why or why not?

(e) In your own words, describe the tradeoffs between choosing Rmin vs. Rmax (or some value in-between) as the value of pull-up resistor to use for an open-drain circuit.

