Practice Homework Solution for Module 1

1. Unsigned base conversions (LO 1-1).

   (a) $(2C9E)_{16}$ **to base 2**

   $(0010\ 1100\ 1001\ 1110)_2$

   (b) $(1101001)_2$ **to base 10**

   $(105)_{10}$

   (c) $(1101001)_2$ **to base 16**

   $(69)_{16}$

   (d) $(8576)_{10}$ **to base 16**

   $(2180)_{16}$

   (e) $(A27F)_{16}$ **to base 8**

   $(121177)_8$

2. Short answer questions over basic electronic components (LO 1-7).

   (a) Write two different formulas for OHM's LAW:

   V=IR   V/I=R

   (b) Describe what a resistor does:

   Limits current flow

   (c) Write two different formulas for calculating the power dissipation of a resistor:

   V^2/R I^2R

   (d) Describe what a diode does.

   Restricts direction of current flow (from anode to cathode)

   (e) Describe what affects the brightness of a light emitting diode (LED):

   Forward current

   (f) Describe what a capacitor does:

   Stores charge

   (g) Describe a functional difference between a MOSFET and a BJT:

   MOSFETs are voltage-controlled switches, BJTs are current-controlled

   (h) When a MOSFET is off, its drain-to-source impedance is on the order of:

   o(1,000,000) ohms

   (i) When a MOSFET is on, its drain-to-source impedance is on the order of:

   o(10) ohms

   (j) Describe a functional difference between an N-channel MOSFET and a P-channel MOSFET:

   positive Vgs turns N-channel on, negative Vgs turns P-channel on

3. Prove DeMorgan's Law (T13) for **n=3** using perfect induction (LO 1-6).

X1	**X2**	**X3**	**X1 · X2 · X3**	**(X1 · X2 · X3)**	**(X1 · X2 · X3)′**	**X1′**	**X2′**	**X3′**	**X1′ + X2′ + X3′**
0	0	0	0	0	1	1	1	1	1
0	0	1	0	0	1	1	1	0	1
0	1	0	0	0	1	1	0	1	1
0	1	1	0	0	1	1	0	0	1
1	0	0	0	0	1	0	1	1	1
1	0	1	0	0	1	0	1	0	1
1	1	0	0	0	1	0	0	1	1
1	1	1	1	1	0	0	0	0	0

4. Prove the dual of the Covering theorem ($T9^D$) using axioms and other theorems (LO 1-3).

($T9^D$)   X · (X + Y) = X

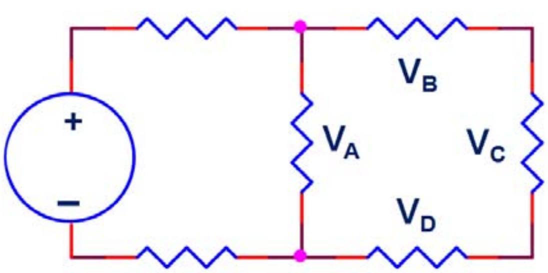
X · (X + Y) = (X+0) · (X + Y)   T1

= X + (Y · 0) $T8^D$

= X + 0 $T2^D$

= X   T1

5. Determine voltages V_A, V_B, V_C, and V_D if each resistor is 100Ω and the voltage source is 10 volts (LO 1-7).

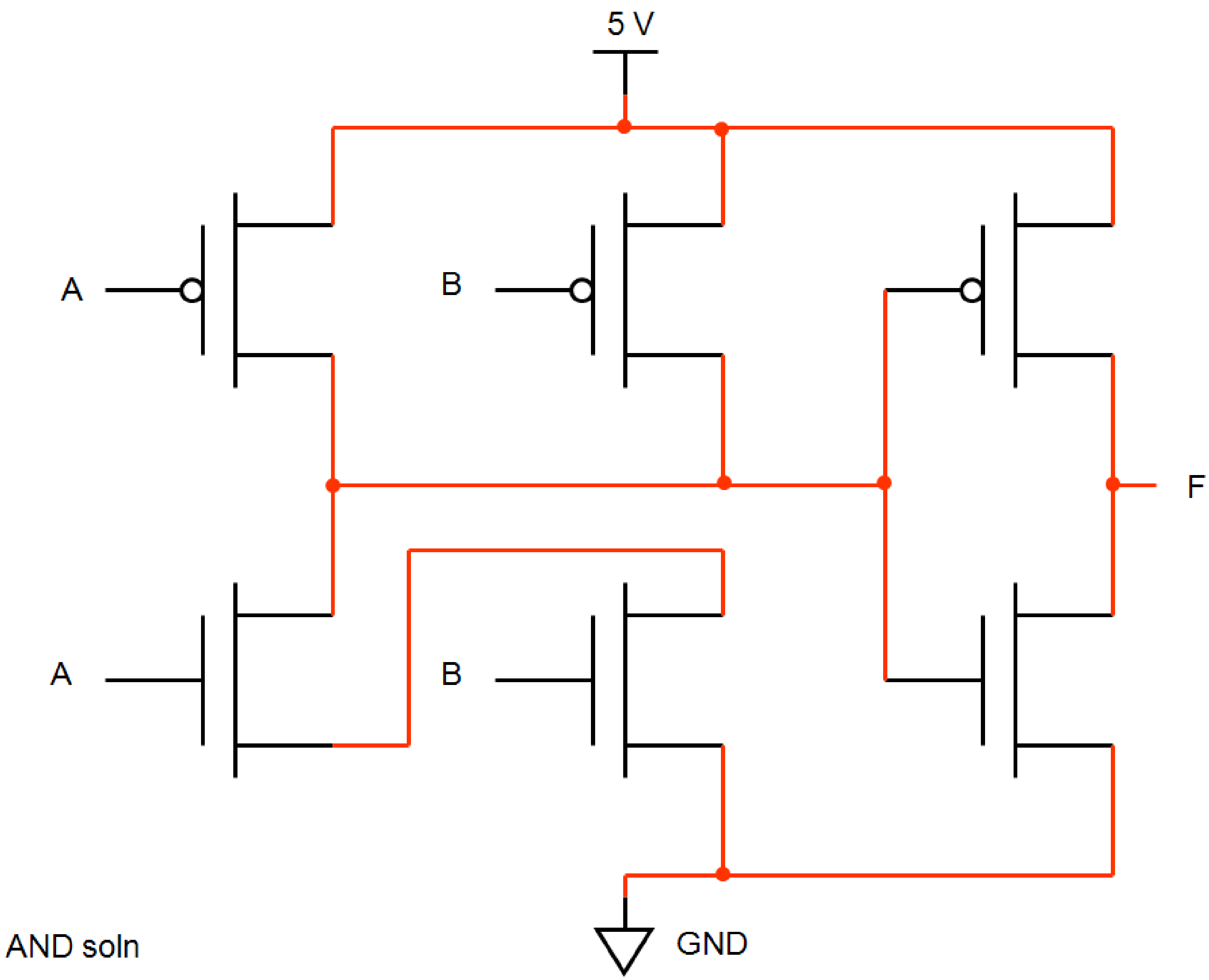


V_A = 10 x (75/275) = 2.73 V

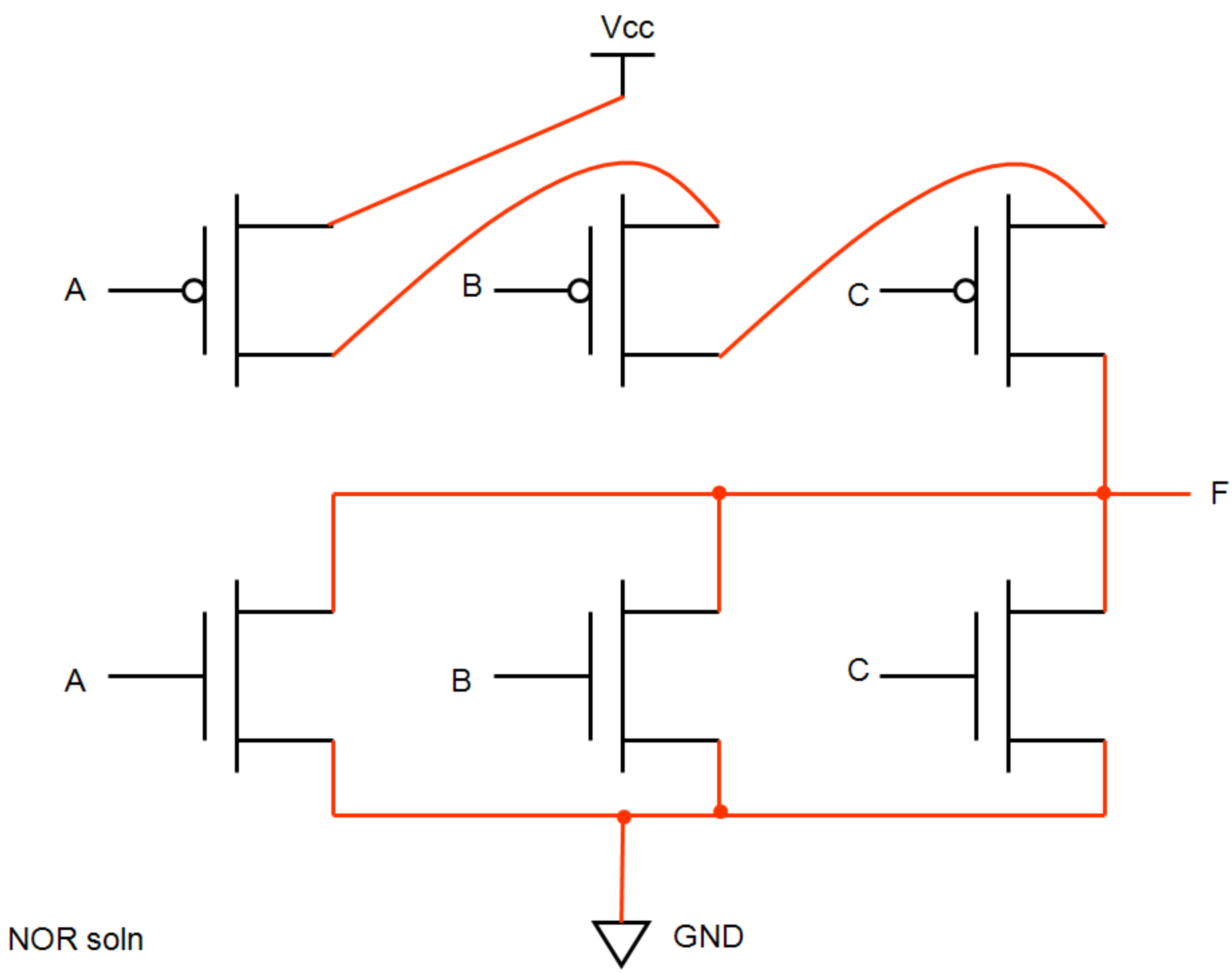
$V_A = V_B + V_C + V_D$ where $V_B = V_C = V_D$

$V_B = V_C = V_D$ = 0.91 V

6. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **two-input AND** gate. The gate inputs should be labeled A and B, and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well (LO 1-10).



7. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **three-input NOR** gate. The gate inputs should be labeled A, B and C, and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well (LO 1-12).



8. Given that a (5-volt) CMOS gate's P-channel output pull-up has an "on" resistance of 160Ω and that its N-channel output pull-down has an "on" resistance of 80Ω:

(a) If the desired V_{OHmin} is 4.4 volts and the desired V_{OLmax} is 0.4 volts, what are the gate's I_{OHmax} and I_{OLmax} ratings? (LO 1-19)

I_{OHmax} = **-0.6/160 = -3.75 mA** I_{OLmax} = **0.4/80 = 5.0 mA**

(b) If a DCNM of 1.2 volts is desired for this CMOS gate family, what do its V_{IHmin} and V_{ILmax} specifications need to be, based on the values given in part (a)? (LO 1-14)

V_{IHmin} = **4.4-1.2 = 3.2 V** V_{ILmax} = **0.4+1.2 = 1.6 V**

(c) If the I_{IH} and I_{IL} specifications for gates in this family are +0.1 mA and -0.1 mA, respectively, what is the practical fan-out for circuits constructed using these gates, based on values calculated in part (a)? (LO 1-20)

fanout = min(3.75/0.1, 5.0/0.1) = 37.5

Practical fan-out = **37 ("floor" of 37.5)**

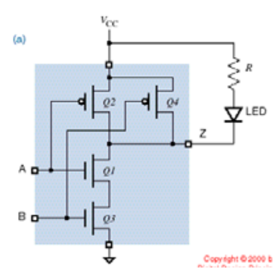
(d) Show how an LED (with forward voltage V_{LED} = 1.5 V) should be interfaced to gates in this family to obtain maximum brightness, and calculate the value of the current limiting resistor required along with its power dissipation. (LO 1-21)

Circuit and calculations:

$V_R = 5 - 1.5 - 0.4 = 3.1V$

$I_R = 5$ mA

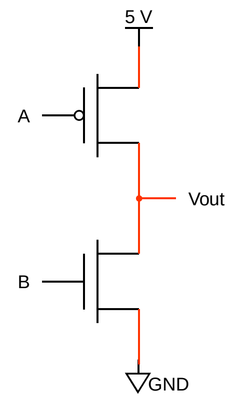
$R = 3.1/.005 = 620\ \Omega$



Current limiting resistor = 620 Ω Resistor power dissipation = 15.5 mW

9. Given that the P-channel device in the circuit below has **ON** and **OFF** resistances of **80 Ω** and **2 MΩ** (respectively) and that the N-channel device has **ON** and **OFF** resistances of **60 Ω** and **3 MΩ** (respectively), complete the table listing the **output voltages** obtained for each input combination as well as the **power dissipation** (in ***milliwatts***). *Show your calculations* (LOs 1-10 and 1-11).

A	B	P-ch	N-ch	Req (N+P)	V_{out}	Power Dissip Vcc^2/Req
0V	0V	on	off	3,000,080 Ω	4.99987	0.008333 mW
0V	5V	on	on	140 Ω	2.14286	178.57 mW
5V	0V	off	off	5,000,000 Ω	3.00000	0.005 mW
5V	5V	off	on	2,000,060 Ω	0.0001499	0.0124996 mW

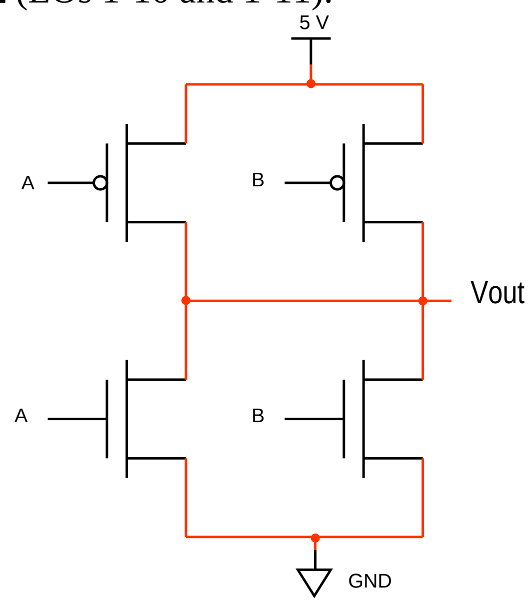


10. One of your best friends from another major, "Raul", found some N- and P-channel MOSFETs in your "geek box" and wired them together as shown below. Help Raul figure out what he has created by determining V_{out} for all possible input combinations (for the sake of analysis, assume the **ON** resistance of **each** MOSFET (both P- and N-channel) is **10Ω** and that its **OFF** resistance is **1 MΩ** (LOs 1-10 and 1-11).

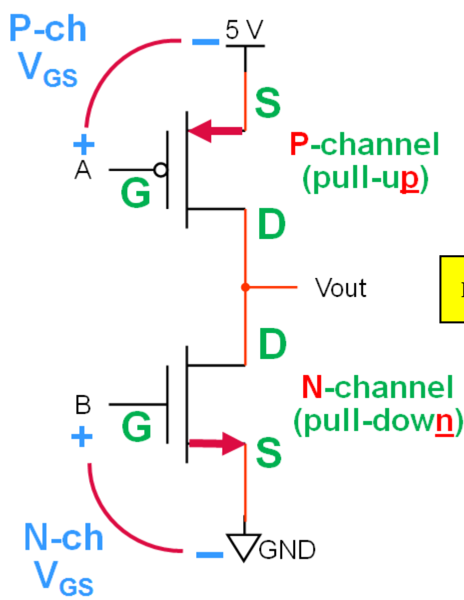
A	B	V_{out}
0V	0V	4.99995
0V	5V	2.5000
5V	0V	2.5000
5V	5V	0.000049995

Describe what Raul has created:

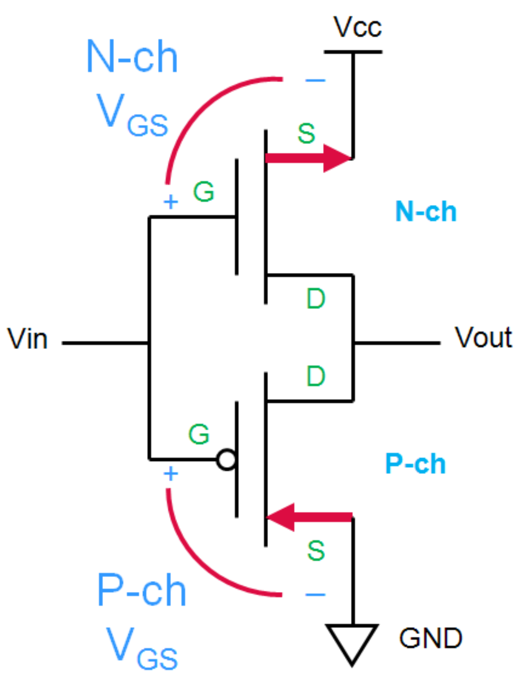
"nothing useful"



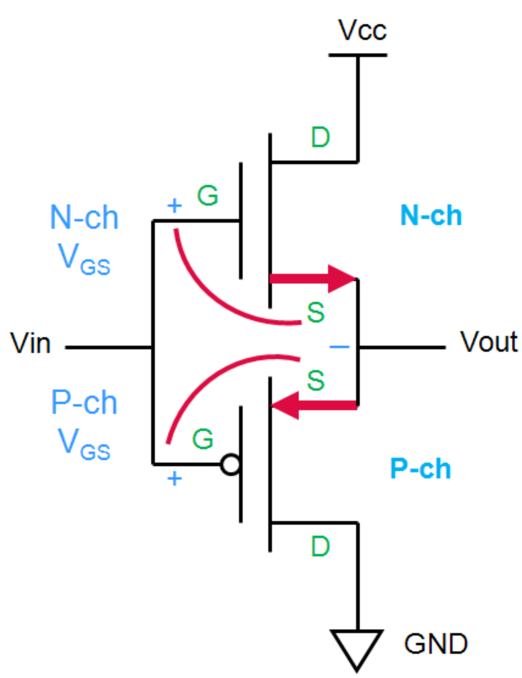
11. A common question students have relates to ***why*** the P-channel device has to serve as a “pull-up” while the N-channel device has to serve as a “pull-down” (i.e., why can’t it be the “other way around”?). To convince yourself of this reality, try drawing a CMOS inverter “upside down” (with an N-channel device used as a pull-up and a P-channel device used as a pull-down) and analyze the circuit you have created (i.e., determine its Vi-Vo characteristics). Describe your conclusion. (LO 1-10)



normal CMOS inverter



“flipped” upside-down → current unable to flow (*cannot pull output high or low*)



each transistor “flipped” in “upside-down” circuit → unable to establish V_{GS} potential to turn either transistor ON

12. Assume two hypothetical logic families have the following D.C. characteristics:

Logic Family "A"

$V_{CC} = 5$ V	$V_{OH} = 4.4$ V	$V_{OL} = 0.40$ V	$V_{IH} = 3.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} – V_{OL})/2$	$I_{OH} = -4$ mA	$I_{OL} = 4$ mA	$I_{IH} = 0.4\ \mu A$	$I_{IL} = -0.4\ \mu A$

Logic Family "B"

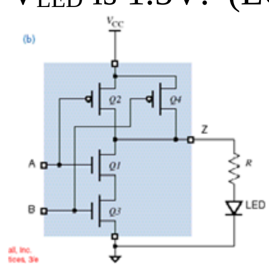
$V_{CC} = 5$ V	$V_{OH} = 3.3$ V	$V_{OL} = 0.30$ V	$V_{IH} = 2.60$ V	$V_{IL} = 1.60$ V
$V_{TH} = (V_{OH} – V_{OL})/2$	$I_{OH} = -400\ \mu A$	$I_{OL} = 8$ mA	$I_{IH} = 40\ \mu A$	$I_{IL} = -0.4$ mA

(a) Calculate the following (*show work*):

- (LO 1-14) DCNM $_{A\rightarrow B}$ **min(4.4-2.6, 1.6-0.4) = 1.2V**
- (LO 1-14) DCNM $_{B\rightarrow A}$ **min(3.3-3.6, 1.6-0.3) = -0.3V**
- (LO 1-20) Practical Fanout $_{A\rightarrow B}$ **min(4/0.04, 4/0.4) = 10**
- (LO 1-20) Practical Fanout $_{B\rightarrow A}$ **min(400/0.4, 8/0.0004) = 1000**

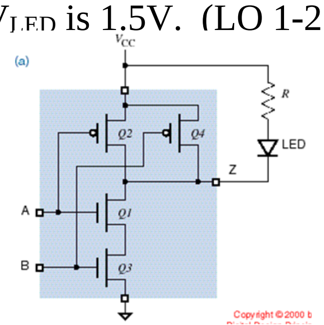
(b) Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "A"** gate driving an LED to the maximum brightness possible in a ***current sourcing*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)

R= 2.9/0.004 = 725 Ω



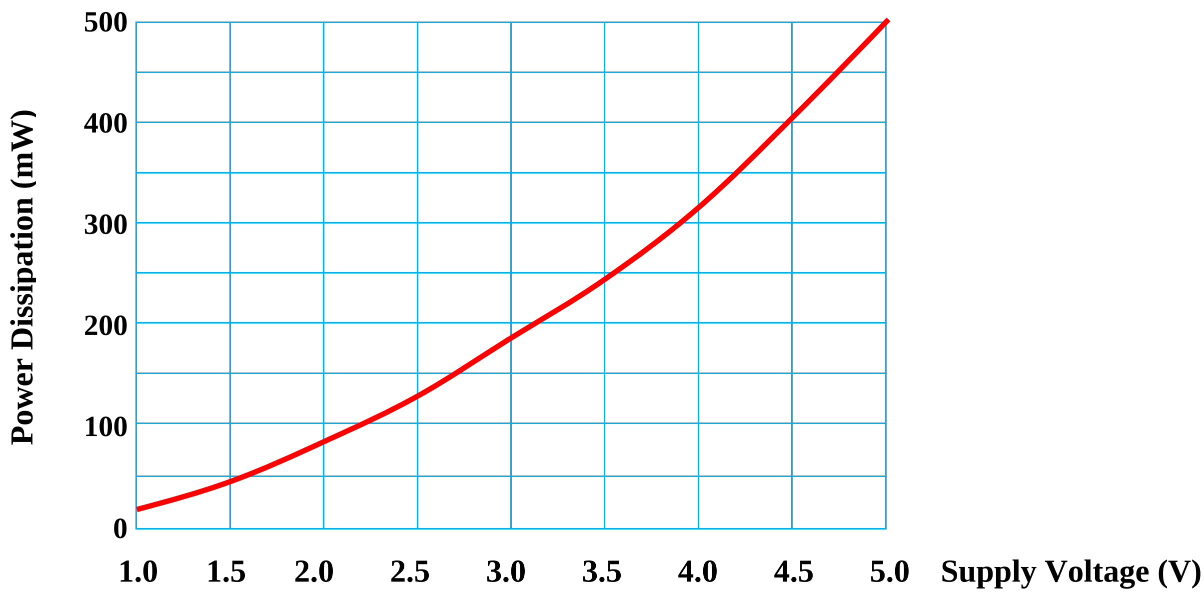
(c) Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "B"** gate driving an LED to the maximum brightness possible in a ***current sinking*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)

R = 3.2/0.008 = 400 Ω

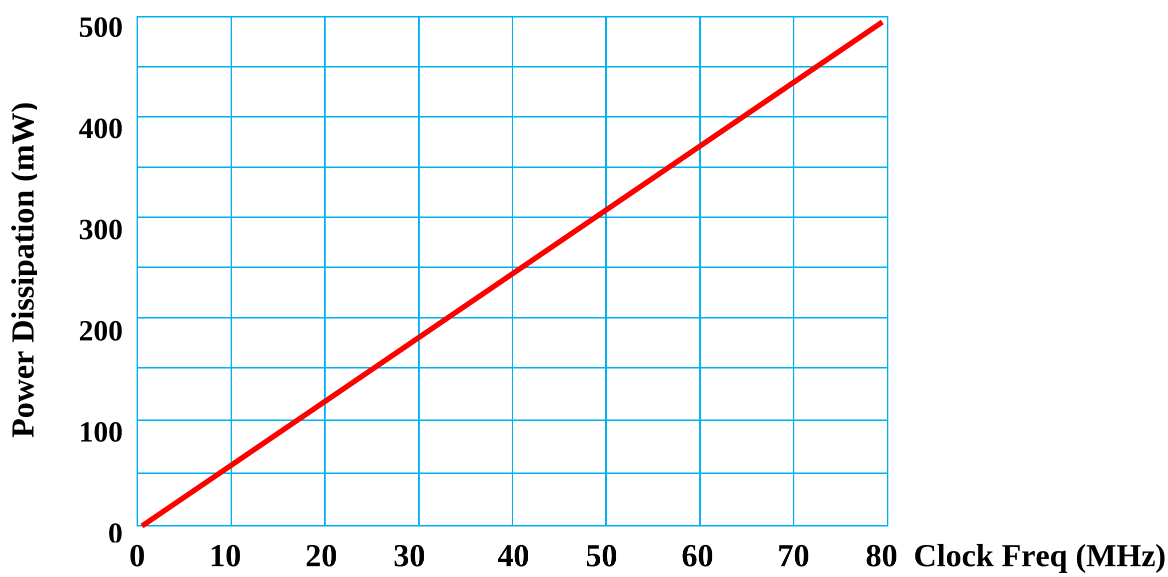


13. A particular CMOS microcontroller is designed to operate over a supply voltage range of **1.0 V** to **5.0 V** and at a maximum clock frequency of **80 MHz** (no minimum clock frequency is specified). The *maximum power dissipation* over this range of supply voltage and clock frequency is specified to be **500 milliwatts**.

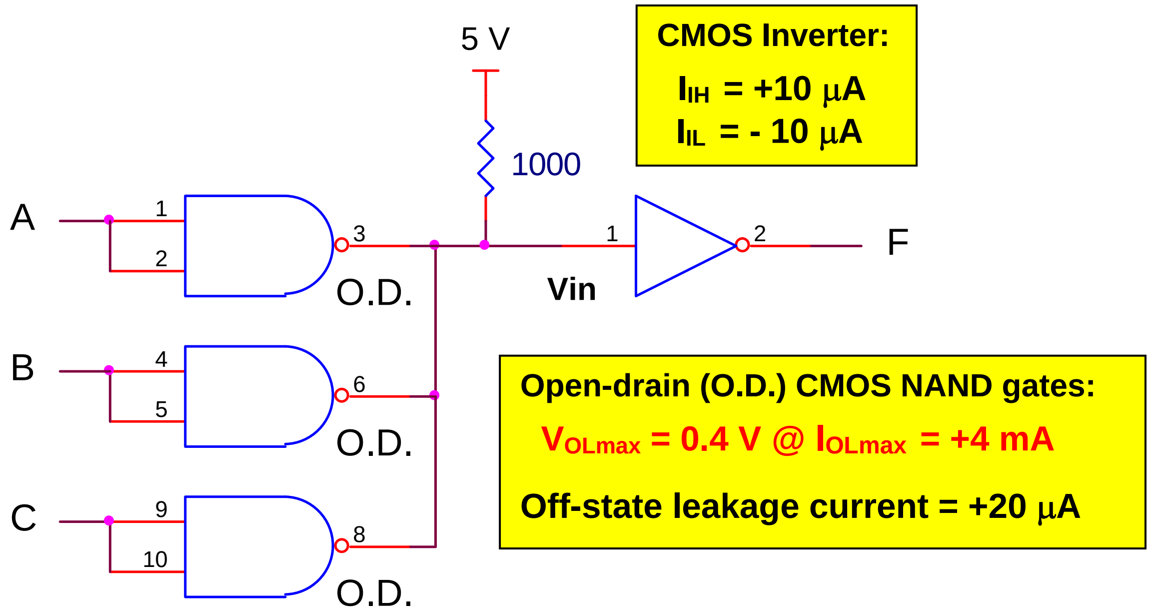
(a) Plot the relationship between *power dissipation* and *supply voltage* for this microcontroller (LO 1-29).



(b) Plot the relationship between *power dissipation* and *clock frequency* for this microcontroller (LO 1-28).



14. Given the circuit, below, calculate V_{in} (the CMOS inverter input voltage) for each of the cases indicated along with the current ***individually*** sunk by each active open drain gate. *Show your calculations.* (LOs 1-34 and 1-35).



Key: ON resistance of each OD gate is 0.4/0.004 = 100 Ω

A	B	C	Ron Total	V_{in} to Inverter	Current Sunk by Each Active O.D. Gate
0 V	0 V	0 V	-	5 – (0.00007x1000) = 4.93 V	(20 μA leakage)
5 V	0 V	0 V	1100	5x100/1100 = 0.4545 V	4.545 mA
5 V	5 V	0 V	1050	5x50/1050 = 0.2381 V	2.381 mA
5 V	5 V	5 V	1033	5x33/1033 = 0.1597 V	1.618 mA

15. Given the circuit, below, along with its Vi-Vo (input – output voltage) relationship, determine the following (show calculations where applicable):

    (a) estimate the ON resistance of the O.D. NAND gate (LO 1-25)
    fall time = 10 ns = R_{on} x 100 pF → R_{on} = 100Ω
    (b) estimate the value of the pull-up resistor (LO 1-36)
    rise time = 100 ns = R_{pullup} x 100 pF → R_{pullup} = 1000Ω
    (c) estimate the t_{TLH} of the O.D. NAND gate (LO 1-25)
    rise time = 100 ns
    (d) estimate the t_{THL} of the O.D. NAND gate (LO 1-25)
    fall time = 10 ns
    (e) estimate the t_{PHL} of the O.D. NAND gate (LO 1-23)
    fall propagation delay = 10 ns
    (f) estimate the t_{PLH} of the O.D. NAND gate (LO 1-23)
    rise propagation delay = 40 ns