Practice Homework Problems for Module 1

1. Unsigned base conversions (LO 1-1).

   (a) **$(2C9E)_{16}$ to base 2**

   (b) **$(1101001)_{2}$ to base 10**

   (c) **$(1101001)_{2}$ to base 16**

   (d) **$(8576)_{10}$ to base 16**

   (e) **$(A27F)_{16}$ to base 8**

2. Short answer questions over basic electronic components (LO 1-7).

   (a) Write two different formulas for OHM's LAW:

   (b) Describe what a resistor does:

   (c) Write two different formulas for calculating the power dissipation of a resistor:

   (d) Describe what a diode does.

   (e) Describe what affects the brightness of a light emitting diode (LED):

   (f) Describe what a capacitor does:

   (g) Describe a functional difference between a MOSFET and a BJT:

   (h) When a MOSFET is off, its drain-to-source impedance is on the order of:

   (i) When a MOSFET is on, its drain-to-source impedance is on the order of:

   (j) Describe a functional difference between an N-channel MOSFET and a P-channel MOSFET:

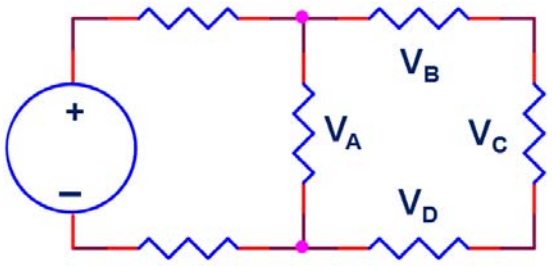
3. Prove DeMorgan's Law (T13) for **n=3** using perfect induction (LO 1-6).

X1	X2	X3	X1 · X2 · X3	(X1 · X2 · X3)	(X1 · X2 · X3)′	X1′	X2′	X3′	X1′ + X2′ + X3′
0	0	0							
0	0	1							
0	1	0							
0	1	1							
1	0	0							
1	0	1							
1	1	0							
1	1	1							

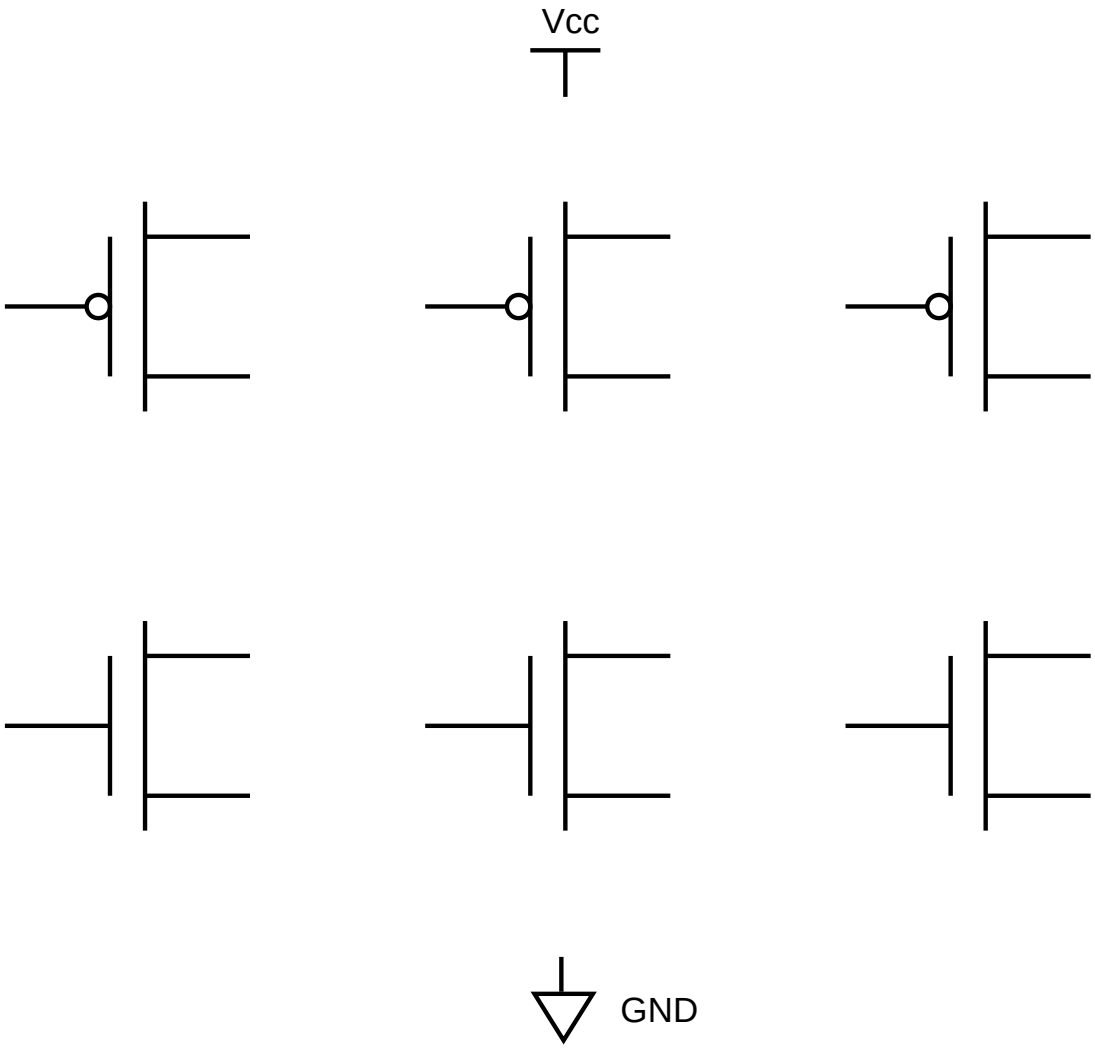
4. Prove the dual of the Covering theorem ($T9^D$) using axioms and other theorems (LO 1-3).

($T9^D$) X · (X + Y) = X

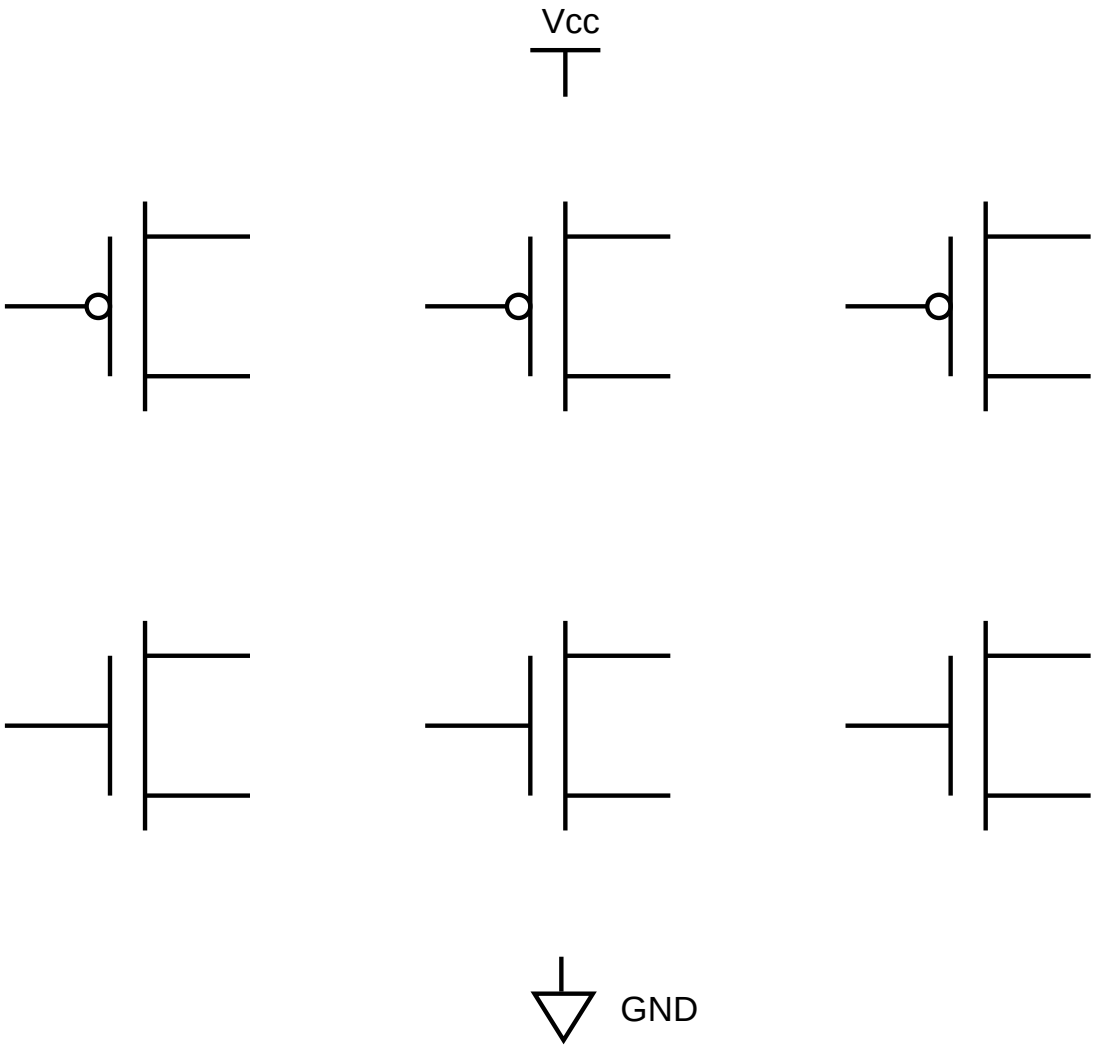
5. Determine voltages V_A, V_B, V_C, and V_D if each resistor is 100Ω and the voltage source is 10 volts (LO 1-7).



6. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **two-input AND** gate. The gate inputs should be labeled A and B, and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well (LO 1-10).



7. Using a total of **three** N-channel MOSFETs and **three** P-channel MOSFETs, draw a circuit schematic for a **three-input NOR** gate. The gate inputs should be labeled A, B and C, and the gate output should be labeled F. Be sure to show the power (Vcc) and ground (GND) connections as well (LO 1-12).



8. Given that a (5-volt) CMOS gate's P-channel output pull-up has an "on" resistance of 160Ω and that its N-channel output pull-down has an "on" resistance of 80Ω:

(a) If the desired V_{OHmin} is 4.4 volts and the desired V_{OLmax} is 0.4 volts, what are the gate's I_{OHmax} and I_{OLmax} ratings? (LO 1-19)

I_{OHmax} = _____ mA I_{OLmax} = _____ mA

(b) If a DCNM of 1.2 volts is desired for this CMOS gate family, what do its V_{IHmin} and V_{ILmax} specifications need to be, based on the values given in part (a)? (LO 1-14)

V_{IHmin} = _____ V V_{ILmax} = _____ V

(c) If the I_{IH} and I_{IL} specifications for gates in this family are +0.1 mA and -0.1 mA, respectively, what is the practical fan-out for circuits constructed using these gates, based on values calculated in part (a)? (LO 1-20)

Practical fan-out = _____

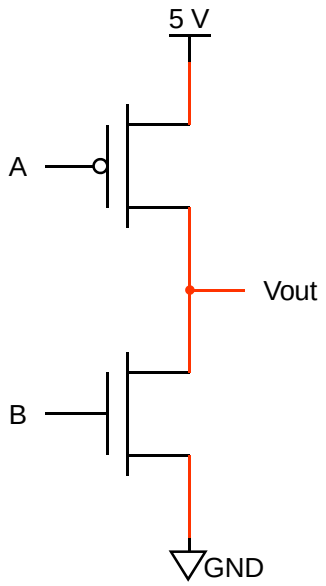
(d) Show how an LED (with forward voltage V_{LED} = 1.5 V) should be interfaced to gates in this family to obtain maximum brightness, and calculate the value of the current limiting resistor required along with its power dissipation. (LO 1-21)

Circuit and calculations:

Current limiting resistor = _____Ω Resistor power dissipation = _____ mW

9. Given that the P-channel device in the circuit below has **ON** and **OFF** resistances of **80 Ω** and **2 MΩ** (respectively) and that the N-channel device has **ON** and **OFF** resistances of **60 Ω** and **3 MΩ** (respectively), complete the table listing the **output voltages** obtained for each input combination as well as the **power dissipation** (in ***milliwatts***). *Show your calculations* (LOs 1-10 and 1-11).

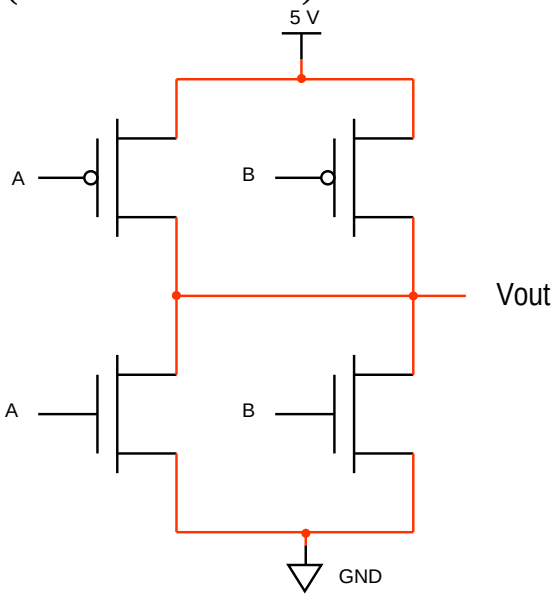
A	B	V_{out}	Power Dissipation
0V	0V		
0V	5V		
5V	0V		
5V	5V		



10. One of your best friends from another major, "Raul", found some N- and P-channel MOSFETs in your "geek box" and wired them together as shown below. Help Raul figure out what he has created by determining V_{out} for all possible input combinations (for the sake of analysis, assume the **ON** resistance of **each** MOSFET (both P- and N-channel) is **10Ω** and that its **OFF** resistance is **1 MΩ** (LOs 1-10 and 1-11).

A	B	V_{out}
0V	0V	
0V	5V	
5V	0V	
5V	5V	

Describe what Raul has created:



11. A common question students have relates to ***why*** the P-channel device has to serve as a "pull-up" while the N-channel device has to serve as a "pull-down" (i.e., why can't it be the "other way around"?). To convince yourself of this reality, try drawing a CMOS inverter "upside down" (with an N-channel device used as a pull-up and a P-channel device used as a pull-down) and analyze the circuit you have created (i.e., determine its Vi-Vo characteristics). Describe your conclusion. (LO 1-10)

12. Assume two hypothetical logic families have the following D.C. characteristics:

Logic Family "A"

V_{CC} = 5 V	V_{OH} = 4.4 V	V_{OL} = 0.40 V	V_{IH} = 3.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -4 mA	I_{OL} = 4 mA	I_{IH} = 0.4 μA	I_{IL} = -0.4 μA

Logic Family "B"

V_{CC} = 5 V	V_{OH} = 3.3 V	V_{OL} = 0.30 V	V_{IH} = 2.60 V	V_{IL} = 1.60 V
$V_{TH} = (V_{OH} - V_{OL})/2$	I_{OH} = -400 μA	I_{OL} = 8 mA	I_{IH} = 40 μA	I_{IL} = -0.4 mA

(a) Calculate the following (*show work*):

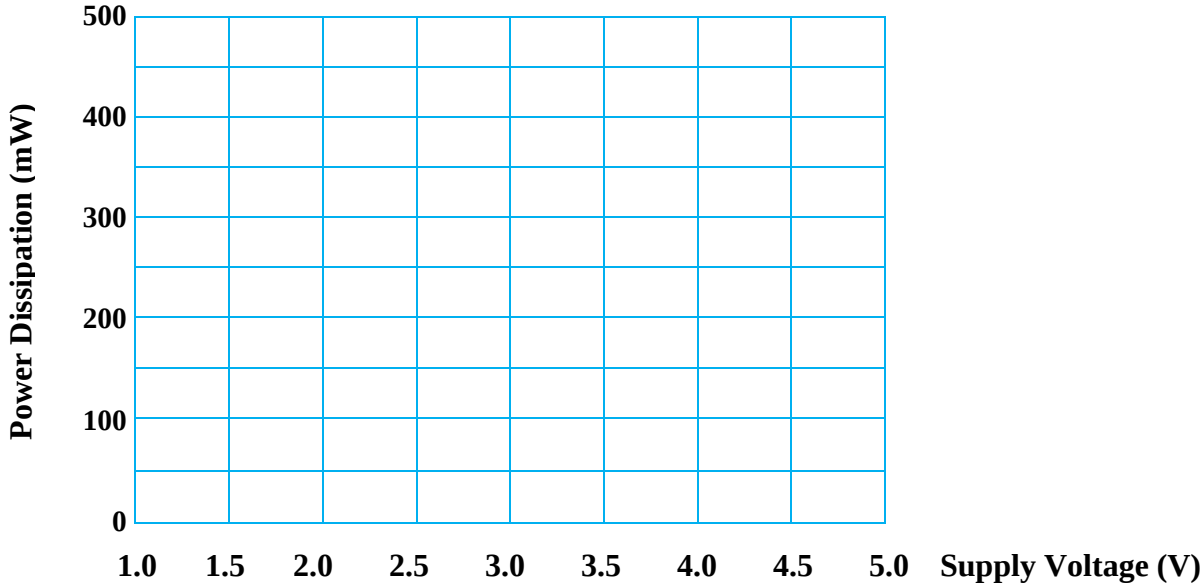
- (LO 1-14) DCNM $_{A\rightarrow B}$
- (LO 1-14) DCNM $_{B\rightarrow A}$
- (LO 1-20) Practical Fanout $_{A\rightarrow B}$
- (LO 1-20) Practical Fanout $_{B\rightarrow A}$

(b) Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "A"** gate driving an LED to the maximum brightness possible in a ***current sourcing*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)

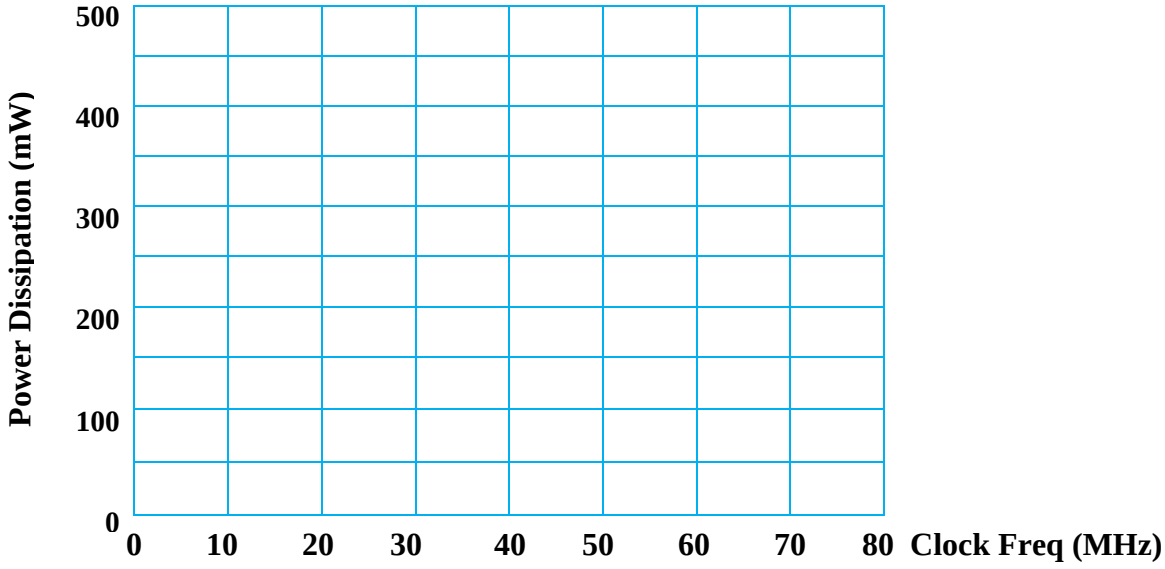
(c) Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "B"** gate driving an LED to the maximum brightness possible in a ***current sinking*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)

13. A particular CMOS microcontroller is designed to operate over a supply voltage range of **1.0 V** to **5.0 V** and at a maximum clock frequency of **80 MHz** (no minimum clock frequency is specified). The *maximum power dissipation* over this range of supply voltage and clock frequency is specified to be **500 milliwatts**.

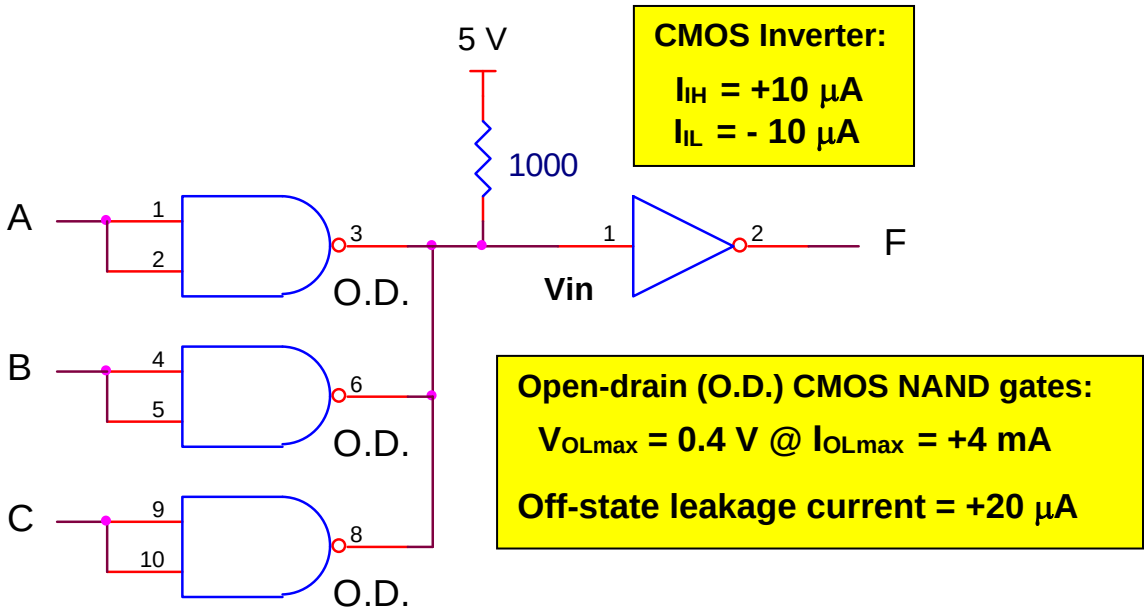
(a) Plot the relationship between *power dissipation* and *supply voltage* for this microcontroller (LO 1-29).



(b) Plot the relationship between *power dissipation* and *clock frequency* for this microcontroller (LO 1-28).



14. Given the circuit, below, calculate V_{in} (the CMOS inverter input voltage) for each of the cases indicated along with the current ***individually*** sunk by each active open drain gate. *Show your calculations.* (LOs 1-34 and 1-35).



A	B	C	V_{in} to Inverter	Current Sunk by Each Active O.D. Gate
0 V	0 V	0 V		
5 V	0 V	0 V		
5 V	5 V	0 V		
5 V	5 V	5 V		

15. Given the circuit, below, along with its Vi-Vo (input – output voltage) relationship, determine the following (show calculations where applicable):

    a. estimate the ON resistance of the O.D. NAND gate (LO 1-25)

    b. estimate the value of the pull-up resistor (LO 1-36)

    c. estimate the t_{TLH} of the O.D. NAND gate (LO 1-25)

    d. estimate the t_{THL} of the O.D. NAND gate (LO 1-25)

    e. estimate the t_{PHL} of the O.D. NAND gate (LO 1-23)

    f. estimate the t_{PLH} of the O.D. NAND gate (LO 1-23)