Homework 9 - Solution

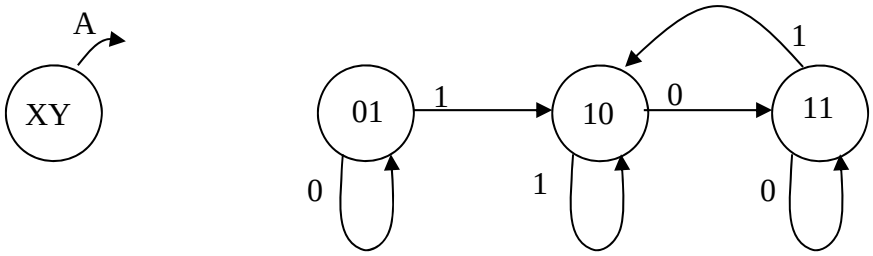
Due at the beginning of your scheduled lab period

Last Name (Printed): _____ **Lab Div:** _____ **Date:** _____

E-mail: __ __ __ __ __ __ __ __ **@**purdue.edu **Signature:** _____

*Printed copies of these pages along with your original (**hand-annotated**, **not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.***

1. [8 points] Given the following state transition diagram, determine:



(a) The next state equation for X if the state machine is designed for **minimum cost**

X* = X+A

(b) The next state equation for X if the state machine is designed for **minimum risk**

X* = X + A•Y (based on forcing to state 01 from unused state – other solutions too)

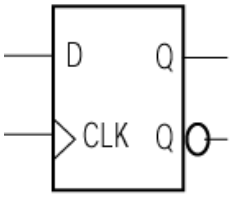
(c) The next state equation for Y if the state machine is designed for **minimum cost**

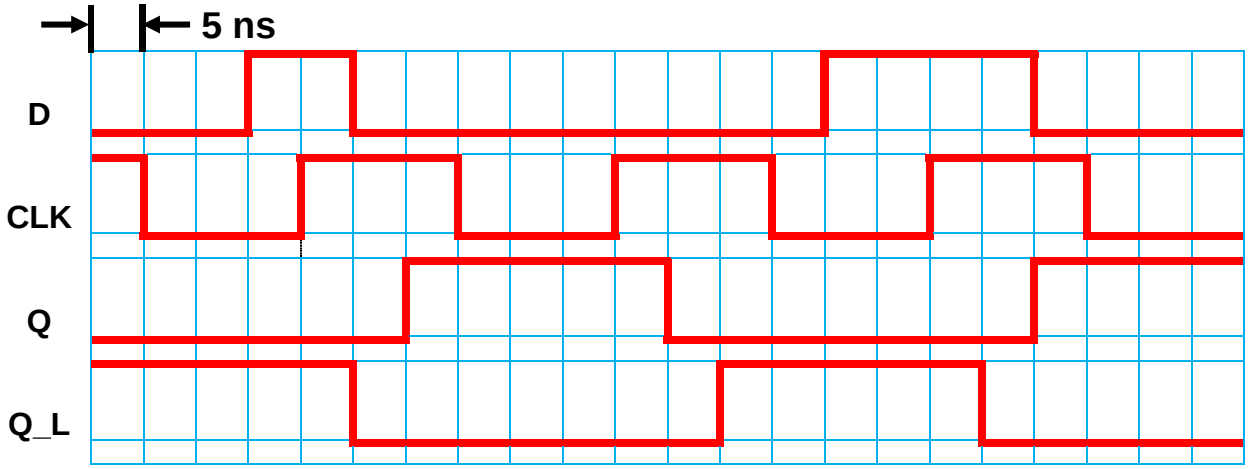
Y* = A′

(d) The next state equation for Y if the state machine is designed for **minimum risk**

Y* = A′ + X′•Y′ (based on forcing to state 01 from unused state – other solutions too)

2. [5 pts] Given the following timing chart for an edge-triggered D flip-flop, determine the following based on the excitation signals (D and CLK) depicted:





(a) The **nominal setup time** provided for the D flip-flop 5 ns

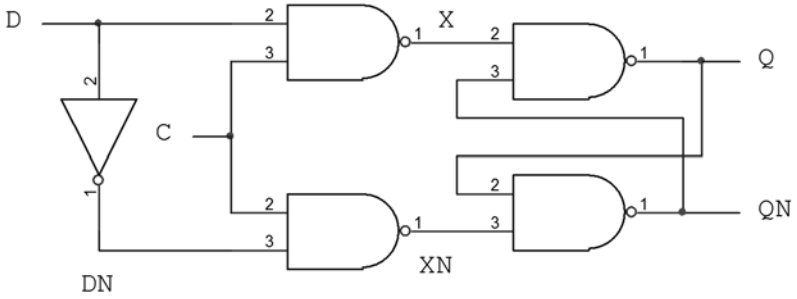
(b) The **nominal hold time** provided for the D flip-flop 5 ns

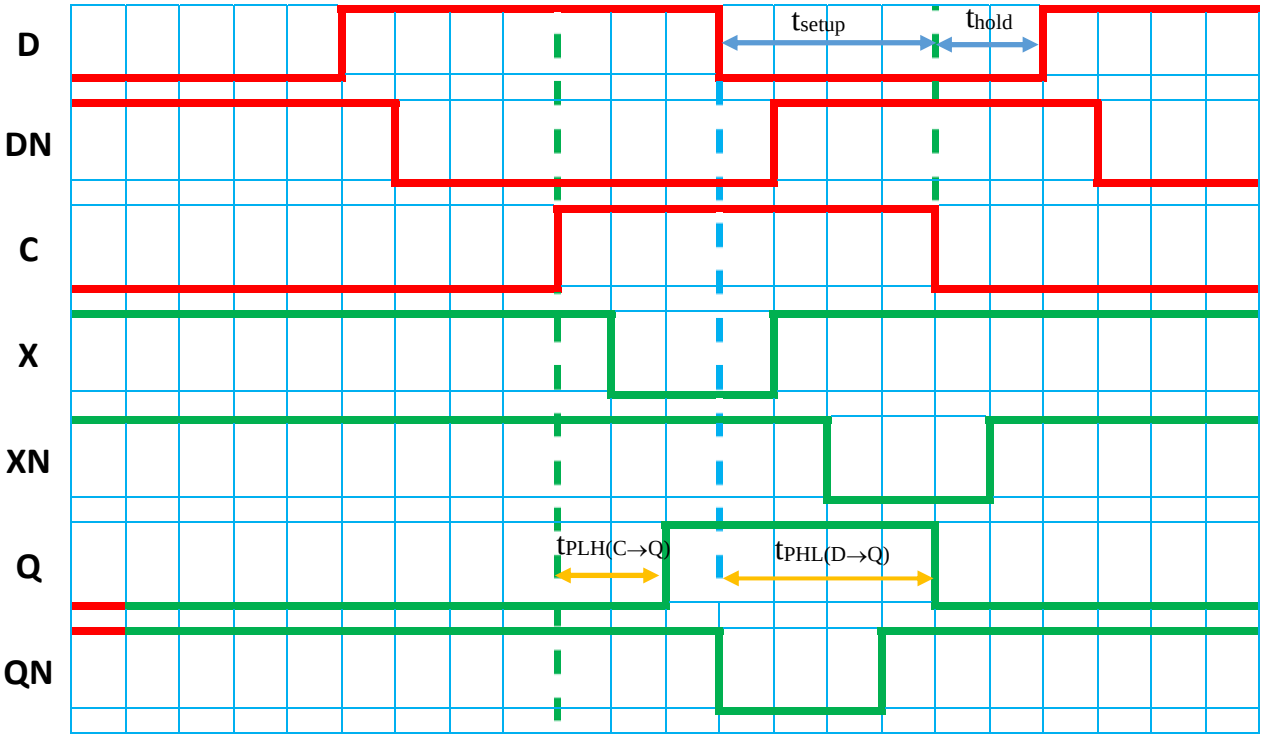
(c) The **nominal clock pulse width** provided for the D flip-flop 15 ns

(d) The $\mathbf{t_{PHL(C\rightarrow Q)}}$ of the D flip-flop 5 ns

(e) The $\mathbf{t_{PLH(C\rightarrow Q)}}$ of the D flip-flop 10 ns

3. [13 pts] Complete the timing chart, below, for a D latch with enable (C), and answer the questions that follow. Assume each gate has 10 ns of delay (t_{PLH} and t_{PHL}), and that each division on the chart is 10 ns. 2 pts, each waveform; 1 pt, each value





(a) Determine the **minimum time** input C should be asserted (while the D input remains stable) to ensure reliable operation of the latch. 20 ns (2 gate delays)

(b) Determine the **nominal setup time** provided for the D latch. 40 ns

(c) Determine the **nominal hold time** provided for the D latch. 20 ns

(d) Determine the $\mathbf{t_{PLH(C\rightarrow Q)}}$ of the D latch. 20 ns

(e) Determine the $\mathbf{t_{PHL(D\rightarrow Q)}}$ of the D latch. 40 ns

Score: _____ / 26