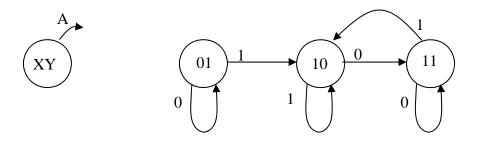
## Homework 9

Due at the beginning of your scheduled lab period

Last Name (Printed):		Lab Div:	Date:
E-mail:	@purdue.edu Signature:		

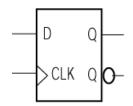
<u>Printed</u> copies of these pages along with your <u>original</u> (hand-annotated, not photocopied) written solution in the <u>space provided</u> (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – copying the work of someone else does not accomplish this.

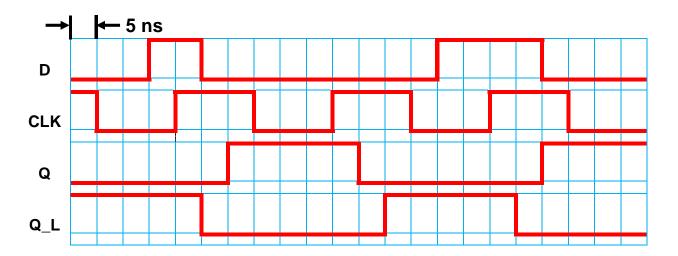
1. [8 points] Given the following state transition diagram, determine:



- (a) The next state equation for X if the state machine is designed for **minimum cost**
- (b) The next state equation for  $\boldsymbol{X}$  if the state machine is designed for  $\boldsymbol{minimum\ risk}$
- (c) The next state equation for Y if the state machine is designed for minimum cost
- (d) The next state equation for Y if the state machine is designed for **minimum risk**

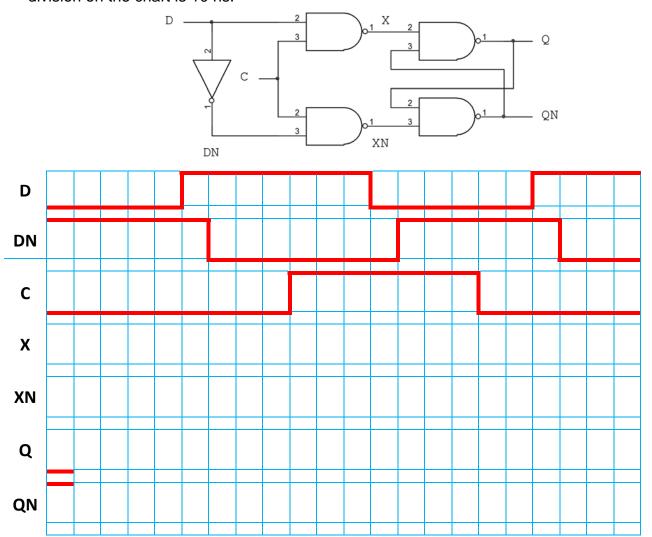
2. [5 pts] Given the following timing chart for an edge-triggered D flip-flop, determine the following based on the excitation signals (D and CLK) depicted:





- (a) The **nominal setup time** provided for the D flip-flop
- (b) The **nominal hold time** provided for the D flip-flop
- (c) The nominal clock pulse width provided for the D flip-flop
- (d) The  $t_{PHL(C\rightarrow Q)}$  of the D flip-flop
- (e) The  $\mathbf{t}_{\mathsf{PLH}(\mathsf{C} \to \mathsf{Q})}$  of the D flip-flop

3. [13 pts] Complete the timing chart, below, for a D latch with enable (C), and answer the questions that follow. Assume each gate has 10 ns of delay (tplh and tphl), and that each division on the chart is 10 ns.



- (a) Determine the **minimum time** input C should be asserted (while the D input remains stable) to ensure reliable operation of the latch.
- (b) Determine the **nominal setup time** provided for the D latch.
- (c) Determine the **nominal hold time** provided for the D latch.
- (d) Determine the  $\mathbf{t}_{PLH(C \to Q)}$  of the D latch.
- (e) Determine the  $\mathbf{t}_{PHL(D\rightarrow Q)}$  of the D latch.