Homework 8 – Key

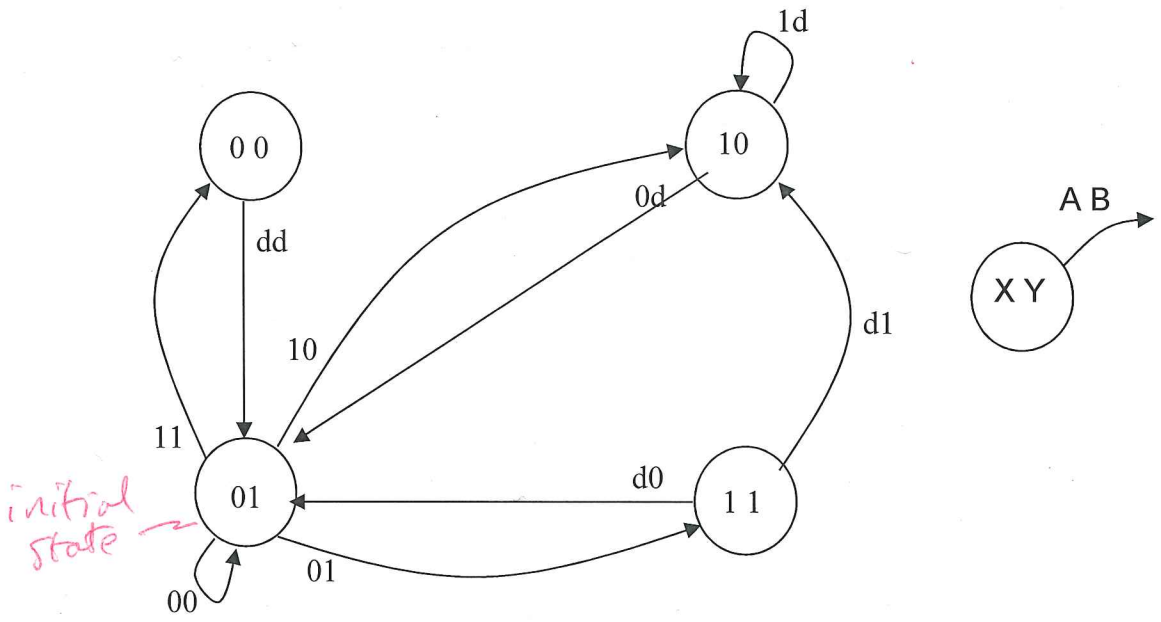
Due at the beginning of your scheduled lab period

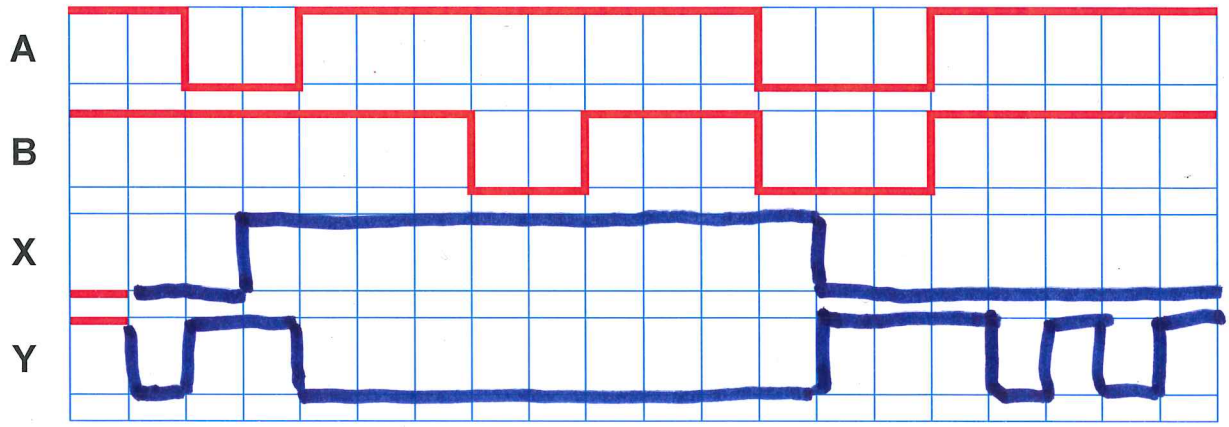
Last Name (Printed): _____ **Lab Div:** _____ **Date:** _____

E-mail: _____@purdue.edu **Signature:** _____

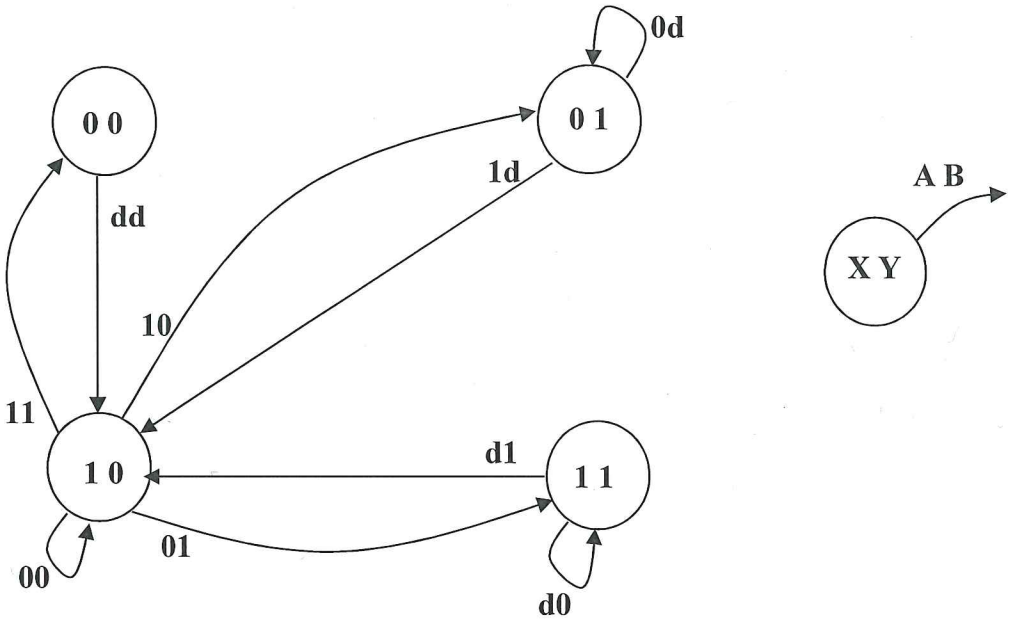
*Printed copies of these pages along with your original (**hand-annotated**, **not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.***

1. [4 pts] Given the following state transition diagram, complete the timing chart below.



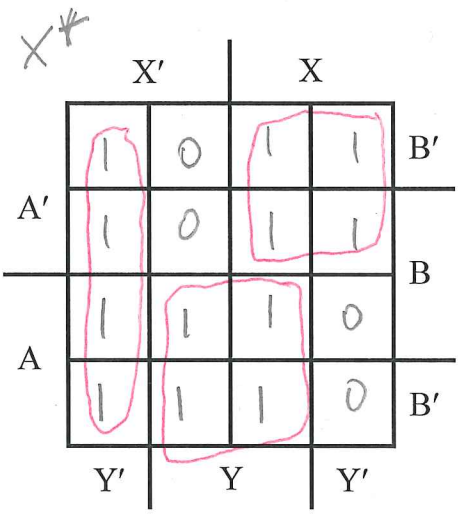


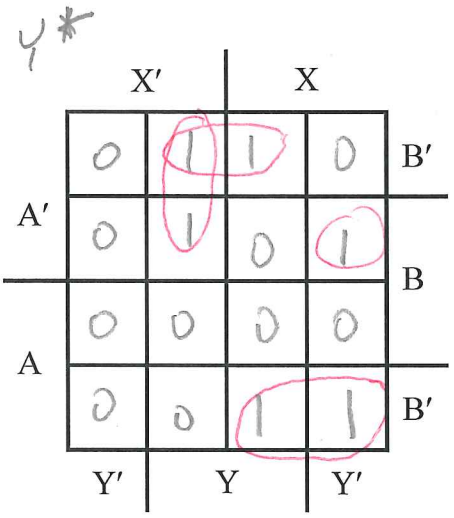
2. [6 pts] Given the following state transition diagram, determine the *next state equations* it represents in *minimum sum-of-products form.*



X	Y	A	B	X*	Y*
0	0	0	0	1	0
0	0	0	1	1	0
0	0	1	0	1	0
0	0	1	1	1	0
0	1	0	0	0	1
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	1	0
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	1	0	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	1	1
1	1	1	1	1	0

X* and Y* are "shorthand" for the next state of X and Y

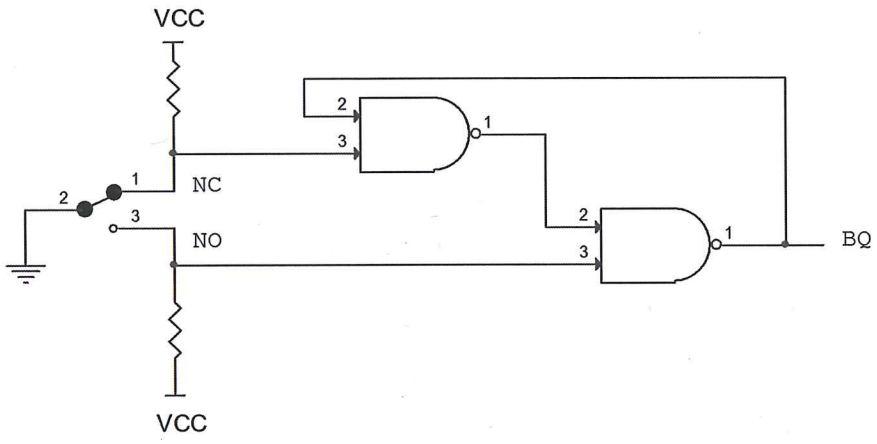




$X^* = X'Y' + A'X + AY$

$Y^* = A'X'Y + A'B'Y + AB'X + A'BXY'$

3. [4 pts] Write a Verilog code module that implements the following circuit:



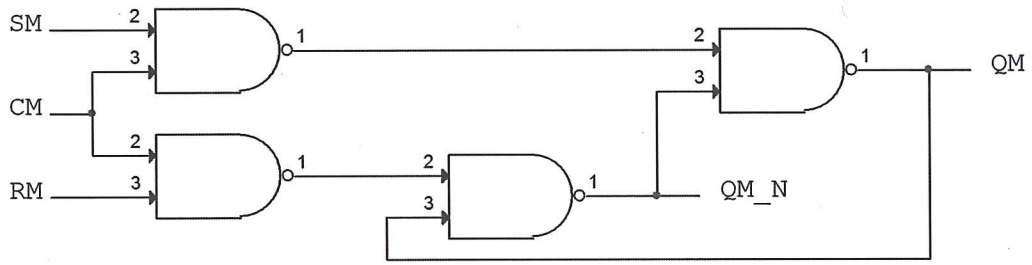

```
module bounceless_switch(NC,NO,BQ);

 input wire NC,NO;
 output wire BQ;

 assign BQ = ~NO | (NC & BQ);


endmodule
```

4. [6 pts] Write a Verilog code module that implements the following circuit:




```
module master_latch(SM,RM,CM,QM,QM_N);

 input wire SM,RM,CM;
 output wire QM,QM_N;

 assign QM = ~(~(SM&CM) & QM_N);
 assign QM_N = ~(~(RM&CM) & QM);


endmodule
```

Score: _____ / 20