

Homework 5

Due at the beginning of your scheduled lab period

Last Name (Printed): _____ Lab Div: _____ Date: _____

E-mail: _____ @purdue.edu Signature: _____

Printed copies of these pages along with your *original* (**hand-annotated, not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. **NOTE:** The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.**

1. [4 pts] For the function mapped below:

	W'		W		
Y'	1	1	0	1	Z'
	0	0	0	1	
Y	1	0	0	1	Z
	1	1	0	1	Z'
	X'	X	X'		

(a) Write a minimal sum-of-products expression and calculate its cost:

(b) Write a minimal product-of-sums expression and calculate its cost:

2. [4 pts] Express the *complement* of the following function as an ON SET and draw a NAND-NAND circuit realization:

$$F(X,Y,Z) = X' \cdot Y + X \cdot Z'$$

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3. [4 pts] Express the *dual* of the following function as an OFF SET and draw a NOR-NOR circuit realization:

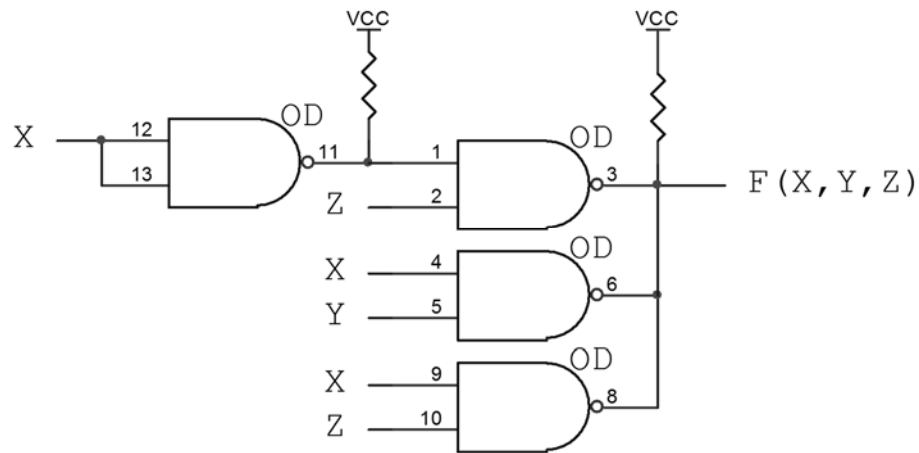
$$F(X,Y,Z) = X \cdot Y' + X' \cdot Z$$

4. [12 pts] Assuming that *only true* variables are available, realize the function $F(X,Y,Z)$ mapped below three different ways:
- Using only 7400 (quad 2-input NAND) chips
 - Using only 7402 (quad 2-input NOR) chips
 - Using only 7403 (quad 2-input open-drain NAND) chips

	X'		X	
Z'	0	1	1	1
Z	1	0	0	1
	Y'	Y		Y'

Show complete schematics for each realization, along with your derivations.

5. [6 pts] Given the following circuit, determine the ON set and write both a minimal SoP and minimal PoS expression for the function it realizes.



6. [6 pts] Sketch the response of the circuit, below, to the input signals provided. Assume the input signals (A, B, C) have been in the initial states shown prior to the beginning of the chart, and that each gate has a t_{PLH} and t_{PHL} of 10 ns. *Identify the hazard* (by name) if one occurs in the output (F).

