Homework 4

Due at the beginning of your scheduled lab period

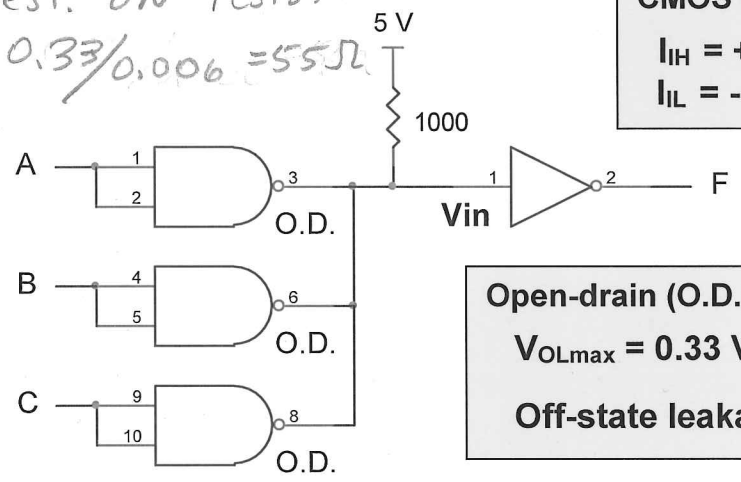
Last Name (Printed): KEY **Lab Div:** ____ **Date:** ____

E-mail: _____@purdue.edu **Signature:** 18 PTS

*Printed copies of these pages along with your original (**hand-annotated, not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.***

1. [12 pts] Given the circuit, below, calculate V_{in} (the CMOS inverter input voltage) for each of the cases indicated along with the current ***individually*** sunk by each active open drain gate. *Show your calculations.* (LOs 1-34 and 1-35).

est. ON resistance
0.33/0.006 = 55Ω



CMOS Inverter:
I_{IH} = +2 µA
I_{IL} = - 2 µA

Open-drain (O.D.) CMOS NAND gates:
V_{OLmax} = 0.33 V @ I_{OLmax} = +6 mA
Off-state leakage current = +25 µA

A	B	C	O.D. Equivalent ON Resistance	V_{in} to Inverter	Current Sunk by Each Active O.D. Gate
0 V	0 V	0 V	—	4.923 V	25 µA - leakage only
5 V	0 V	0 V	1055 Ω	0.261 V	4.74 mA
5 V	5 V	0 V	1027.5 Ω	0.134 V	2.43 mA
5 V	5 V	5 V	1018.3 Ω	0.090 V	1.64 mA

all off.

leakage = 3 × 25 µA + I_{IH} (2 µA) = 77 µA

$V_{in} = 5 - (77 \times 10^{-6}) \times 10^{3} = 4.923$ V

2. [6 pts] Given the circuit, below, along with its Vi-Vo (input – output voltage) relationship, determine the following (show calculations where applicable):

   a. estimate the ON resistance of the O.D. NAND gate (LO 1-25)

   fall time = 5ns = R_{on} X 100pF → R_{on} = 50Ω

   b. estimate the value of the pull-up resistor (LO 1-36)

   rise time = 35ns = R_{pullup} X 100pF → R_{pullup} = 350Ω

   c. estimate the t_{TLH} of the O.D. NAND gate (LO 1-25)

   rise time = 35ns

   d. estimate the t_{THL} of the O.D. NAND gate (LO 1-25)

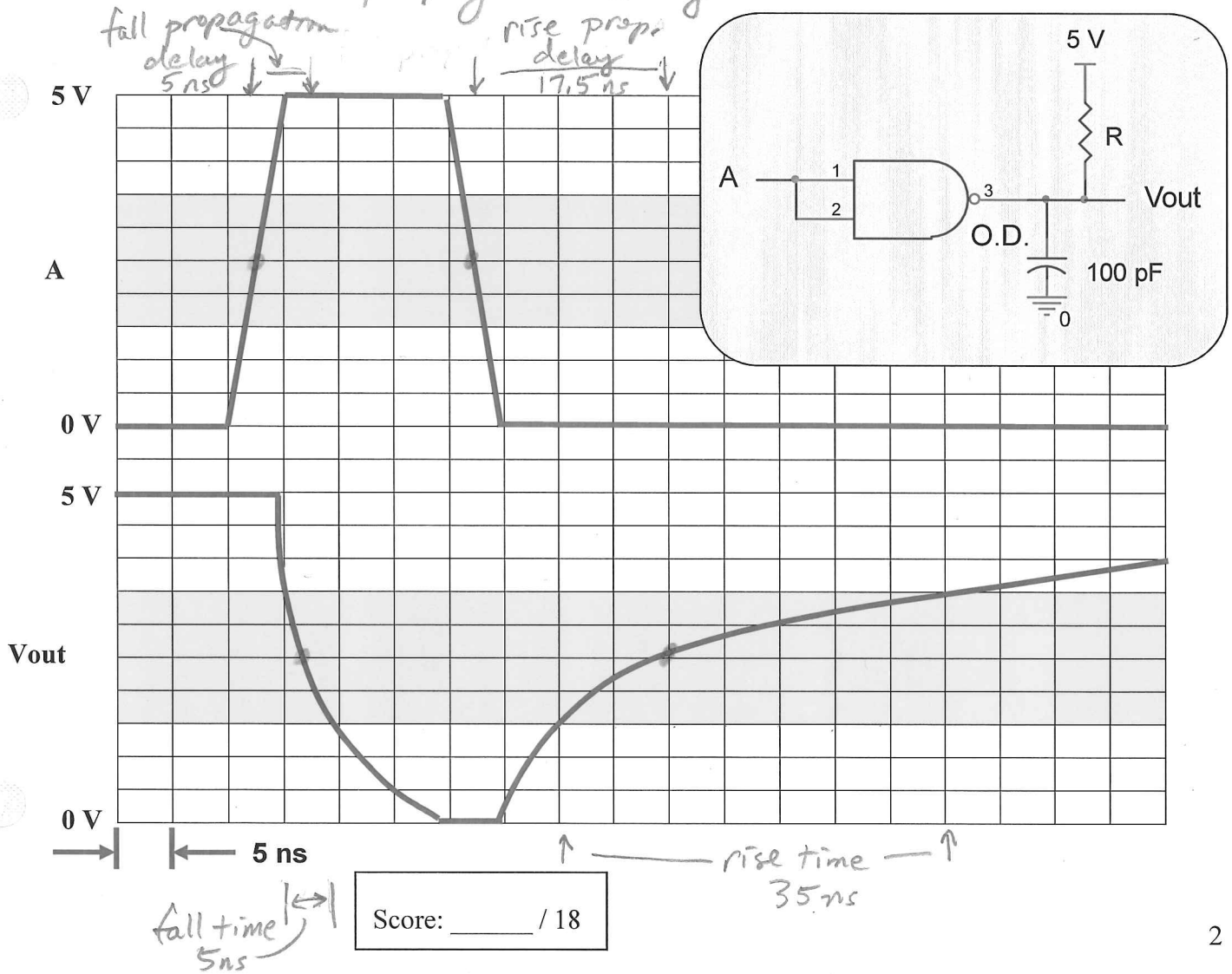
   fall time = 5ns

   e. estimate the t_{PHL} of the O.D. NAND gate (LO 1-23)

   fall propagation delay = 5 ns

   f. estimate the t_{PLH} of the O.D. NAND gate (LO 1-23)

   rise propagation delay = 17.5 ns



Score: _____ / 18