Homework 3

Due at the beginning of your scheduled lab period

Last Name (Printed): KEY **Lab Div:** ____ **Date:** ____

E-mail: ____@purdue.edu **Signature:** 20 PTS

*Printed copies of these pages along with your original (**hand-annotated, not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.***

1. [8 pts] Assume two logic families have the following D.C. characteristics:

Logic Family "A"

$V_{CC} = 5$ V	$V_{OH} = 4.1$ V	$V_{OL} = 0.4$ V	$V_{IH} = 3.3$ V	$V_{IL} = 1.3$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -7.5$ mA	$I_{OL} = 7.5$ mA	$I_{IH} = 0.25$ µA	$I_{IL} = -0.25$ µA

Logic Family "B"

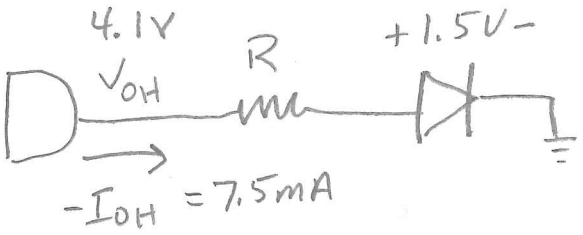
$V_{CC} = 5$ V	$V_{OH} = 3.4$ V	$V_{OL} = 0.33$ V	$V_{IH} = 2.7$ V	$V_{IL} = 1.2$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -900$ µA	$I_{OL} = 8.8$ mA	$I_{IH} = 13$ µA	$I_{IL} = -0.13$ mA

(a) [4 pts] Calculate the following (*show work*):

- (LO 1-14) DCNM $_{A\to B}$ $\min(4.1 - 2.7,\ 1.2 - 0.4) = 0.8\,V$
- (LO 1-14) DCNM $_{B\to A}$ $\min(3.4 - 3.3,\ 1.3 - 0.33) = 0.1\,V$
- (LO 1-20) Practical Fanout $_{A\to B}$ $\min\left(\frac{7.5}{0.013},\ \frac{7.5}{0.13}\right) = 57$
- (LO 1-20) Practical Fanout $_{B\to A}$ $\min\left(\frac{900}{0.25},\ \frac{8800}{0.25}\right) = 3600$

Problem 1, continued…

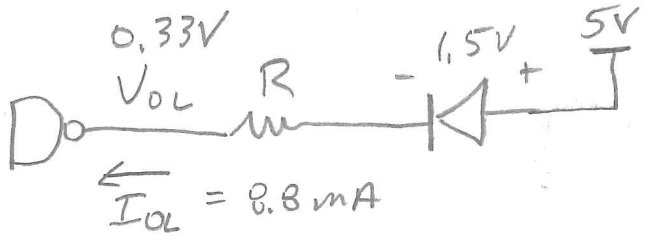
(b) [2 pts] Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "A"** gate driving an LED to the maximum brightness possible in a ***current sourcing*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)



$V_R = 4.1 - 1.5 = 2.6V$

$R = 2.6 / 0.0075 = 347\,\Omega$

(c) [2 pts] Draw the circuit and calculate the **value of the current limiting resistor** for a **Type "B"** gate driving an LED to the maximum brightness possible in a ***current sinking*** configuration. Assume V_{LED} is 1.5V. (LO 1-21)



$V_R = 5 - 1.5 - 0.33$

$= 3.17V$

$R = 3.17 / 0.0088 = 360\,\Omega$

2. [8 pts] Given that a (5-volt) CMOS gate's P-channel pull-up has an "on" resistance of 60 Ω and that its N-channel pull-down has an "on" resistance of 30 Ω:

(a) [2 pts] If the desired V_{OHmin} is 4.6 volts and the desired V_{OLmax} is 0.25 volts, what are the gate's I_{OHmax} and I_{OLmax} ratings? (LO 1-19)

$-0.4\,V / 60\,\Omega$ $\qquad$ $0.25\,V / 30\,\Omega$

I_{OHmax} = -6.67 mA $\qquad$ I_{OLmax} = 8.3 mA

(b) [2 pts] If a DCNM of 1.5 volts is desired for this CMOS gate family, what do its V_{IHmin} and V_{ILmax} specifications need to be, based on the values given in part (a)? (LO 1-14)

$4.6 - 1.5$ $\qquad$ $0.25 + 1.5$

V_{IHmin} = 3.1 V $\qquad$ V_{ILmax} = 1.75 V

(c) [1 pt] If the I_{IH} and I_{IL} specifications for gates in this family are +0.1 mA and -0.1 mA, respectively, what is the practical fan-out for circuits constructed using these gates, based on values calculated in part (a)? (LO 1-20)

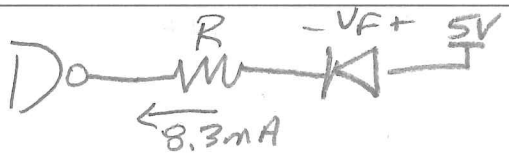
$\min(6.67/0.1,\ 8.3/0.1) = 66.7$

Practical fan-out = 66

Note – practical fanout is the next lowest integer ("floor function")

(d) [3 pts] Show how an LED (forward voltage V_{LED} = 1.5 V) should be interfaced to gates in this family to obtain maximum brightness, and calculate the value of the current limiting resistor required along with its power dissipation. (LO 1-21)

Circuit and calculations:



$V_R = 5 - 1.5 - 0.25$

$= 3.25\,V$

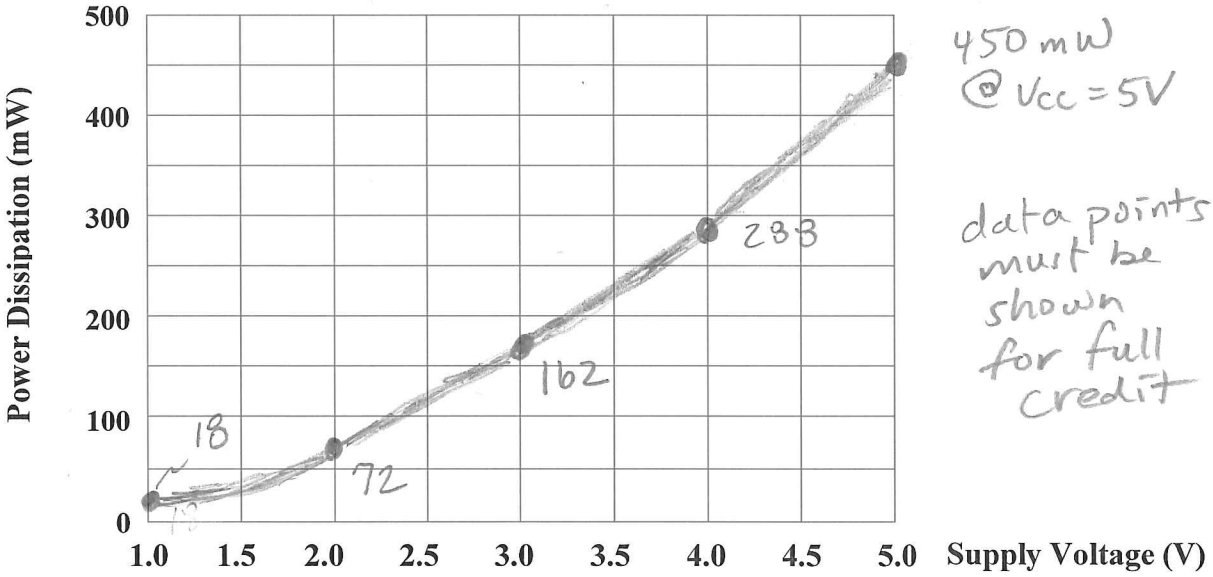
$R = \frac{3.25}{0.0083} = 392\,\Omega$ $\qquad$ $P_R = I^2R = (0.0083)^2(392)$

$= 27\,mW$

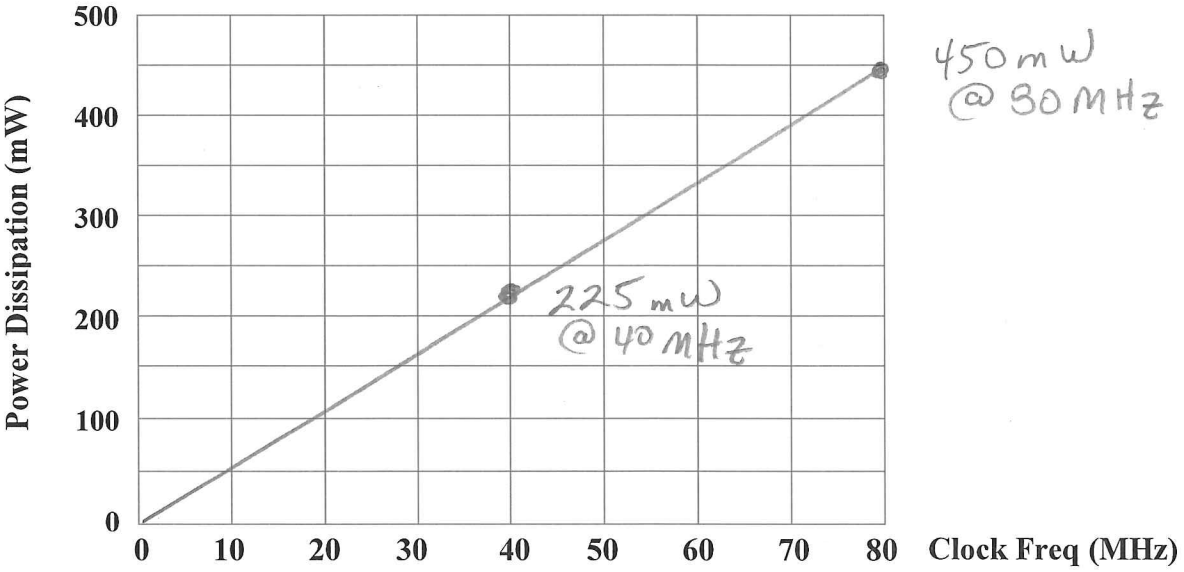
Current limiting resistor = 392 Ω $\qquad$ Resistor power dissipation = 27 mW

3. [4 pts] A particular CMOS microcontroller is designed to operate over a supply voltage range of **1.0 V** to **5.0 V** and at a maximum clock frequency of **80 MHz** (no minimum clock frequency is specified). The *maximum power dissipation* over this range of supply voltage and clock frequency is specified to be **450 milliwatts**.

   (a) [2 pts] Plot the relationship between *power dissipation* and *supply voltage* for this microcontroller (LO 1-29).



   (b) [2 pts] Plot the relationship between *power dissipation* and *clock frequency* for this microcontroller (LO 1-28).



Score: _____ / 20