Homework 2

Due at the beginning of your scheduled lab period

Last Name (Printed): KEY **Lab Div:** ____ **Date:** ____

E-mail: ____@purdue.edu **Signature:** 28 pts max

*Printed copies of these pages along with your original (**hand-annotated, not photocopied**) written solution in the space provided (unless otherwise indicated) are required in order to receive credit. NOTE: The purpose of homework is to provide an opportunity for practicing the kinds of problems you will be asked to solve on quizzes and exams – **copying the work of someone else does not accomplish this.***

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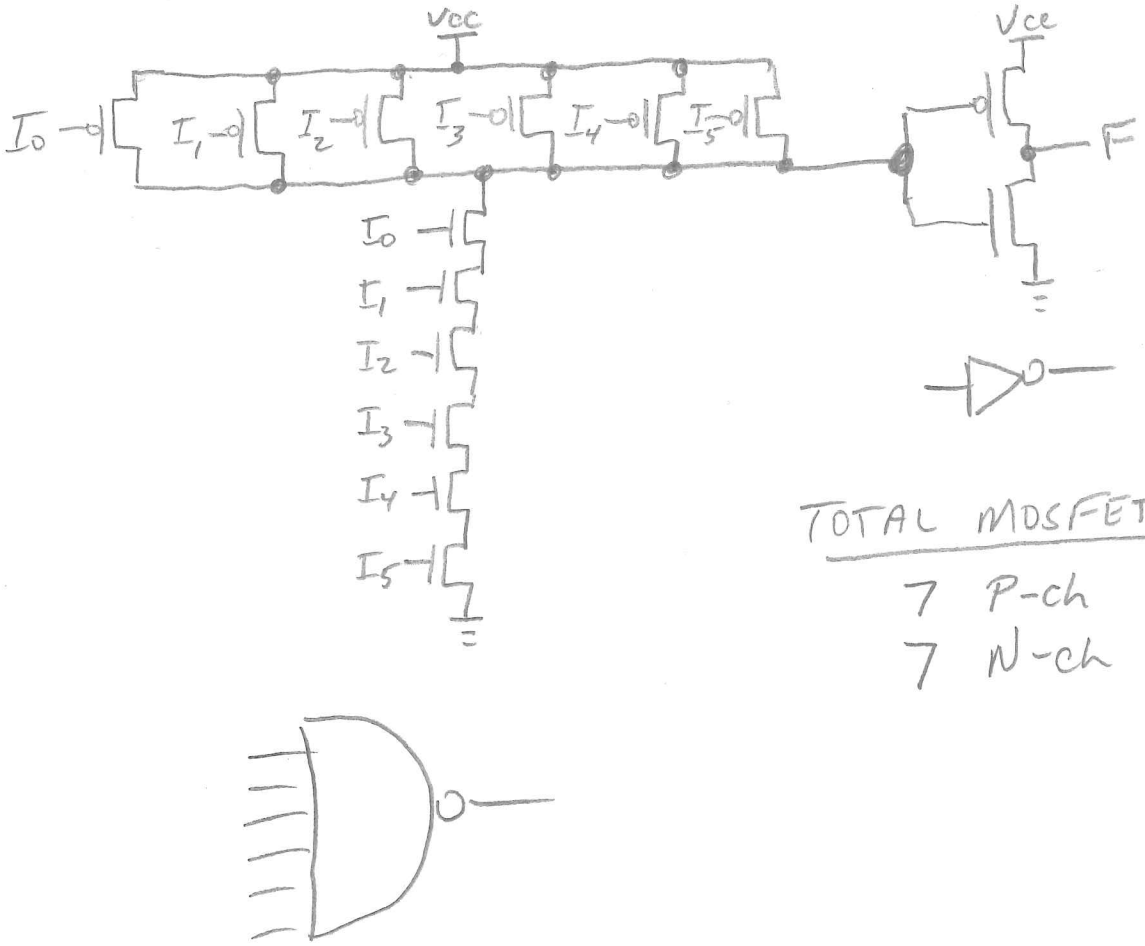
1. [4 pts] Show a MOSFET-level diagram for a 6-input AND gate realized using a 6-input NAND gate followed by an inverter gate. Label the inputs $I_0 \ldots I_5$ and the output F. Be sure to show the power (Vcc) and ground (GND) connections as well. Determine the total number of N- and P-channel MOSFETs required for this realization (LO 1-10).



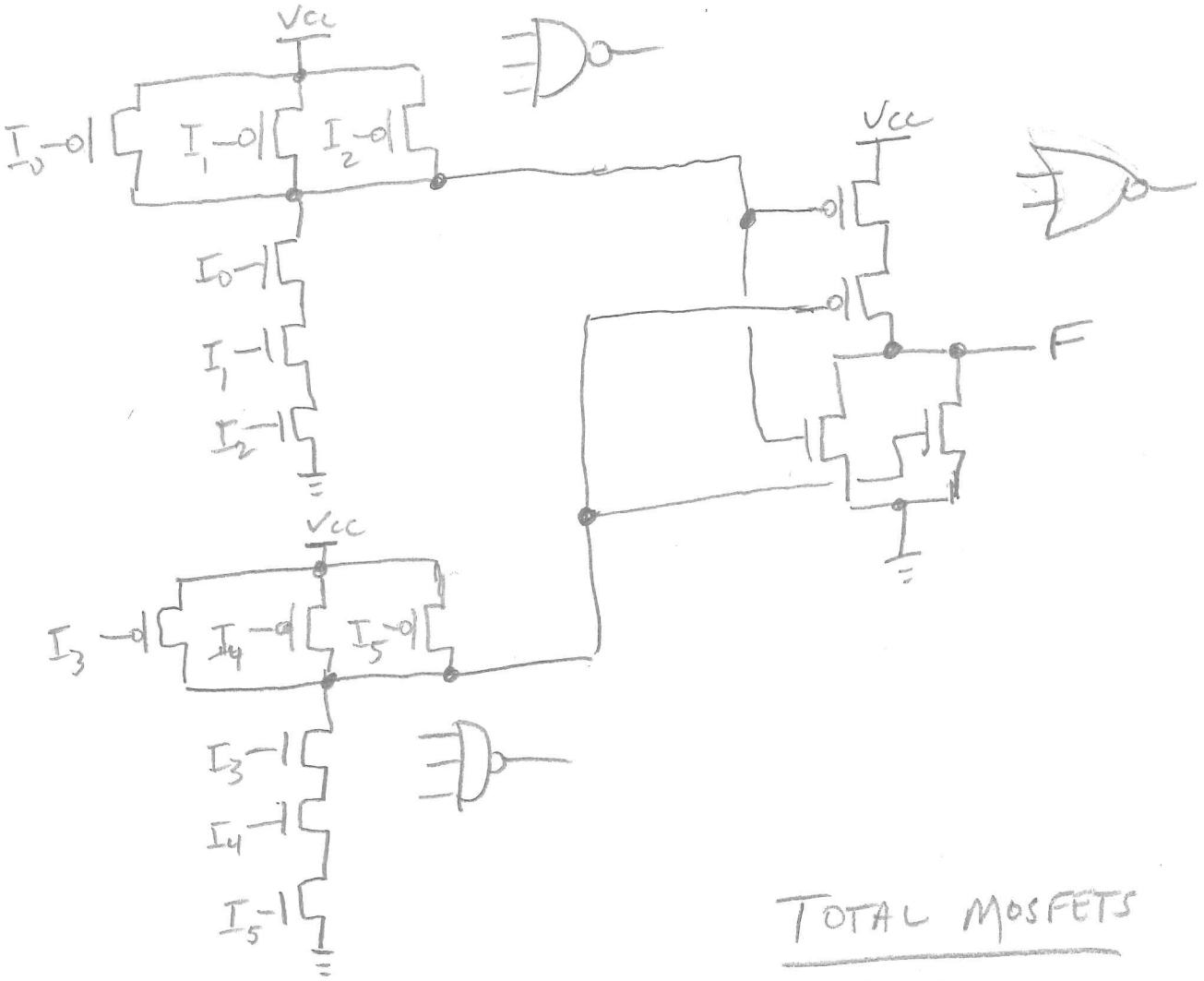
TOTAL MOSFETS

7 P-ch

7 N-ch

8

2. [6 pts] Show a MOSFET-level diagram for a 6-input AND gate realized using two 3-input NAND gates on the first level and a (single) 2-input NOR gate on the second level. Label the inputs $I_0 \ldots I_5$ and the output F. Determine the total number of N- and P-channel MOSFETs required for this realization. Be sure to show the power (Vcc) and ground (GND) connections as well (LO 1-12).



TOTAL MOSFETS

8 P-ch

8 N-ch

3. [4 pts] Read the section on *Fan-In* (5th Ed., pp. 741-742; 4th Ed., pp. 92-93) in the course text. Based on this material, list the tradeoffs between the two 6-input AND functions realized in problems 1 and 2, from a practical point of view. Then provide rationale for which realization would be preferable, based on the tradeoffs you have enumerated.

The additive "on" resistance of series transistors limits the fan-in of CMOS gates, typically to 4 for NOR gates and 6 for NAND gates. The realization in problem 1 pushes this limit, but is still acceptable. The realization in problem 2 is well within the fan-in constraints, but requires 2 more transistors than problem 1. Therefore, the realization in problem 1 would be cheaper and therefore preferable.

4. [4 pts] Given that the P-channel device in the circuit below has **ON** and **OFF** resistances of **50 Ω** and **1 MΩ** (respectively) and that the N-channel device has **ON** and **OFF** resistances of **20 Ω** and **2 MΩ** (respectively), complete the table listing the **output voltages** obtained for each input combination as well as the **power dissipation** (in ***milliwatts***). *Show your calculations* (LOs 1-10 and 1-11).

	A	B	V_{out}	Power Dissipation	Series Req
Noff, Pon	0V	0V	4.999	12.5 μW	2,000,050
both on	0V	5V	1.43	357 mW	50 + 20 = 70
both off	5V	0V	3.33	8.3 μW	3,000,000
Non, Poff	5V	5V	.0001	25.0 μW	1,000,020