# Homework 13 - Key

1. [11 pts] Complete the system control table, below, and derive the system control equations needed to complete Step 5 of Experiment 13. Write out each equation using Verilog syntax.

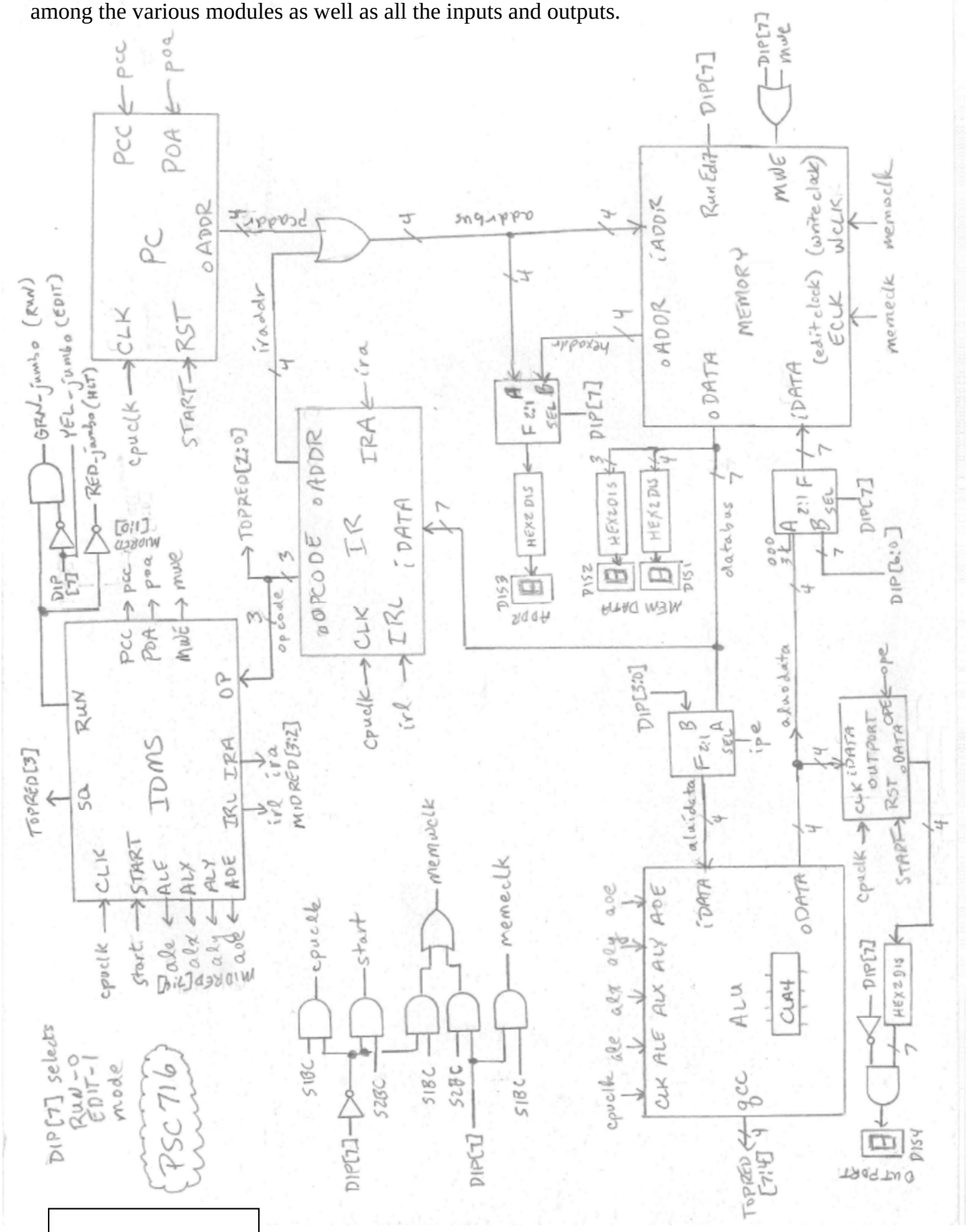
| Decoded State | Instruction Mnemonic | MWE | PCC | POA | IRL | IRA | AOE | ALE | ALX | ALY | IPE | OPE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S0 | — | | H | H | H | | | | | | | |
| S1 | HLT | L | L | d | L | d | d | L | d | d | d | L |
| S1 | LDA | | | | | H | | H | H | | | |
| S1 | ADD | | | | | H | | H | | | | |
| S1 | SUB | | | | | H | | H | | H | | |
| S1 | AND | | | | | H | | H | H | H | | |
| S1 | STA | H | | | | H | H | | | | | |
| S1 | INA | | | | | | | H | H | | H | |
| S1 | OUA | | | | | | H | | | | | H |

Upon execution of **HLT** instruction, all synchronous control signals should be negated (combinational control signals are don't cares).

Equations for each system control equation (written as assignment statements in Verilog):

```
assign MWE = RUN & S[1] & STA;   // synchronous control signals
assign PCC = RUN & S[0];         // should be ANDed with RUN
assign POA = S[0];
assign IRL = RUN & S[0];
assign IRA = S[1] & (LDA | STA | ADD | SUB | AND);
assign AOE = S[1] & (STA | OUA);
assign ALE = RUN & S[1] & (LDA | ADD | SUB | AND | INA);
assign ALX = S[1] & (LDA | AND | INA);
assign ALY = S[1] & (SUB | AND);
assign IPE = S[1] & INA;
assign OPE = RUN & S[1] & OUA;
```

2. [14 pts] Referring to Step 5 of the `lab13_top_template.v` file provided for Experiment 13 on the course website, sketch a **block diagram** of the entire circuit below, showing the interconnections among the various modules as well as all the inputs and outputs.




Score: _____ / 25