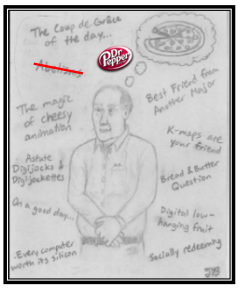
ECE 270 Lab Practical Exam

Study Guide



Procedures

- You must take the LPE during your scheduled lab:
  - 7:30 am labs, exam will be 8:00 am – 10:00 am
  - 11:30 am labs, exam will be Noon – 2:00 pm
  - 2:30 pm labs, exam will be 3:00 pm – 5:00 pm
- There will be NO MAKEUPS or TIME SWAPPING except for those that have been authorized in advance (students requiring accommodations will start at the same time as other students in their assigned division)
- NO REFERENCES will be allowed – you are expected to know basic Verilog syntax
- A "map" of the CPLD board switches and LEDs will be provided, along with a Verilog "top_template" file defining the pin assignments

What to Expect

- You will be required to sign (and abide by) the following academic honesty statement:

  *"In signing this statement, I hereby agree **NOT TO DISCUSS** the contents of this exam with **ANY OTHER STUDENT.** I understand that, if I fail to honor this agreement, I will receive a score of **ZERO** for this exam and be subject to possible disciplinary action."*

- You will be asked to write Verilog code that realizes the specified design
- Each lab division will be assigned a randomly selected problem to solve (from the pool of available questions this semester)
- The LPE counts for 10% of your course grade

How to Prepare for the LPE

- Review the experiment descriptions and solutions that you have assembled in your *Lab Notebook*
- Review the following topics:
  - structure/syntax of Verilog and coding strategies
  - decoders, multiplexers, and priority encoders
  - sequence generators
  - counters, shift registers, and state decoding
  - sequence recognizers
  - two's complement arithmetic, condition code generation, and magnitude comparators (*both signed and unsigned*)
  - carry look-ahead adder realizations
  - BCD full adder/accumulator realization
  - arithmetic logic unit structure and realization
  - personal simple computer realization (*including Verilog modules that have been provided*)

Potential Verilog Modules to Realize

- Lab 9
  - Counters and decoders
  - Sequence generator state machine
- Lab 10
  - Scrolling message display shift register
  - Character sequence generator state machine
- Lab 11
  - Sequence recognizer state machine
  - Random number generator (LFSR)
- Lab 12
  - Adder/subtractor with condition codes
  - Magnitude comparator (signed and unsigned)
  - BCD full adder and accumulator
- Lab 13
  - PC, IR, ALU, IDMS blocks
  - Memory editor

IMPORTANT!

Be sure you understand all the steps completed for each experiment, *including* code that you may have "cut and paste" from the notes and/or code that has been provided.

NOTE: The last day to complete all lab makeups is the office hour session on Monday, April 22, 2019.