OUTCOME #3: "an ability to analyze and design sequential logic circuits."

Multiple Choice – select the single most appropriate response for each question.
Note that "none of the above" MAY be a VALID ANSWER.

Place answers on the supplied BUBBLE SHEET only – nothing written here will be graded.

1. A new type of flip-flop, the BF ("Best Friend"), is described by the following PS-NS table. The characteristic equation for this flip-flop is:
   (A) **Q* = F′•Q + B•Q**
   (B) **Q* = F•Q + B′•Q′**
   (C) **Q* = F•Q′ + B•Q**
   (D) **Q* = F′•Q′ + B′•Q**
   (E) none of the above

2. The excitation required to effect a state transition of the BF flip-flop from "0" to "1" is:
   (A) **B=0, F=d**
   (B) **B=d, F=0**
   (C) **B=1, F=d**
   (D) **B=d, F=1**
   (E) none of the above

BF Flip-Flop PS-NS Table for Questions 1 and 2

B	F	Q	Q*
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

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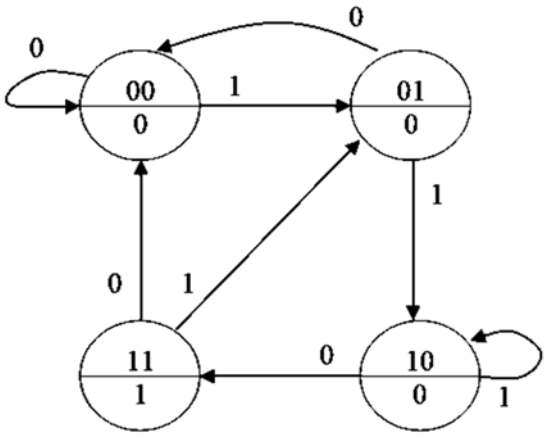
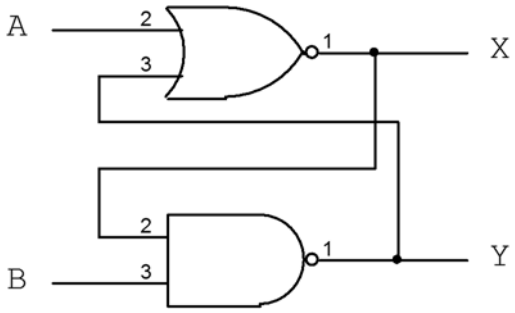
3. Assuming the state machine depicted in the given state transition diagram is initialized to state **00**, the input sequence **1101011100** will cause the following output sequence to be generated:
   (A) **0010000010**
   (B) **0000000000**
   (C) **0010000001**
   (D) **0001000001**
   (E) none of the above

4. The **embedded binary sequence** recognized by this state machine is the pattern:
   (A) **001**
   (B) **011**
   (C) **100**
   (D) **110**
   (E) none of the above

State Transition Diagram for Questions 3 and 4



The following circuit applies to questions 5 through 9 (write the NS equations, complete the PS-NS table, and draw the state transition diagram before answering the questions):



X* = _____

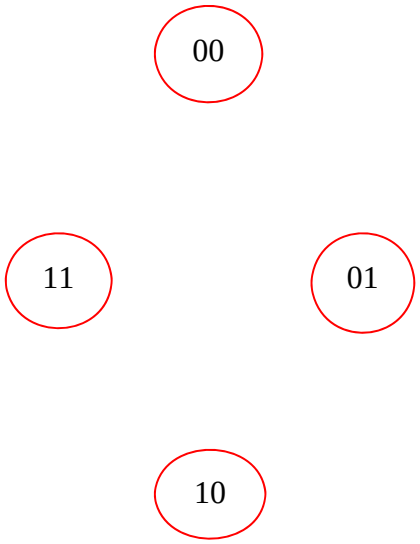
Y* = _____

5. The next state equation for Y is:
   (A) **Y* = B′ · X′**
   (B) **Y* = B′ + X′**
   (C) **Y* = B′ + A + Y**
   (D) **Y* = B′ · (A +Y)**
   (E) none of the above

6. State **X=0, Y=1** is:
   (A) an initial state
   (B) a final state
   (C) a trap state
   (D) an accepting state
   (E) none of the above

7. The following state **cannot** occur:
   (A) **X=0, Y=0**
   (B) **X=0, Y=1**
   (C) **X=1, Y=0**
   (D) **X=1, Y=1**
   (E) none of the above

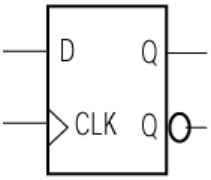
X	Y	A	B	X*	Y*
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		

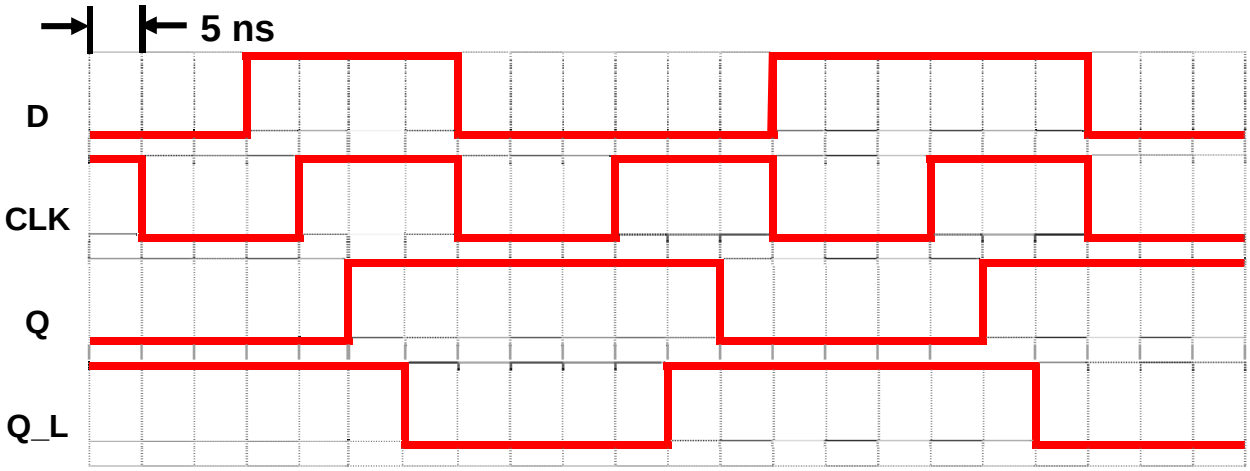


8. Based on the state transition diagram, if this feedback sequential circuit is initialized to state **X=0, Y=0** and combination **A=0, B=0** is (continuously) applied to its inputs, the (steady state) output combination will be:
   (A) **X=0, Y=0**
   (B) **X=0, Y=1**
   (C) **X=1, Y=0**
   (D) **X=1, Y=1**
   (E) unpredictable

9. Based on the state transition diagram, if this feedback sequential circuit is initialized to state **X=0, Y=0** and combination **A=0, B=1** is (continuously) applied to its inputs, the outputs will:
   (A) be unpredictable
   (B) stay at **X=0, Y=0**
   (C) change to **X=1, Y=1**
   (D) "oscillate" between **X=0, Y=0** and **X=1, Y=1**
   (E) none of the above

The following figure applies to questions 10 through 13:





10. The **nominal setup time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

    (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

11. The **nominal hold time** provided for the D flip-flop, based on the excitation signals (D and CLK) depicted in the timing chart, is:

    (A) 20 ns (B) 15 ns (C) 10 ns (D) 5 ns (E) none of the above

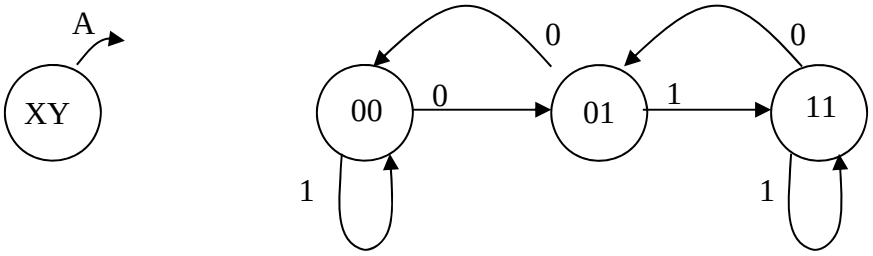
12. The $t_{PLH(C \rightarrow Q)}$ of the D flip-flop is:

    (A) 5 ns (B) 10 ns (C) 15 ns (D) 20 ns (E) none of the above

13. The $t_{PHL(C \rightarrow Q)}$ of the D flip-flop is:

    (A) 20 ns (B) 15 ns (C) 10 ns (D) 5 ns (E) none of the above

The following state transition diagram applies to questions 14 through 16:



14. If designed for **minimum <u>cost</u>**, the next state equation for **X** is:
    (A) **X* = X + Y**
    (B) **X* = A·Y**
    (C) **X* = Y + X·A + X′·A′**
    (D) **X* = X + (X′+Y)·A′**
    (E) none of the above

15. If designed for **minimum <u>cost</u>**, the next state equation for **Y** is:
    (A) **Y* = X·A**
    (B) **Y* = A·Y**
    (C) **Y* = Y + X·A + X′·A′**
    (D) **Y* = X + Y·A + Y′·A′**
    (E) none of the above

16. Designing a state machine based on **minimum <u>cost</u>** means:
    (A) there are no “don’t cares” in the excitation equations
    (B) there are no “don’t cares” in the next state equations
    (C) there are no “don’t cares” in the output equations
    (D) all of the above
    (E) none of the above

17. As a contestant on the hit TV series ***Digital Dynasty***, you have been asked to “digitally dual” with your BECEFE (best ECE friend *evah*) over the phenomenon of metastability. You confidently explain that the **<u>next state</u>** of an edge-triggered D flip-flop will most likely be **<u>random</u>** if:
    (A) its minimum setup time requirement is not met
    (B) its minimum hold time requirement is not met
    (C) its minimum clock pulse width requirement is not met
    (D) all of the above
    (E) none of the above

The following Verilog program applies to questions 18 through 21 (complete the PS-NS table and draw the state transition diagram before answering the questions):

```
module mystery_seq1(CLK, Q);
  input wire CLK;
  output reg [2:0] Q;

  reg [2:0] next_Q;

   always @ (posedge CLK) begin
    Q <= next_Q;
  end

 always @ (Q) begin
   next_Q[2] =  Q[1]&~Q[0] | Q[2]&~Q[1];
   next_Q[1] = ~Q[2]&~Q[0] | Q[2]& Q[0];
   next_Q[0] =  Q[1]& Q[0] | Q[2]&~Q[1];
  end
endmodule
```

Q2	Q1	Q0	Q2*	Q1*	Q0*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

18. The number of states in the **periodic sequence** is:

    (A) 1 (B) 3 (C) 6 (D) 8 (E) none of these

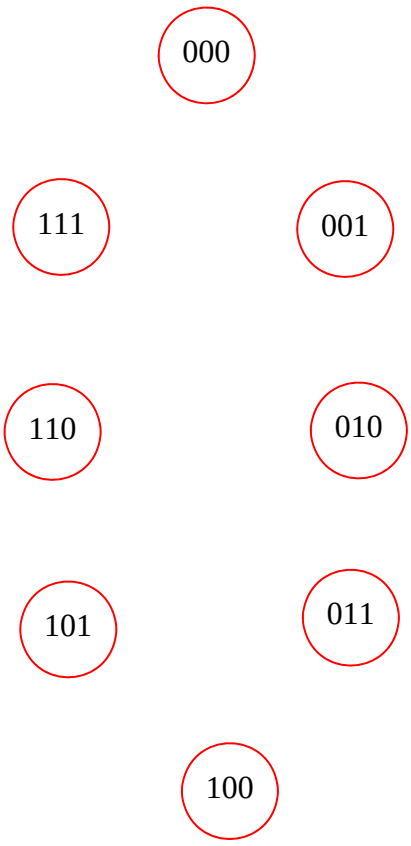
19. The **maximum** number of clock cycles needed for **self-correction** is:

    (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

20. The **number of <u>state variables</u>** needed to **uniquely decode** each of the states in the periodic sequence is:

    (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

21. The "mystery sequencer" is a:
    (A) ring counter
    (B) binary UP counter
    (C) Gray code counter
    (D) switchtail (Johnson) counter
    (E) none of the above



The following Verilog program applies to questions 22 through 25 (complete the PS-NS table and draw the state transition diagram before answering the questions):

```
module mystery_seq2(CLK, Q);
  input wire CLK;
  output reg [2:0] Q;

  reg [2:0] next_Q;

   always @ (posedge CLK) begin
    Q <= next_Q;
  end

 always @ (Q) begin
   next_Q[2] =  Q[1] & (Q[2] | Q[0]);
   next_Q[1] =  Q[0];
   next_Q[0] = ~Q[2];
  end
endmodule
```

Q2	Q1	Q0	Q2*	Q1*	Q0*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

22. The number of states in the **periodic sequence** is:

    (A) 1 (B) 3 (C) 6 (D) 8 (E) none of these

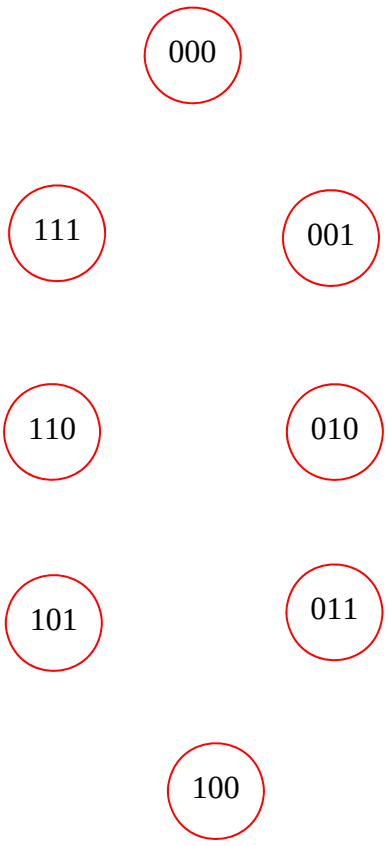
23. The **maximum** number of clock cycles needed for **self-correction** is:

    (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

24. The **number of <u>state variables</u>** needed to **uniquely decode** each of the states in the periodic sequence is:

    (A) 0 (B) 1 (C) 2 (D) 3 (E) none of these

25. The "mystery sequencer" is a:
    (A) ring counter
    (B) binary UP counter
    (C) Gray code counter
    (D) switchtail (Johnson) counter
    (E) none of the above



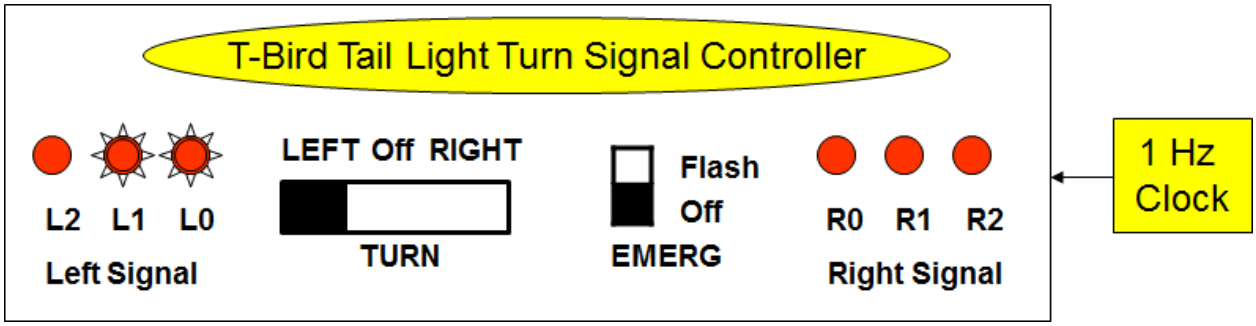
The following Verilog program applies to questions 26 and 27:

```
module pmbc(CLK, D, Q);
  input wire CLK;
  input wire [3:0] D;
  output reg [3:0] Q;
  reg [3:0] next_Q;

  always @ (posedge CLK) begin
    Q <= next_Q;
  end

  always @ (Q) begin
    if (Q == D) begin
      next_Q = 4'b0000;
    end
    else begin
      next_Q[0] = ~Q[0];
      next_Q[1] =  Q[1] ^  Q[0];
      next_Q[2] =  Q[2] ^ (Q[1] & Q[0]);
      next_Q[3] =  Q[3] ^ (Q[2] & Q[1] & Q[0]);
    end
  end
endmodule
```

26. To create a (4-bit) **binary** (i.e. **modulo 16**) counter, the data inputs D[3:0] should be:
    (A) **0 0 0 0**
    (B) **1 0 0 1**
    (C) **1 0 1 0**
    (D) **1 1 1 1**
    (E) none of the above

27. To create a **BCD** (i.e. **modulo 10**) counter, the data inputs D[3:0] should be:
    (A) **0 0 0 0**
    (B) **1 0 0 1**
    (C) **1 0 1 0**
    (D) **1 1 1 1**
    (E) none of the above

The following figure and description applies to questions 28 through 30:



Illustrated above is an automotive turn signal where each "tail light" consists of three LEDs, illuminated in a "building dot" mode to indicate the turn direction. The "left" or "right" turn direction is selected by a 3-position (single pole) switch with a "center off" position (like a "real" automotive turn signal). The left or right building dot sequence should continuously repeat as long as the LEFT or RIGHT input is asserted (note these inputs are *mutually exclusive* based on the physical construction of the switch); when LEFT and RIGHT are both negated (i.e., the TURN switch is in the "center off" position), all LEDs should be off. An "emergency flash" mode (in which all the tail lights alternate between the on and off states) is controlled by the EMERG input. If the "emergency flash mode" is selected, the six lights should alternate between the "all on" and "all off" states and the LEFT and RIGHT inputs should be ignored.

28. If designed as a **Mealy model** where the **minimum number of state variables possible** is used (per solution shown in the practice homework), the total number of **macrocells** needed to realize the turn signal controller will be:
    (A) **3**
    (B) **6**
    (C) **8**
    (D) **9**
    (E) none of the above

29. If designed as a **Moore model** where the **minimum number of state variables possible** is used (per solution shown in textbook on pp. 570-576), the total number of **macrocells** needed to realize the turn signal controller will be:
    (A) **3**
    (B) **6**
    (C) **8**
    (D) **9**
    (E) none of the above

30. If designed as a **Moore model** where the **output variables are the state variables**, the total number of **unused states** will be:
    (A) **56**
    (B) **64**
    (C) **256**
    (D) **512**
    (E) none of the above