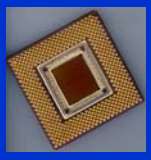

Introduction to Digital System Design

Exam #3 Review Notes

ECE 270 Exam #3

- Date: Tuesday, March 26
- Time: 6:30-7:30 PM
- Place: PHYS 112, PHYS 114, FRNY G140
- Material covered: Module 3

IMPORTANT:

- ✓ Know your SEATING and ROOM ASSIGNMENTS
- ✓ Bring your PUID card (must be presented when you turn in your exam)
- ✓ Bring a #2 pencil and a good eraser

Restrictions

- Closed book and notes
- Use of TI-30II XS calculator allowed
- Electronic devices may not be used
- Earphones/earbuds may not be worn
- Cell phones must be turned off and put away
- Caps may not be worn during the exam
- Makeup exams must be scheduled before the evening exam occurs – turn in an "Early Makeup Exam Request Form" (on course web site under Exam Information) at least one week prior to the scheduled exam

Learning Outcomes

A student who successfully fulfills the course requirements will have demonstrated:

1. an ability to analyze and design CMOS logic gates
2. an ability to analyze and design combinational logic circuits
3. an ability to analyze and design sequential logic circuits
4. an ability to analyze and design computer logic circuits
5. an ability to realize, test, and debug practical digital circuits

Learning Outcome Assessment

- *You will earn 1% bonus credit for each course outcome you successfully demonstrate*
  - For Outcomes 1-4, basic competency will be assessed based on hourly exam questions, for which a minimum score of 60% will be required
  - For Outcome 5, a score of 60% on each lab experiment *or* a score of 60% on the Lab Practical Exam will be required for successful demonstration

Grade Determination

90% to 100%	A-, A, A+
80% to 90%	B-, B, B+
70% to 80%	C-, C, C+
60% to 70%	D-, D, D+
< 60%	F

Bonus Exercises "BON"	Δ_1%
Class Participation (iClickers) "CLICK"	4.0%
Homework Exercises "HW" (13 @ 0.77%)	10.0%
Lab Experiments "EXP" (13 @ 1.5%)	19.5%
Lab Quizzes "QZ" (13 @ 0.5%)	6.5%
Lab Practical Exam "LPE"	10.0%
Outcome Assessment Exams "POA" (4 @ 12.5%)	50.0%
Outcome Demonstration Bonus "LODBN" (5 @ 1%)	Δ_2%
	100+Δ%

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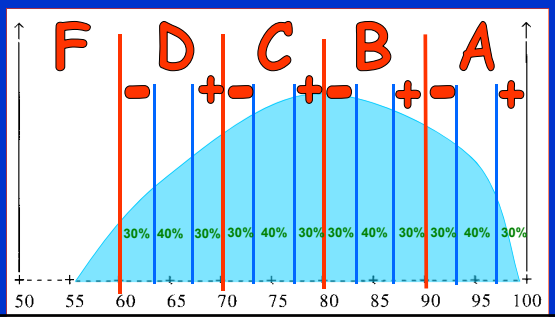
Grade Determination

- Calculation of Raw Weighted Percentage:

$$RWP = \frac{\sum_i WGT_i \times SCORE_i}{\sum_i WGT_i} \times 100$$

- RWP then "curved" (mean-shifted) with respect to upper percentile of class, yielding the Normalized Weighted Percentage (NWP)
- Windowed Standard Deviation (WSD) for class is calculated based on statistics of "middle" 90% of class
- Cutoff Width Factor (CWF) is then *max*(WSD,10), i.e., the *nominal cutoffs* are 90-80-70-60 for A-B-C-D, respectively

± Grading Visualization (CWF=10)



Learning Objectives

As part of faculty participation in the Purdue IMPACT initiative, a detailed set of learning objectives have been developed based on Bloom's taxonomy

The goal is to *teach intentionally* and *test intentionally* based on the stated outcomes and objectives

A list of learning objectives is included in the Lecture Summary Notes for each outcome as well as the Class Presentation Slides

Use the list of learning objectives as a guide for reviewing the lecture material and homework problems.

"Best Way to Study for Exam"

- *Re-work* and *fully understand* all homework and example problems worked in class
- Methodically review the entire set of *Learning Objectives* for Outcome 3 and verify you can perform each cognitive domain action
- Make effective use of all the instructional resources available
  - practice exams
  - textbook / practice problems

Possible Questions

- ✓ Describe the difference between a latch and a flip-flop
- ✓ Identify all latch and flip-flop timing parameters
- ✓ Describe the phenomenon of metastability
- ✓ Perform basic sequential circuit analysis (e.g., an S-R latch)
  - ➢ Write next state equations
  - ➢ Construct a present state - next state table
  - ➢ Construct a state transition diagram
  - ➢ Construct a timing chart
- ✓ Analyze sequential circuits containing S-R, D, and T flip-flops

Possible Questions

- ✓ Describe the difference between a Mealy Model and a Moore Model
- ✓ Draw a state transition diagram using either a Mealy Model or a Moore Model
- ✓ Synthesize the characteristic equation of any type of flip-flop (S-R, D, T) from any other type of flip-flop
- ✓ Design a clocked synchronous state machine using edge-triggered D flip-flops
- ✓ Identify all the macrocell-related attribute suffixes in a complex PLD
- ✓ Write a Verilog program that realizes a clocked synchronous state machine (sequence generator, counter/shift register, sequence recognizer)

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