LEARNING OUTCOME #1: "an ability to analyze and design CMOS logic gates."

1. D
2. C
3. D
4. C
5. A
6. C
7. D
8. C
9. D
10. B
11. C
12. B
13. D
14. B
15. A
16. B
17. C
18. C
19. C
20. B
21. B
22. A
23. C
24. A
25. C
26. B
27. A
28. A
29. C
30. B

Question 1: 30% of the students got this question wrong the last time it was asked – don't be one of them! Three iterative divisions of $(72)_{10}$ by 8 yield remainders of 0, 1, 1 (respectively), but don't forget to reverse the order of the remainders to produce the converted number $(110)_8$.

Questions 18-22:

(18) This is the "all off" case, so there is a total of 60 μA of OD leakage current plus 40 μA of I_{IH} flowing through the 1000 Ω resistor, yielding a voltage drop relative to 5 V of 0.1 V (= 4.9V) at the inverter input.

(19) Ron of the OD NAND can be calculated based on the V_{OLmax} (0.5 V) and I_{OLmax} (5 mA) given, which is 100 Ω. The Rmin calculation is based on the "worst case" (from the NAND's point of view) of sinking no more than 5 mA with 4.5 V dropping across it. Therefore, Rmin is 900 Ω. Clearly, Rmax is much greater than Rmin, so we can safely assume that if R = 1000 Ω (shown in circuit), then $R_{min} < R < R_{max.}$

(20) Because the pull-up R in the circuit is greater than Rmin, the voltage drop will be greater across R than in the "worst case" cited above, so the voltage at the inverter input will be less than the specified V_{OLmax} (but greater than zero).

(21) By similar argument, the current sunk will also be less than the specified I_{OLmax} (again, because R is greater than Rmin).

(22) Here the current sunk is split between three OD NAND gates, so it will be less (per gate) than the case in which it is only split two ways, as detailed in the lecture notes.

Questions 25-26: Based on the Vout waveform shown, the fall time of the OD gate is 10 ns and its rise time is 30 ns. R is given as 1500 Ω. The C estimate is based on the rise time, i.e. RC = 30 ns from which a value of 20 pF is obtained. The Ron estimate is based on the fall time, i.e. RC = 10 ns where C = 20 pF (calculated above) from which a value of 500 Ω for Ron is obtained.

Questions 27-28: See the practice homework solution for problem 11.

Questions 29-30: For the purpose of this course, we are modeling MOSFETs as voltage-controlled impedances. Recall that a potential on the "G" terminal on a MOSFET relative to its "S" terminal (V_{GS}) is what turns the device on/off. For question 29, the "S" terminals are referenced to ground; therefore, if Vin is 5 V, the N-channel device will start to turn on while the P-channel will stay off…but, as the N-channel device turns on, the "S" terminal reference raises above ground potential, thereby decreasing V_{GS} which will tend to shut the N-channel device off. In theory, this "tug-of-war" between turning the transistor on while simultaneously turning it off will "settle" at half the supply voltage (2.5 V). If that is the case, the potential of 2.5 V at the S terminals will cause 2.5 mA to be sourced through the 1000 Ω resistor.

Based on similar arguments, the circuit shown for question 30 (referenced to 5 V) will cause the P-channel device to start turning on when Vin is ground (the N-channel device will stay off). But as the P-channel device turns on, its "S" terminal reference becomes lower than 5 V, which will tend to shut off the P-channel device. Once again, the "tug-of-war" (in theory) settles at 2.5 V, causing 2.5 mA to be sunk through the 1000 Ω resistor.