OUTCOME #1: "an ability to analyze and design CMOS logic gates."

Multiple Choice – select the single most appropriate response for each question.
Note that "none of the above" MAY be a VALID ANSWER.

Place answers on the supplied BUBBLE SHEET only – nothing written here will be graded.

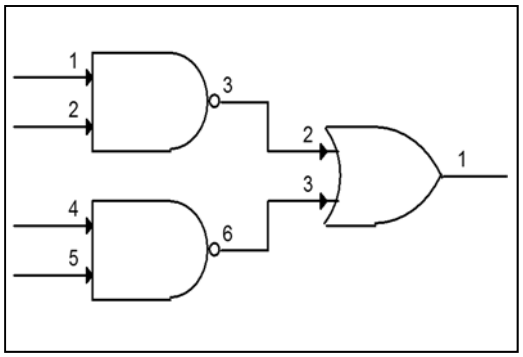
1. One of your *former* best friends from another major (BFFAM) decided to insult you by telling his (other) friends that your IQ had assumed room temperature, i.e. $(72)_{10}$. To put a better spin on this unfortunate reality, in your Faceplant posts you advertise your IQ to prospective employers as a base 8 number. **Expressed as a base 8 number, $(72)_{10}$ is:**

   (A) $(72)_8$ (B) $(90)_8$ (C) $(108)_8$ (D) $(110)_8$ (E) none of these

2. The **nominal (minimum) case** for the **outputs of logic family "A"** to be able to successfully drive **the inputs of logic family "B"** is:
   (A) $\text{fanout}_{A\to B} \geq 0$ and $\text{DCNM}_{A\to B} > 1$
   (B) $\text{fanout}_{A\to B} \leq 0$ and $\text{DCNM}_{A\to B} < 1$
   (C) $\text{fanout}_{A\to B} \geq 1$ and $\text{DCNM}_{A\to B} > 0$
   (D) $\text{fanout}_{A\to B} \leq 1$ and $\text{DCNM}_{A\to B} < 0$
   (E) none of the above

3. The **high impedance state** of a **tri-state buffer** is created by:
   (A) turning "on" both the PMOS and the NMOS transistors at the output of the buffer
   (B) turning "on" the PMOS transistor and turning "off" the NMOS transistor at the output of the buffer
   (C) turning "off" the PMOS transistor and turning "on" the NMOS transistor at the output of the buffer
   (D) turning "off" both the PMOS and the NMOS transistors at the output of the buffer
   (E) none of the above

4. A level of **2-input NAND gates** followed by a **2-input OR gate** is logically equivalent to:
   (A) a 4-input AND gate
   (B) a 4-input OR gate
   (C) a 4-input NAND gate
   (D) a 4-input NOR gate
   (E) none of the above



Based on a growing **consensus** among your BFFAMs (see question 1), you get the bright idea that you might be able to earn back some respect among your Faceplant friends by working out the proof to the **Consensus Theorem** (specifically, its ***dual***). **Identify the theorems applied in each step of the proof, for questions 5 through 7, below.**

Dual of Consensus Theorem: $(X + Y) \bullet (X' + Z) \bullet (Y + Z) = (X + Y) \bullet (X' + Z)$

BFFAM's Proof:

LHS: $(X + Y) \bullet (X' + Z) \bullet (Y + Z)$

Step 1: $= (X + Y) \bullet (X' + Z) \bullet (Y + Z + 0)$

Step 2: $= (X + Y) \bullet (X' + Z) \bullet (Y + Z + X \bullet X')$

Step 3: $= (X + Y) \bullet (X' + Z) \bullet (X + Y + Z) \bullet (X' + Y + Z)$

Step 4: $= (X + Y) \bullet (X + Y + Z) \bullet (X' + Z) \bullet (X' + Y + Z)$

Step 5: $= (X + Y) \bullet (X' + Z)$ Q.E.D.

5. The switching algebra theorem used to obtain the expression in **Step 1** is:
   (A) identity
   (B) null elements
   (C) complements
   (D) involution
   (E) none of the above

6. The switching algebra theorem used to obtain the expression in **Step 3** is:
   (A) commutivity
   (B) complements
   (C) distributivity
   (D) combining
   (E) none of the above

7. The switching algebra theorem used to obtain the expression in **Step 5** is:
   (A) commutivity
   (B) combining
   (C) distributivity
   (D) covering
   (E) none of the above

The following table applies to questions 8 through 11:

Table 1. DC Characteristics of a Hypothetical Logic Family.

$V_{CC} = 5$ V	$V_{OH} = 4.50$ V	$V_{OL} = 0.50$ V	$V_{IH} = 3.00$ V	$V_{IL} = 2.00$ V
$V_{TH} = (V_{OH} - V_{OL})/2$	$I_{OH} = -5.0$ mA	$I_{OL} = 10$ mA	$I_{IH} = 50$ μA	$I_{IL} = -0.1$ mA

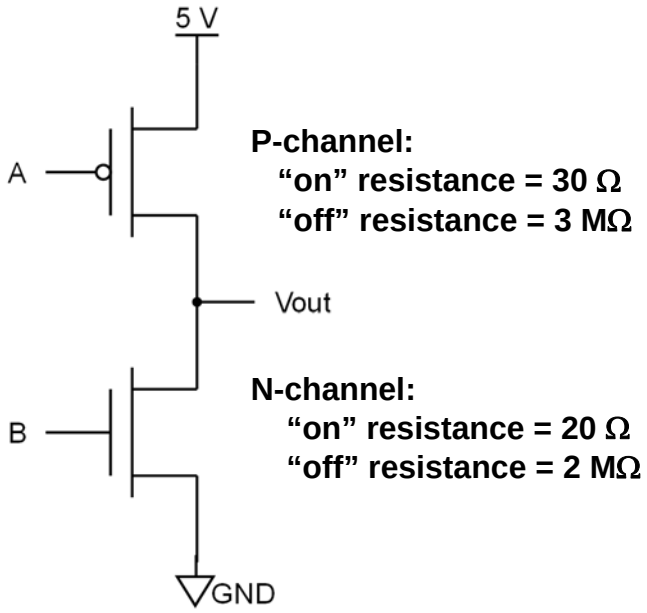
8. The ***DC noise margin*** for this logic family is:
   (A) 0.50 V
   (B) 1.00 V
   (C) 1.50 V
   (D) 2.00 V
   (E) none of the above

9. The ***practical fanout*** for this logic family is:
   (A) 1
   (B) 5
   (C) 10
   (D) 100
   (E) none of the above

10. When interfacing an **LED** that has a **forward voltage of 2.0 V** to this logic family in a ***current sinking*** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:
   (A) 200 Ω
   (B) 250 Ω
   (C) 500 Ω
   (D) 600 Ω
   (E) none of the above-

11. When interfacing an **LED** that has a **forward voltage of 2.0 V** to this logic family in a ***current sourcing*** configuration, **maximum brightness** will be achieved (within the rated specifications) using a current limiting resistor of the value:
   (A) 200 Ω
   (B) 250 Ω
   (C) 500 Ω
   (D) 600 Ω
   (E) none of the above

The following circuit applies to questions 12 through 15:



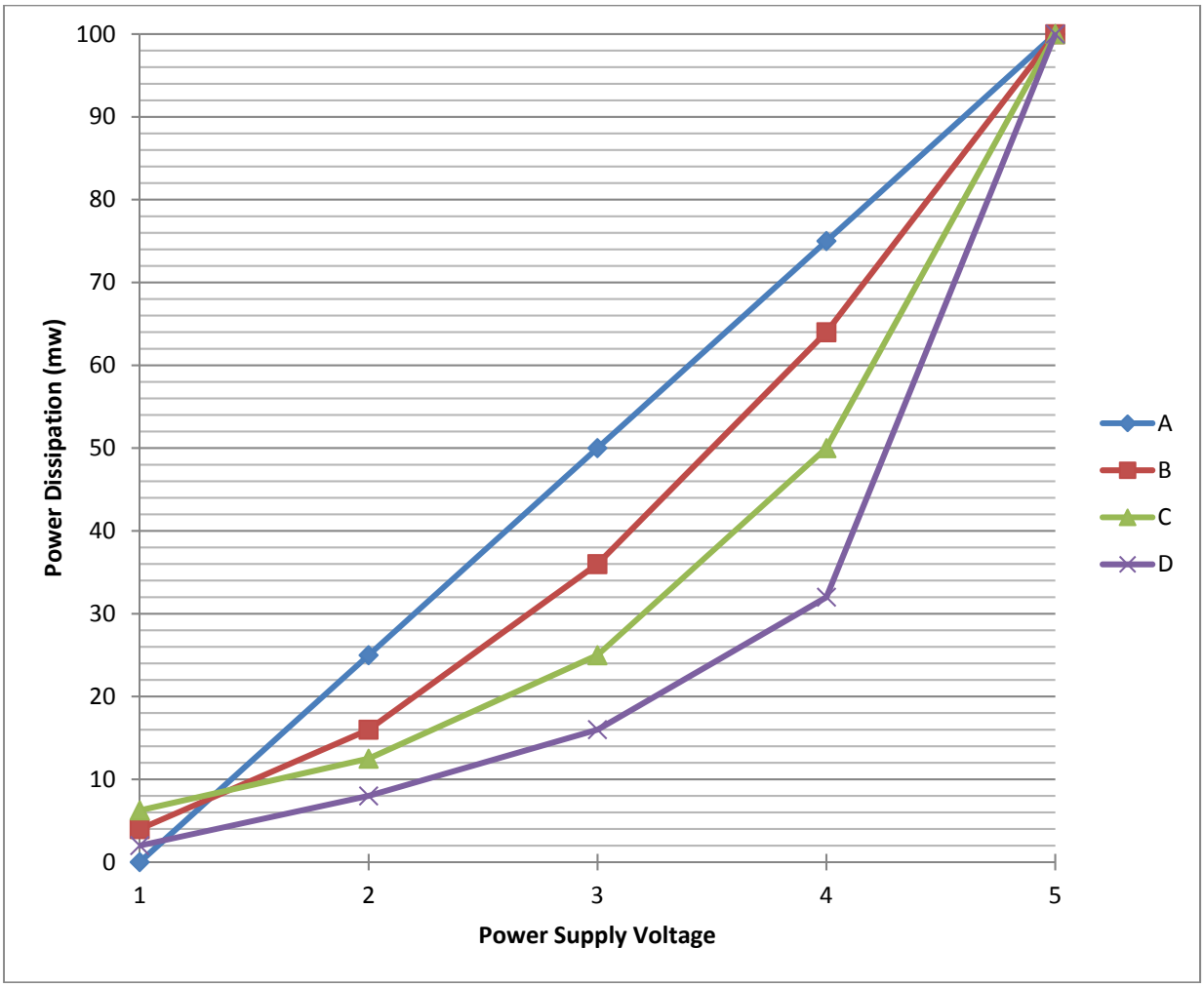
12. When **A = 0 V** and **B = 5 V,** the **potential** at **Vout** will be:
    (A) 0.00 V
    (B) 2.00 V
    (C) 3.00 V
    (D) 5.00 V
    (E) none of the above

13. When **A = 0 V** and **B = 5 V,** the amount of **power dissipate**d by this circuit is:
    (A) 5 µW
    (B) 25 µW
    (C) 250 mW
    (D) 500 mW
    (E) none of the above

14. When **A = 5 V** and **B = 0 V,** the **potential** at **Vout** will be:
    (A) 0.00 V
    (B) 2.00 V
    (C) 3.00 V
    (D) 5.00 V
    (E) none of the above

15. When **A = 5 V** and **B = 0 V,** the amount of **power dissipated** by this circuit is:
    (A) 5 µW
    (B) 25 µW
    (C) 250 mW
    (D) 500 mW
    (E) none of the above

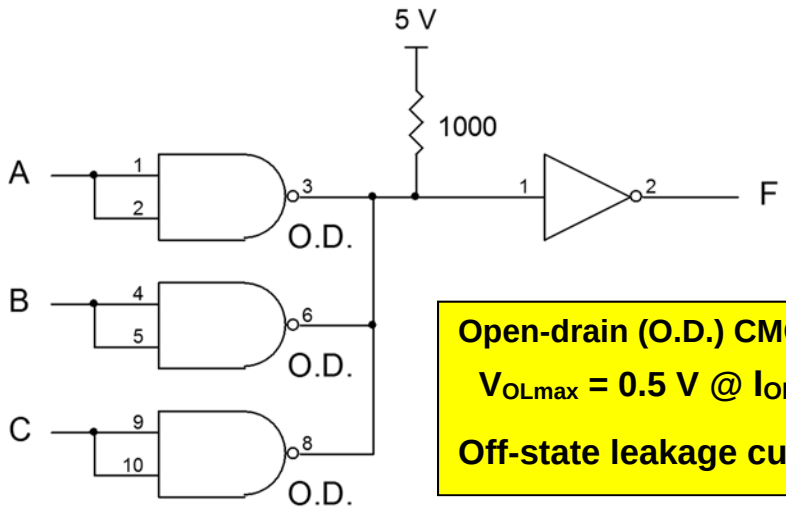
The following figure applies to questions 16 and 17:



16. The **curve** that depicts **power dissipation** of a CMOS circuit as a function of **power supply voltage** (over the range of 1 to 5 volts) is:
    (A) A
    (B) B
    (C) C
    (D) D
    (E) none of the above

17. If the **power supply voltage** of a CMOS circuit is **reduced** from **5.0 volts** to **2.0 volts**, its **power dissipation** will be **reduced by**:
    (A) 4 mW
    (B) 16 mW
    (C) 84 mW
    (D) 96 mW
    (E) none of the above

The following circuit applies to questions 18 through 22:



CMOS Inverter:

I_{IH} = +40 μA
I_{IL} = - 40 μA
V_{IHmin} = 3.5 V
V_{ILmax} = 1.5 V

Open-drain (O.D.) CMOS NAND gates:

V_{OLmax} = 0.5 V @ I_{OLmax} = +5 mA

Off-state leakage current = +20 μA

18. When **A = 0 V, B = 0 V,** and **C = 0 V,** the voltage at the **inverter input** will be:

(A) 0.0 V (B) 0.1 V (C) 4.9 V (D) 5.0 V (E) none of these

19. Based on the **open-drain NAND gate specifications** provided, the value of pull-up resistor shown in the circuit (1000 Ω) is:

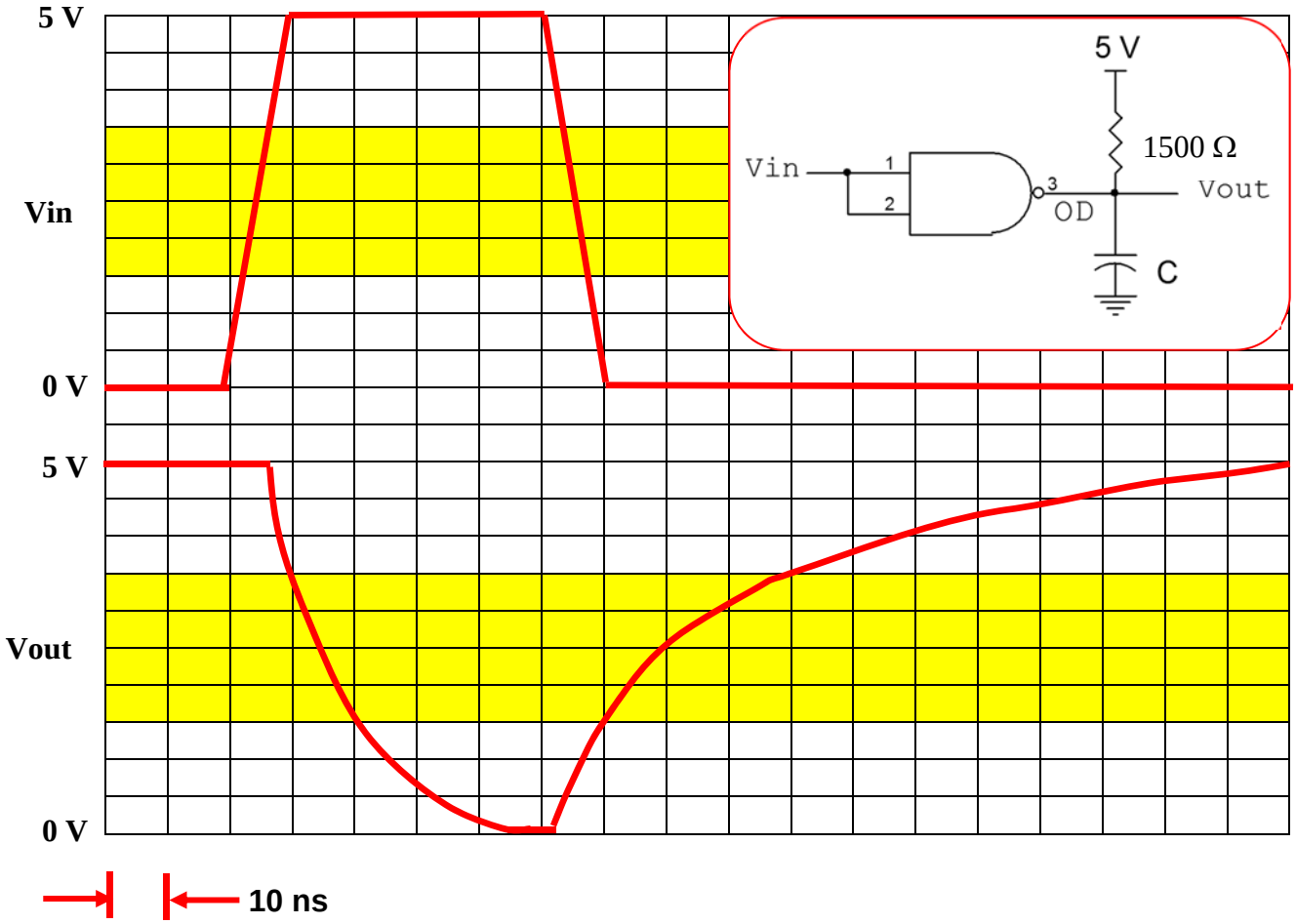
(A) < R_{min} (B) R_{min} (C) R_{min} < R < R_{max} (D) R_{max} (E) > R_{max}

20. When **A = 5 V, B = 0 V,** and **C = 0 V,** the voltage at the **inverter input** will be:
    (A) zero
    (B) greater than zero but less than the specified V_{OLmax}
    (C) exactly the specified V_{OLmax}
    (D) greater than the specified V_{OLmax}
    (E) none of the above

21. When **A = 5 V, B = 0 V,** and **C = 0 V,** the **current sunk** by the active open-drain NAND gate will be:
    (A) zero
    (B) greater than zero but less than the specified I_{OLmax}
    (C) exactly the specified I_{OLmax}
    (D) greater than the specified I_{OLmax}
    (E) none of the above

22. When **A = 5 V, B = 5 V,** and **C = 5 V,** the **current sunk** by <u>each</u> active open-drain NAND gate will be:
    (A) **less than** the case in which **A = 5 V, B = 5 V,** and **C = 0 V**
    (B) **more than** the case in which **A = 5 V, B = 5 V,** and **C = 0 V**
    (C) exactly the specified I_{OLmax}
    (D) greater than the specified I_{OLmax}
    (E) none of the above

The following figure applies to questions 23 through 26 **(each square is 10 ns):**



23. The **rise time (t_{TLH})** for the open-drain NAND gate is approximately:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of these

24. The **fall propagation delay (t_{PHL})** for the open-drain NAND gate is approximately:

(A) 10 ns (B) 20 ns (C) 30 ns (D) 40 ns (E) none of these

25. **Estimate** the value of the **capacitor** (C) based on the RC time constant:

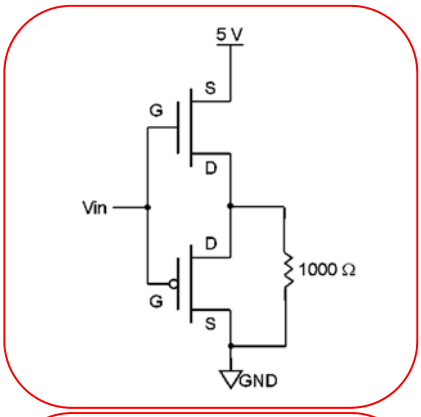
(A) 10 pF (B) 15 pF (C) 20 pF (D) 30 pF (E) none of these

26. **Estimate** the **ON resistance** of the open-drain NAND gate based on the RC time constant:

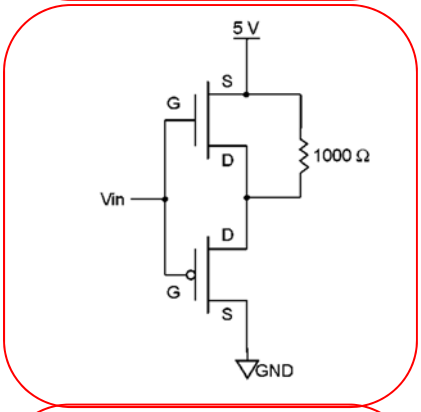
(A) 100 Ω (B) 500 Ω (C) 667 Ω (D) 1000 Ω (E) none of these

For questions 27-30, assume the **"on" resistance** of each MOSFET is **10 Ω** and the **"off" resistance** is **1 MΩ**, and that the **N-** and **P-channel** MOSFETs in each circuit have been **randomly** wired together **as shown.**

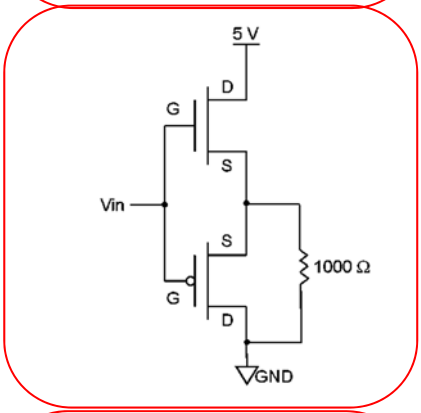
27. The amount of current this circuit can **source** to a 1000 Ω load (referenced to GND) is approximately:
    (A) 0 **mA** regardless of Vin
    (B) 2.5 mA if Vin is 0 V
    (C) 2.5 mA if Vin is 5 V
    (D) 5.0 mA regardless of Vin
    (E) none of the above



28. The amount of current this circuit can **sink** from a 1000 Ω load (referenced to 5 V) is approximately:
    (A) 0 mA regardless of Vin
    (B) 2.5 mA if Vin is 0 V
    (C) 2.5 mA if Vin is 5 V
    (D) 5.0 mA regardless of Vin
    (E) none of the above



29. The amount of current this circuit can **source** to a 1000 Ω load (referenced to GND) is approximately:
    (A) 0 mA regardless of Vin
    (B) 2.5 mA if Vin is 0 V
    (C) 2.5 mA if Vin is 5 V
    (D) 5.0 mA regardless of Vin
    (E) none of the above



30. The amount of current this circuit can **sink** from a 1000 Ω load (referenced to 5 V) is approximately:
    (A) 0 mA regardless of Vin
    (B) 2.5 mA if Vin is 0 V
    (C) 2.5 mA if Vin is 5 V
    (D) 5.0 mA regardless of Vin
    (E) none of the above