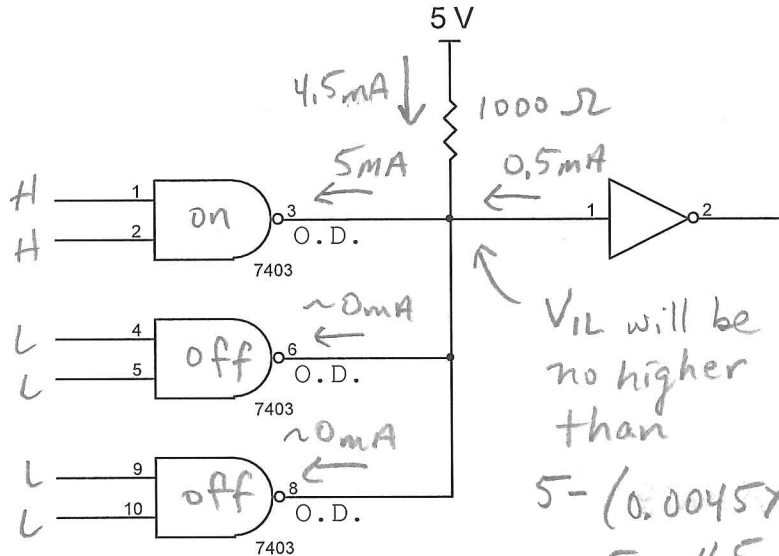


**LEARNING OUTCOME #1: "an ability to analyze and design CMOS logic gates."**

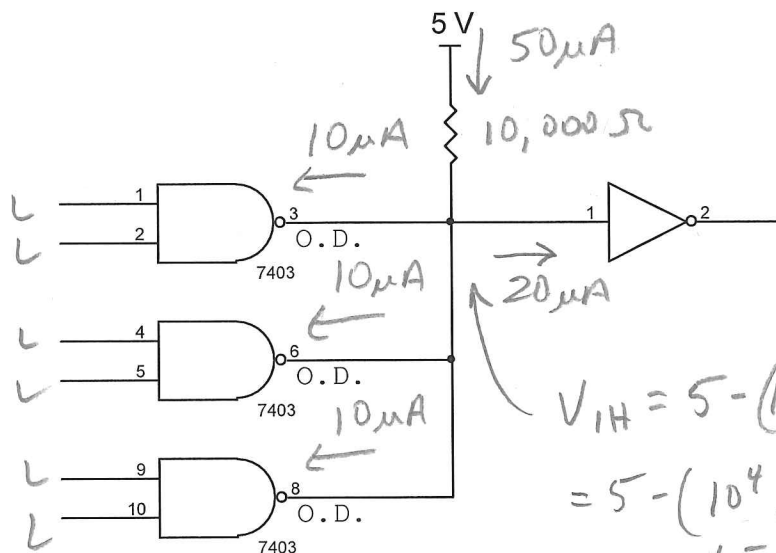
1. C
2. A
3. C
4. B
5. A
6. B
7. C
8. C
9. B
10. E
11. A
12. C
13. C
14. B
15. B
16. C
17. B
18. E
19. B
20. C
21. B
22. C
23. A
24. A
25. D
26. D
27. C
28. A
29. D
30. B

Problem 15 derivation:



Note:  $V_{IL}$  will decrease as additional OD NAND gates are turned on

Problem 16 derivation:



$$\begin{aligned}
 V_{IH} &= 5 - (10,000 \times 50\mu A) \\
 &= 5 - (10^4 \times 5 \times 10^{-5}) \\
 &= 5 - (5 \times 10^{-1}) \\
 &= 5 - 0.5 = 4.5V
 \end{aligned}$$