LEARNING OUTCOME #1: "an ability to analyze and design CMOS logic gates."

1. A – LSN, p. 2; Homework Assignment 1, Problem 1
2. C – LSN, p. 7; Practice Exam A, Problem 3
3. C – LSN, p. 4
4. A – LSN, p. 6
5. B – LSN, p. 17
6. C – LSN, p. 19; Homework Assignment 3, Problem 1a
7. A – LSN, p. 20; Homework Assignment 3, Problem 1a
8. A – LSN, p. 21; Homework Assignment 3, Problem 1c
9. C – LSN, p. 21; Homework Assignment 3, Problem 1b
10. A – LSN, p. 13; Homework Assignment 3, Problems 1b & 2a
11. B – LSN, p. 13; Homework Assignment 3, Problems 1c & 2a
12. D – LSN, p. 37
13. B – LSN, p. 13; Homework Assignment 2, Problem 4
14. C – LSN, p. 36
15. C – LSN, p. 14; Homework Assignment 2, Problems 1-3 (*DDPP 5th Ed.*, pp. 741-742)
16. C – LSN, p. 40; Practice Exam B, Problem 18
17. A – LSN, p. 40; Practice Exam B, Problem 19
18. D – LSN, p. 40; Practice Exam B, Problem 20
19. D – LSN, p. 40; Practice Exam B, Problem 21
20. A – LSN, p. 41; Practice Exam B, Problem 22
21. D – LSN, p. 42; Practice Homework 1, Problem 15f
22. A – LSN, p. 42; Practice Exam B, Problem 22
23. C – LSN, p. 42; Practice Homework 1, Problem 15b
24. A – LSN, p. 42; Practice Exam B, Problem 24
25. C – LSN, p. 40; Practice Exam A, Problem 17
26. B – LSN, p. 40; Practice Exam A, Problem 17
27. A – LSN, p. 17; Practice Exam A, Problem 26
28. D – LSN, p. 32; Practice Exam A, Problem 27
29. A – LSN, p. 33; Practice Exam A, Problem 28
30. C – LSN, p. 22; Practice Exam A, Problem 29