COURSE POLICIES AND PROCEDURES

Course Description: An introduction to digital logic design and hardware engineering with an emphasis on practical design techniques and circuit implementation.

Purpose of Course: ECE 270 serves as a prerequisite for upper-division Computer Engineering courses (e.g., ECE 337, ECE 362, ECE 437, ECE 477). It provides sophomore-level students with a basic overview of digital hardware engineering. Many concepts and techniques introduced in this course will be expanded and utilized in upper-division Computer Engineering courses.

Required Background: Basic understanding of circuits (voltage, current, Ohm's Law) and electrical components (resistors, capacitors, switches, diodes, MOSFETs). .

Course Web Site URL: https://engineering.purdue.edu/ece270

Course E-mail Address: ece270@ecn.purdue.edu

Changing Lab Divisions: You must consistently attend the lab division of ECE 270 lab for which you have registered. All lab division changes must be finalized during the first week of classes.

Text: *Digital Design Principles and Practices – 5th Ed.*, John F. Wakerly, Prentice Hall, 2017 (this text is also used as a reference in ECE 362 and ECE 477). Your learning will be maximized if you read the text assignments prior to coming to lecture.

Materials Required for Purchase: In addition to the course text listed above, you will need to purchase the following materials:

- **iClicker** Student Response Unit (available at bookstores – register on Blackboard)
- **Master Parts Kit** (available at http://www.elexp.com/pur_ece270_362.aspx) – *only needed if you have not previously purchased the kit for another ECE lab course*

Lecture Notes: Posted on the course web site. Each student will be responsible for printing his/her own copy of these materials and bringing them to class.

Computer Account: If you don't already have one, you ***must*** obtain a "coordinated" ITaP/ECN computer account to use the machines in lab. Requests can be sent to ecesite@ecn.purdue.edu. Further, you ***must*** establish a "*name@purdue.edu*" e-mail alias so that course information can be automatically sent to you.

Class Attendance: In a word, **REQUIRED.** You must be ***physically present*** to earn the associated class participation credit – no substitution will be allowed! ***It will be considered "cheating" for someone to use the student response unit ("clicker") of another student to "fake" that student's class participation.***

Consultation Outside of Class: Scheduled office hours for all course staff members will be posted on the course web site. All staff *teaching assistants* can provide consultation for questions concerning lecture material, homework exercises, and laboratory assignments. You are encouraged to make good use of all the "live" office hours available for this course – please do not E-mail long/detailed questions to the course staff about the lecture/lab material, as this type of communication tends to be very inefficient.

Homework: Assigned homework exercises will be collected at the beginning of your scheduled lab period and returned the following week.

Laboratory: The weekly lab meetings for this course will be held in room EE 065. The lab experiments have been designed to reinforce the lecture material; thus, it is very important that you ***attend lecture regularly and do the assigned reading from the course text*** in order to successfully complete the laboratory portion of this course. Quizzes will be given at the beginning of your scheduled lab period to help keep you on track. A separate document details the *Laboratory Policies and Procedures.*

Learning Outcomes and Objectives: A student who successfully fulfills the course requirements will have demonstrated:

1. an ability to analyze and design CMOS logic gates
2. an ability to analyze and design combinational logic circuits
3. an ability to analyze and design sequential logic circuits
4. an ability to analyze and design computer logic circuits
5. an ability to realize, test, and debug practical digital circuits

Learning Outcome Assessment: ***You will earn 1% bonus credit for each course outcome you successfully demonstrate.*** For Outcomes 1-4, basic competency will be assessed based on exam questions, for which a minimum score of **60%** will be required. Two opportunities will be provided to demonstrate competency in Outcome 5: earning a minimum score of **60%** on ***each*** experiment **or** a minimum score of **60%** on the Lab Practical Exam. A score greater than or equal to the passing threshold on ***either*** of these assessments will be sufficient to establish basic competency.

Exams: Evening exams will be used to assess the first three outcomes (see course website for times and locations); the fourth outcome will be assessed during the scheduled final exam session. Seating for each exam will be assigned – be sure to save your exam seating assignment (which will be E-mailed to you before each exam). Also, bring your **PUID card** with you to each exam for identification purposes and to ensure your PUID is correctly entered on your "bubble sheet". All exams will be of a standardized nature and electronically scored; results of each exam will be E-mailed to you once they are graded, along with a record of your outcome demonstration status.

Exam Calculator Policy: The calculator make/model currently approved by the ECE Curriculum Committee for use on exams will be allowed.

Makeup Exams: If you have a known conflict with a scheduled exam, you must take a makeup exam ***prior*** to the scheduled exam time. **No** makeup exams will be given, however, **after** the scheduled exam period unless your absence has been officially excused by the Dean of Students.

"The Best Way to Study for This Course": The best way to learn the kind of material covered in this course is to ***review*** *it as* ***soon*** *after attending class as possible* and to ***practice*** *similar problems*. The *Lecture Summary Notes* will help you *actively encode* essential course material (instructional research has shown that notes ***you*** take in class serve more than for mere "archival" of information – they actually help you *remember* the material presented in lecture). Obviously, *regular lecture attendance* is essential to the entire process. Further, given that we typically *forget* 90% of what we *hear*, but *remember* 80% of what we do, the "best way to study for this course" can be summed up in three words: practice, *practice, practice!*

A Novel Recommendation: Read the assigned text material before each class period, and do the assigned homework problems as soon after lecture as possible. The keys to success are keeping current with the material and making effective use of the learning resources available (e.g., instructor office hours, lab office hours, studying practice exams and quizzes, and effectively utilizing on-line resources).

Grade Weightings: Your raw score (i.e., "**R**aw **W**eighted **P**ercentage" or **RWP**) will be calculated based on the following weights:

Bonus Exercises	Δ_1%
Class Participation: iClickers	4.0%
Homework Assignments (13 @ 0.77%)	10.0%
Lab Experiments (13 @ 1.5%)	19.5%
Lab Quizzes (13 @ 0.5%)	6.5%
Lab Practical Exam	10.0%
Outcome Assessment Exams (4 Outcomes @ 12.5%)	50.0%
Outcome Demonstration Bonus (5 Outcomes @ 1%)	Δ_2%
	100+Δ%

Course Grade Determination: Your **R**aw **W**eighted **P**ercentage (RWP), described above, will be mean-shifted with respect to the upper percentile of the class to obtain a **N**ormalized **W**eighted **P**ercentage (NWP). For example, if the top student has an RWP of 97%, everyone's RWP will be multiplied by 1.031 to obtain their corresponding NWP. Equal-width cutoffs will then be applied based on the **W**indowed **S**tandard **D**eviation (WSD) of the raw class scores; the minimum **C**utoff **W**idth **F**actor (CWF) used will be 10 (i.e., the nominal cutoffs for A-B-C-D will be 90-80-70-60, respectively). Letter grades in the upper 30% of each range will have a "+" designation, and those that fall in the lower 30% of each range will have a "–" designation.

Reporting of Projected Course Grades: Your projected course grade will be calculated periodically throughout the semester (typically after each Primary Assessment Exam) and reported to you via E-mail. Final course grades will be reported to you in a similar fashion.

Borderline Cases: A "borderline" is officially defined as an NWP within 0.5% of a cutoff when the **final** grade calculation is performed. Before course grades are assigned, the instructor will carefully examine all such cases and determine if the next higher grade is warranted. A special bonus, IDPPB (*Instructor Discretion Posi-Points Bonus*), will be used to facilitate borderline adjustments; ***note, however, that the "next higher grade" is NOT automatically guaranteed.***

Incompletes and Conditional Failures: A grade of "I" or "E" will be given *only* for cases in which there are ***documented*** medical or family emergencies that prevent a student from completing required course work by the end of the semester. Note that University Regulations stipulate that a student must be passing in order to ***qualify*** for a grade of "I" or "E".

Campus Emergencies: In the event of a major campus emergency, course requirements, deadlines, and grading percentages are subject to changes that may be necessitated by a revised semester calendar or other circumstances beyond the instructor's control. Should such an emergency occur, information will be posted on the course web site Message Board.

Professionalism and Academic Honesty: The temptation to cheat is particularly prevalent in large enrollment courses such as this one. In the long run, *short-cuts in school work* breed *short-cuts in careers*, i.e., the less you invest in your education, the less you will have to show for it later in life. A large part of the educational process is simply developing the *discipline* and *mindset* required to contribute in a given technical area once you graduate. If for nothing other than your own benefit, *do not copy the work of any other student* (past or present). Further, be advised that any *documented* case of "cheating" will result in a **FAILING GRADE** for the course as well as possible disciplinary action. All cases of academic dishonesty will be reported to the ECE Associate Head as well as to the Dean of Students. ***A professional person does not take credit for the work of someone else*.**

Examples of Cheating: Contrary to the beliefs of the post-modern "situational ethics" crowd, there are indeed absolutes that apply to integrity and honesty. Examples of activities that will be construed to be "cheating" include **(but are not limited to)** the following:

- forging another student's signature on a homework verification form
- turning in a homework verification form for a student who is not present
- copying the work of another student (past or present) and representing that work as your own
- divulging the contents of an exam to students who have not yet taken it
- obtaining information about an exam prior to taking it
- having someone else take an exam for you
- bringing "cheat sheets" in any shape/form with you to an exam
- using a cell phone or other electronic device to share information during an exam
- using a pen camera, cell phone, or any other device to photograph exam materials
- modifying a graded lab or homework paper and submitting it for reevaluation
- sharing lab solutions with other students
- using another student's (past or present) lab or homework files
- discussing the lab practical exam before all students have completed it
- using an iClicker that belongs to someone else to "fake" their class attendance
- copying and/or redistributing any of the copyrighted materials posted on the course web site
- posting solutions to homework problems or lab experiments

Mediocrity: One of the biggest problems facing our educational system today is mediocrity – too many students want to learn merely (often *barely*) enough to "get by". In fact, higher education is probably the only "commodity" from which consumers want to get the *least* amount for their money! Clearly, if our country is to be competitive in an expanding world market, a renewed commitment to excellence is absolutely essential. To quote C. R. Swindoll, "The greatest waste of natural resources is the number of people who never achieve their potential."

Bonus Exercises: Good for you if you've read this far! There will be numerous exercises that will count as bonus credit toward your course grade. To earn bonus credit, you must: (1) consistently attend class, (2) bring notes and reference materials with you to each class meeting, (3) complete reading any assigned text/reference material before each class meeting, and (4) regularly check the *Message Board* on the course web site.

Lecture and Lab Outline:

Learning Outcome	***Lecture and Lab Topics***
1. An ability to analyze and design CMOS logic gates (8 lectures)	Number systems, base conversion, switching algebra, basic electronic components and concepts, logic signals, CMOS logic circuits, logic levels and noise margins, current sourcing and sinking, transition time, propagation delay, power consumption and decoupling, Schmitt triggers, transmission gates, three-state and open-drain outputs
2. An ability to analyze and design combinational logic circuits (8 lectures)	Combinational circuit analysis and synthesis, mapping and minimization, timing hazards, XOR/XNOR functions, programmable logic devices, hardware description languages, combinational building blocks: decoders, encoders, and multiplexers
3. An ability to analyze and design sequential logic circuits (9 lectures)	Bi-stable elements, set-reset and data latches, data and toggle flip-flops, state machine structure and analysis, clocked synchronous state machine synthesis, state machine design examples: sequence generators, counters and shift registers, and sequence recognizers
4. An ability to analyze and design computer logic circuits (11 lectures)	Signed number notation; radix addition and subtraction; adder, subtractor, and comparator circuits; carry look-ahead adder circuits; multiplier circuits; BCD adder circuits; simple computer top-down specification, instruction execution tracing, bottom-up realization, basic extensions, and advanced extensions
5. An ability to realize, test, and debug practical digital circuits (13 lab experiments)	Demonstration of Basic Logic Functions, Measurement of Gate Electrical Characteristics, Measurement of Gate Timing Characteristics, Implementation of Dual and Complement Functions, Investigation of Timing Hazards, Introduction to ispLever™ and Programmable Logic Devices, 7-Segment Alphanumeric Decoder, Introduction to Sequential Circuits, Introduction to ispMACH Development Board, Scrolling 7-Segment Display, Digital Combination Lock with Pseudo-Random Combination, Arithmetic Circuit, Simple Computer