ECE 440

VCOs

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October 3, 2012

From TI Application Report (Sept. 2002)

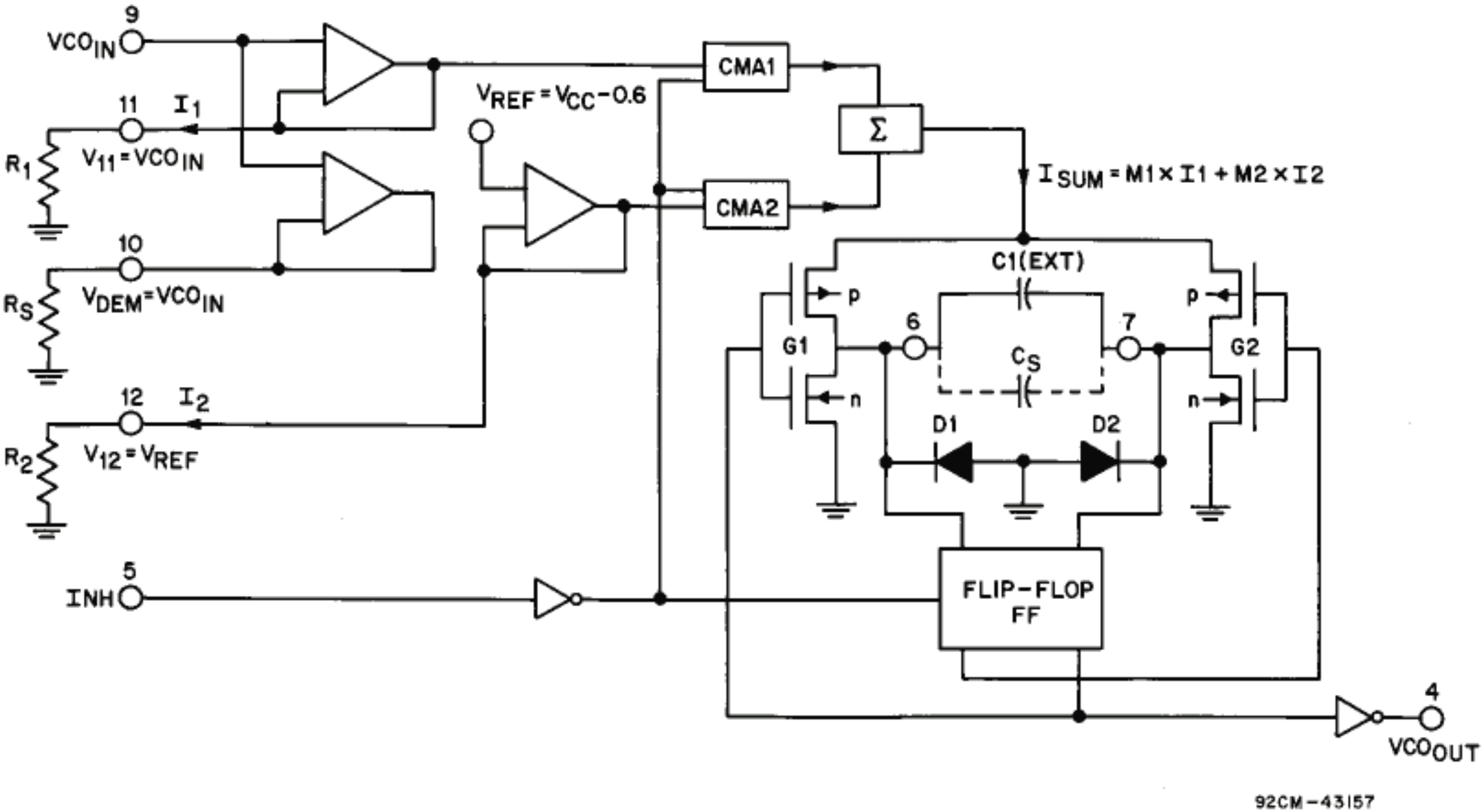

Figure 15. VCO Portion of CD74HC4046A/7046A Functional Block Diagram

From Fairchild Datasheet (Oct. 2003)

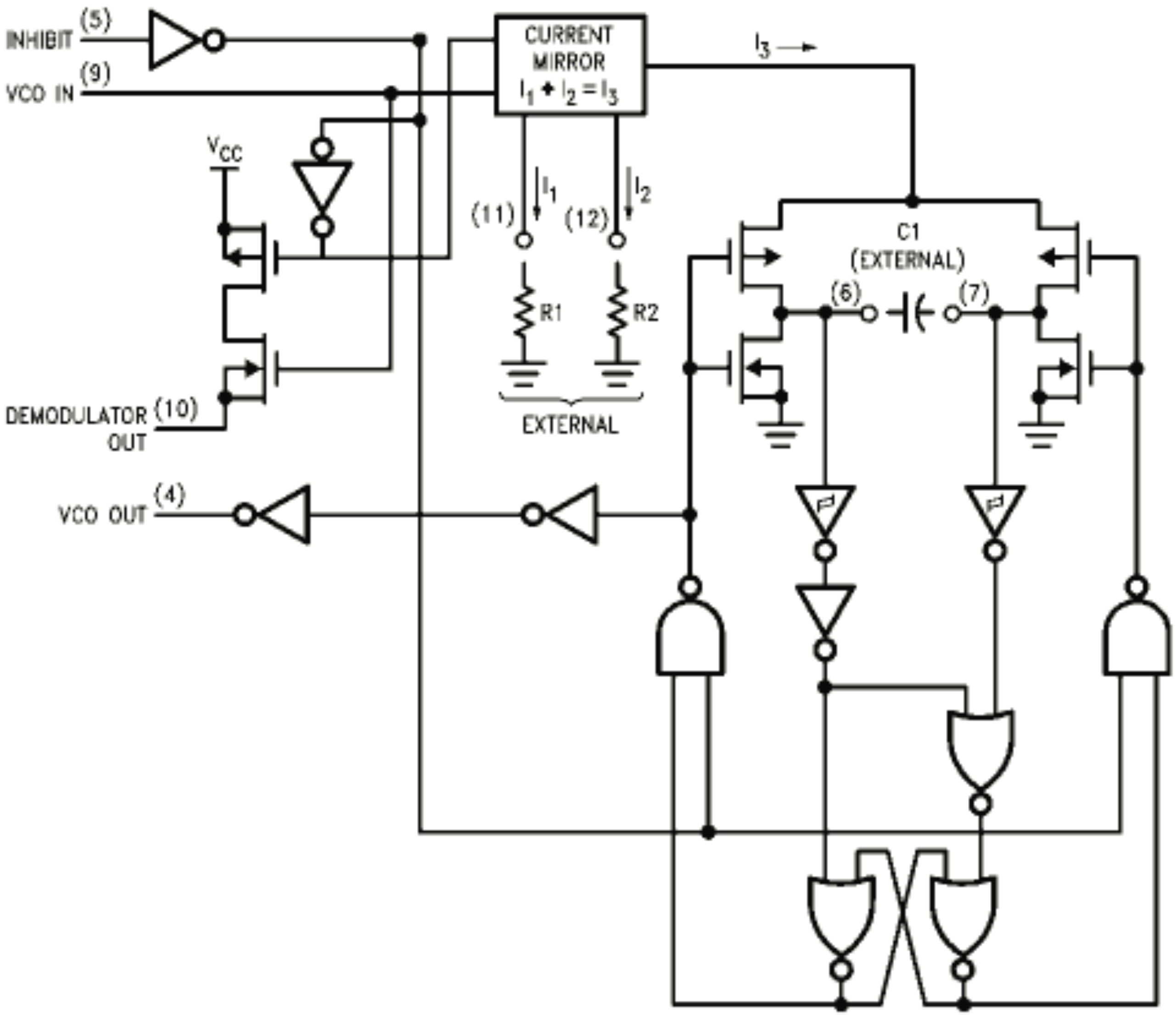

FIGURE 2. Logic Diagram for VCO

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From Fairchild Datasheet (Oct. 2003)

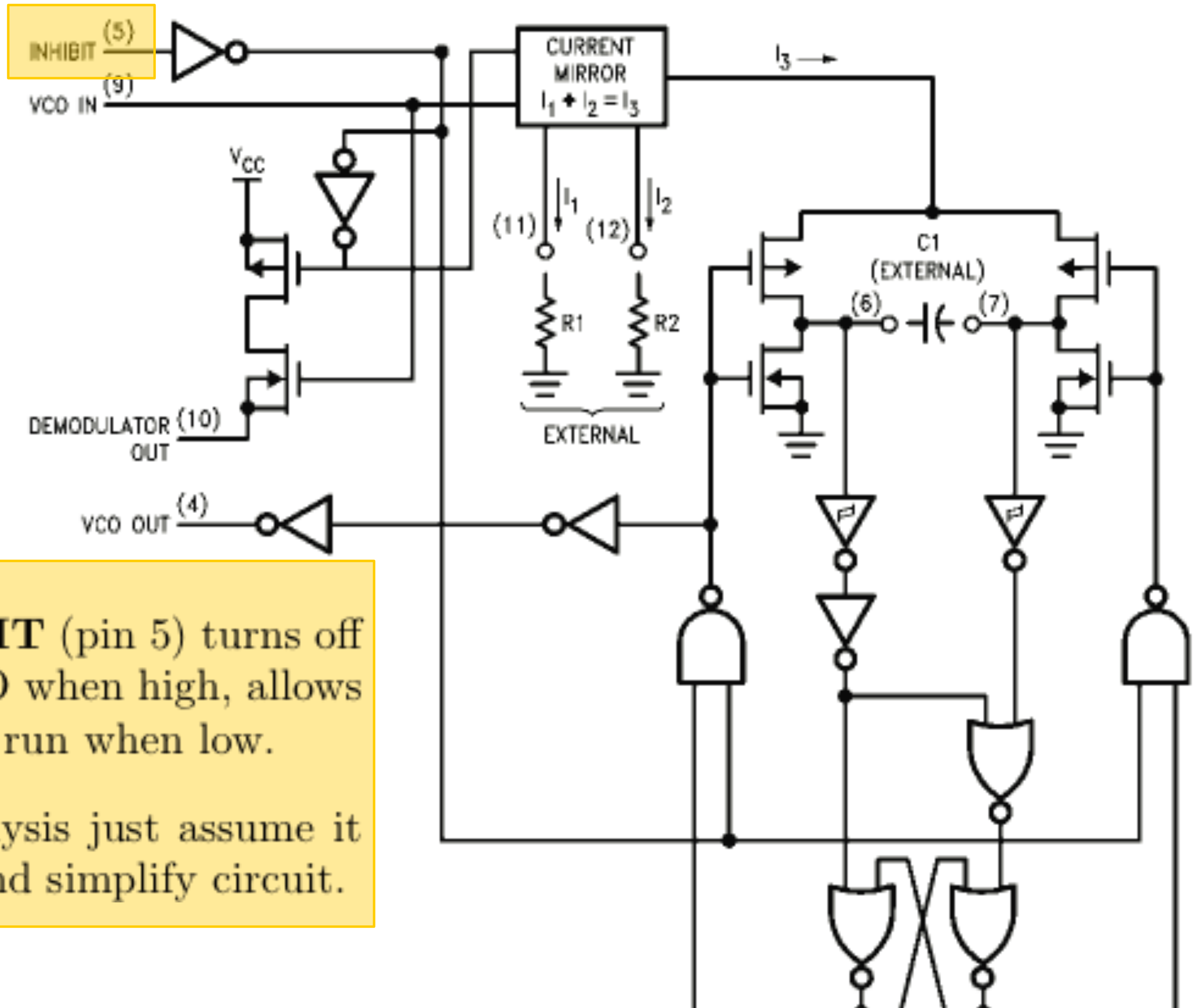
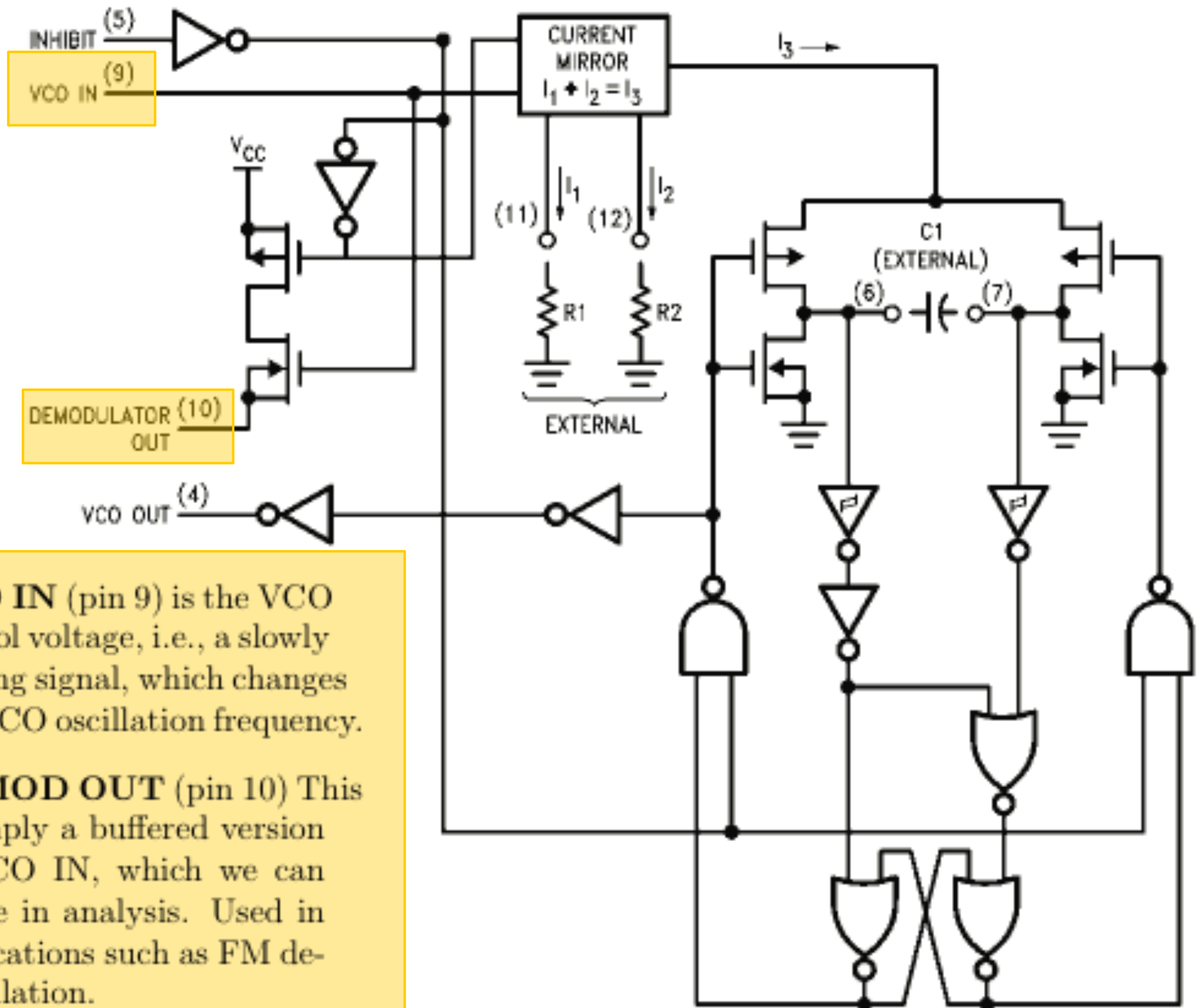


FIGURE 2. Logic Diagram for VCO

- **INHIBIT** (pin 5) turns off the VCO when high, allows VCO to run when low.
- For analysis just assume it is low and simplify circuit.

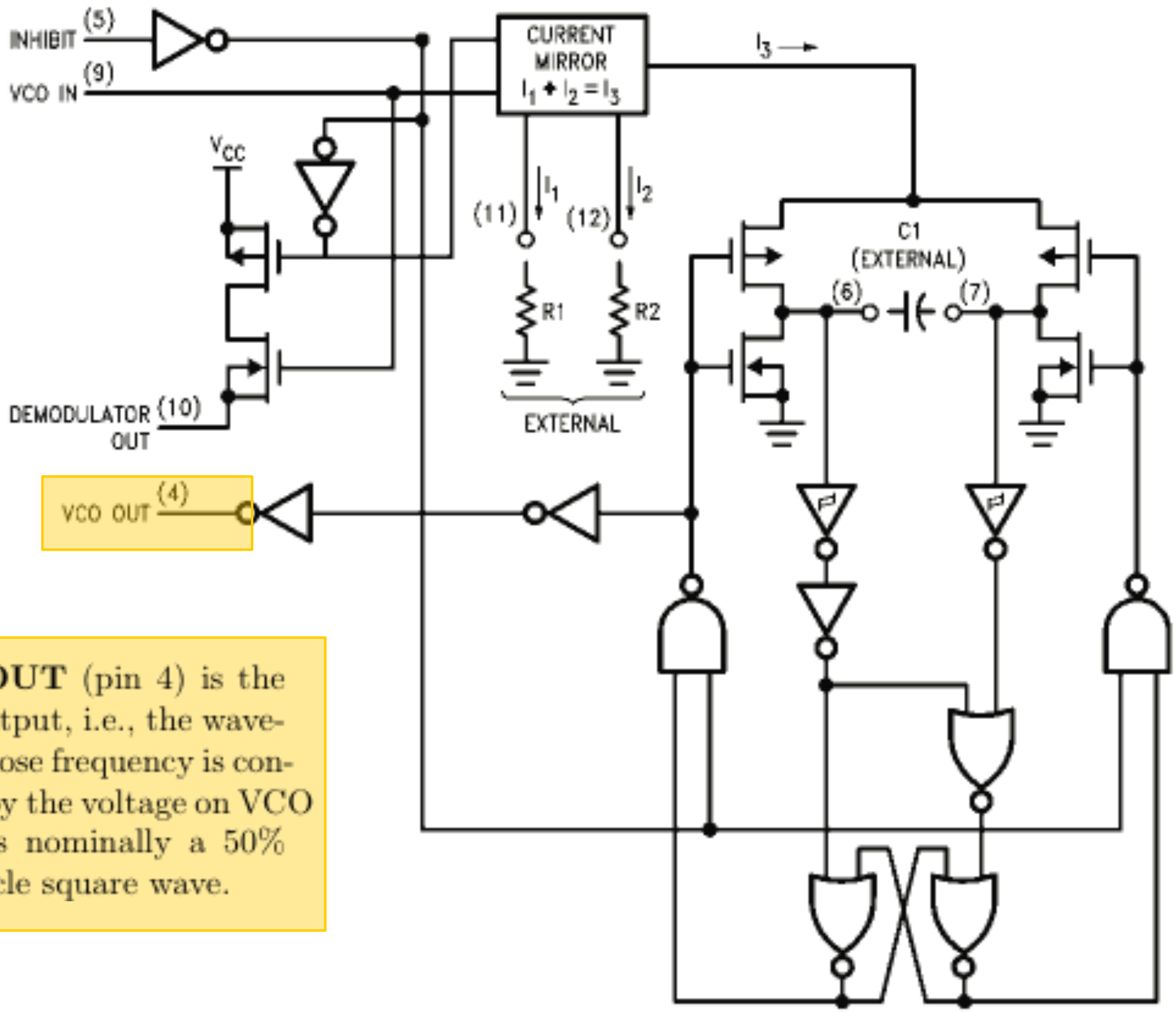
From Fairchild Datasheet (Oct. 2003)



- **VCO IN** (pin 9) is the VCO control voltage, i.e., a slowly varying signal, which changes the VCO oscillation frequency.
- **DEMOD OUT** (pin 10) This is simply a buffered version of VCO IN, which we can ignore in analysis. Used in applications such as FM demodulation.

FIGURE 2. Logic Diagram for VCO

From Fairchild Datasheet (Oct. 2003)



- **VCO OUT** (pin 4) is the VCO output, i.e., the waveform whose frequency is controlled by the voltage on VCO IN. It is nominally a 50% duty cycle square wave.

FIGURE 2. Logic Diagram for VCO

From Fairchild Datasheet (Oct. 2003)

- **Current source** I_3 value is a linear combination of the currents I_1 (pin 11) and I_2 (pin 12):

$$I_3 = M_1 I_1 + M_2 I_2.$$

- $I_1 = \frac{\text{VCO IN}}{R_1}$.
- $I_2 = \frac{\text{Vcc - 0.6 V}}{R_2}$.
- Freq. of VCO directly proportional to I_3. Thus I_2 sets min. VCO freq. and I_1 is used to vary freq. from min. to max.

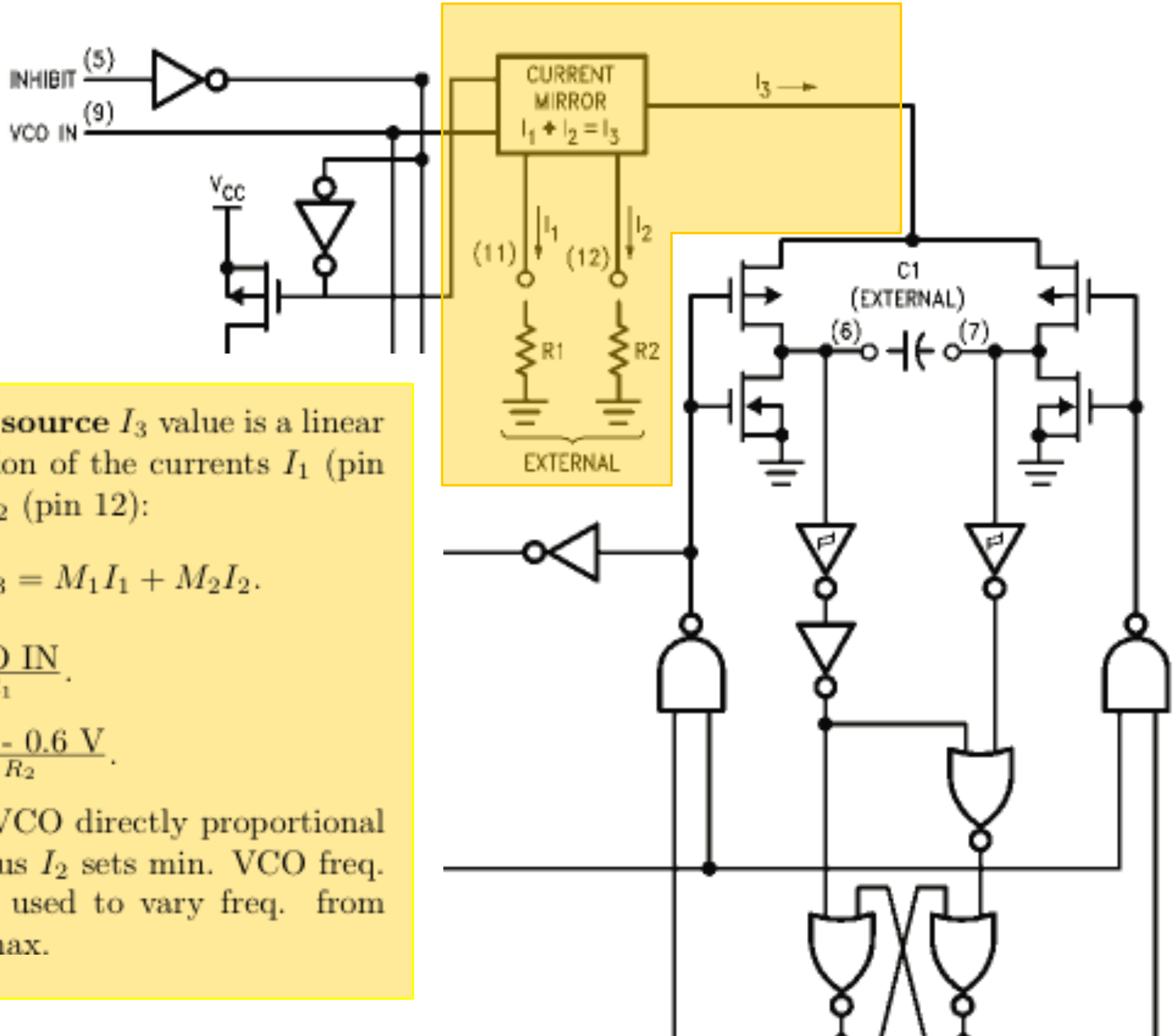
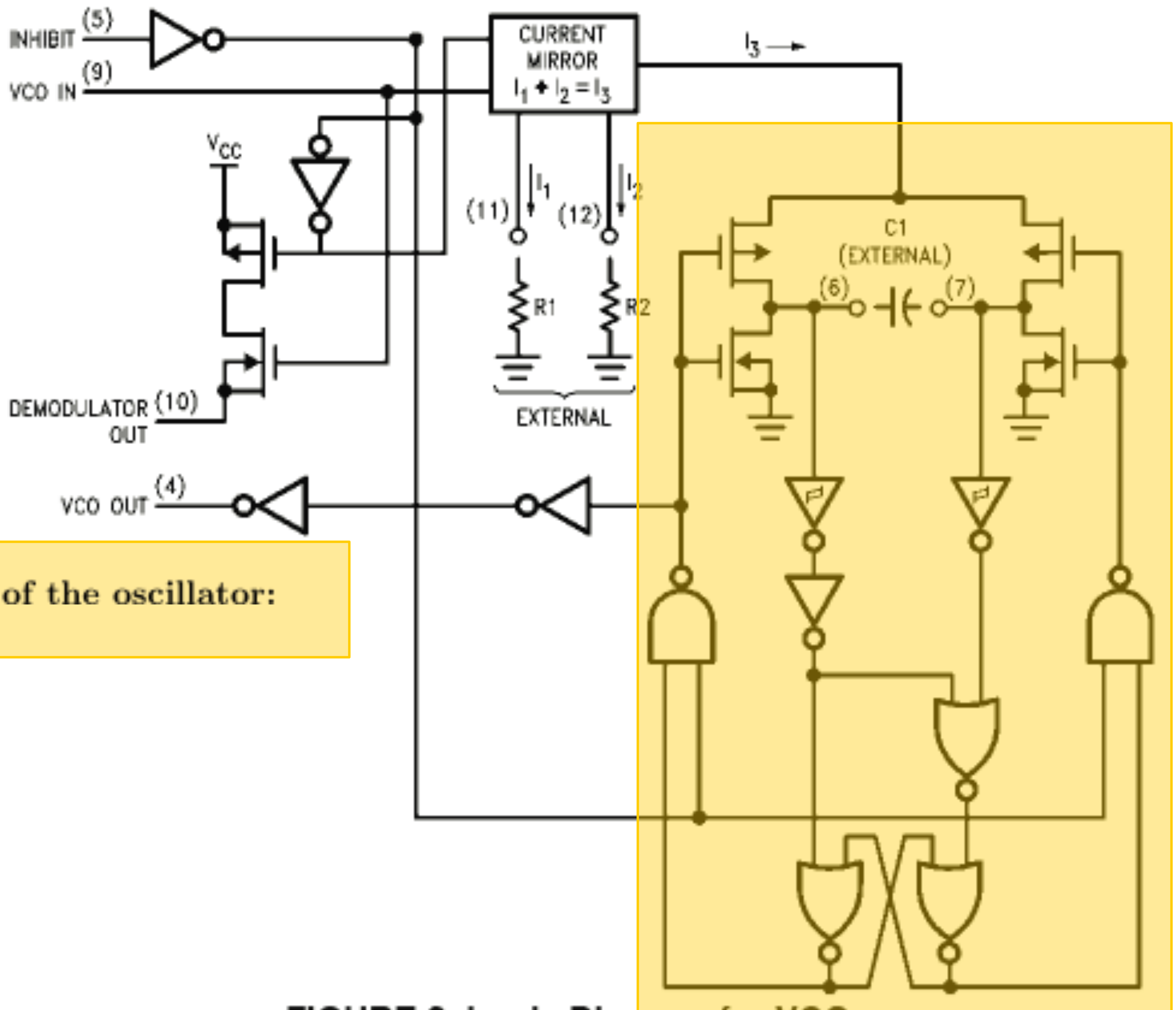


FIGURE 2. Logic Diagram for VCO

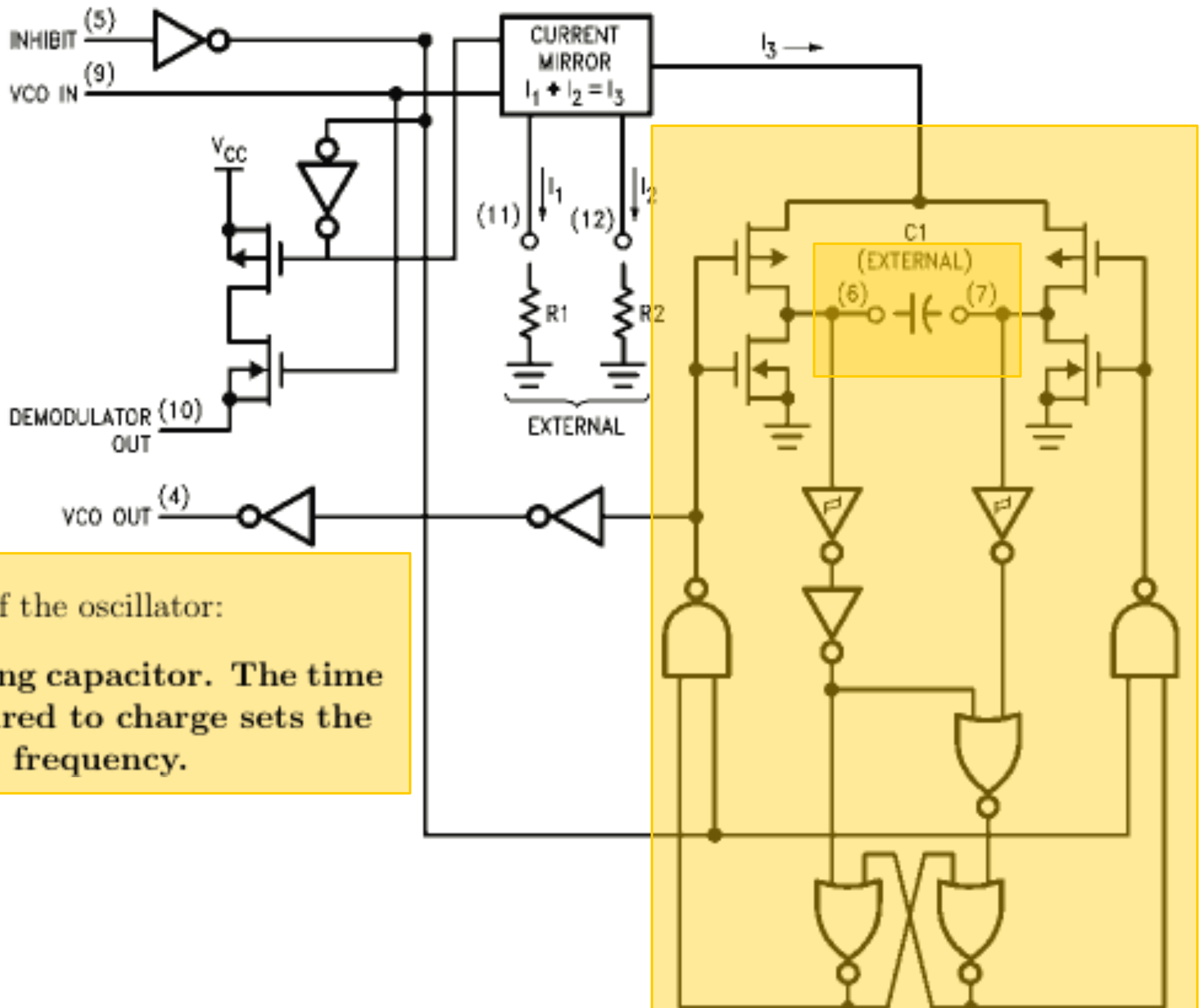
From Fairchild Datasheet (Oct. 2003)



- The core of the oscillator:

FIGURE 2. Logic Diagram for VCO

From Fairchild Datasheet (Oct. 2003)



- The core of the oscillator:
  - **Timing capacitor. The time required to charge sets the VCO frequency.**

FIGURE 2. Logic Diagram for VCO

From Fairchild Datasheet (Oct. 2003)

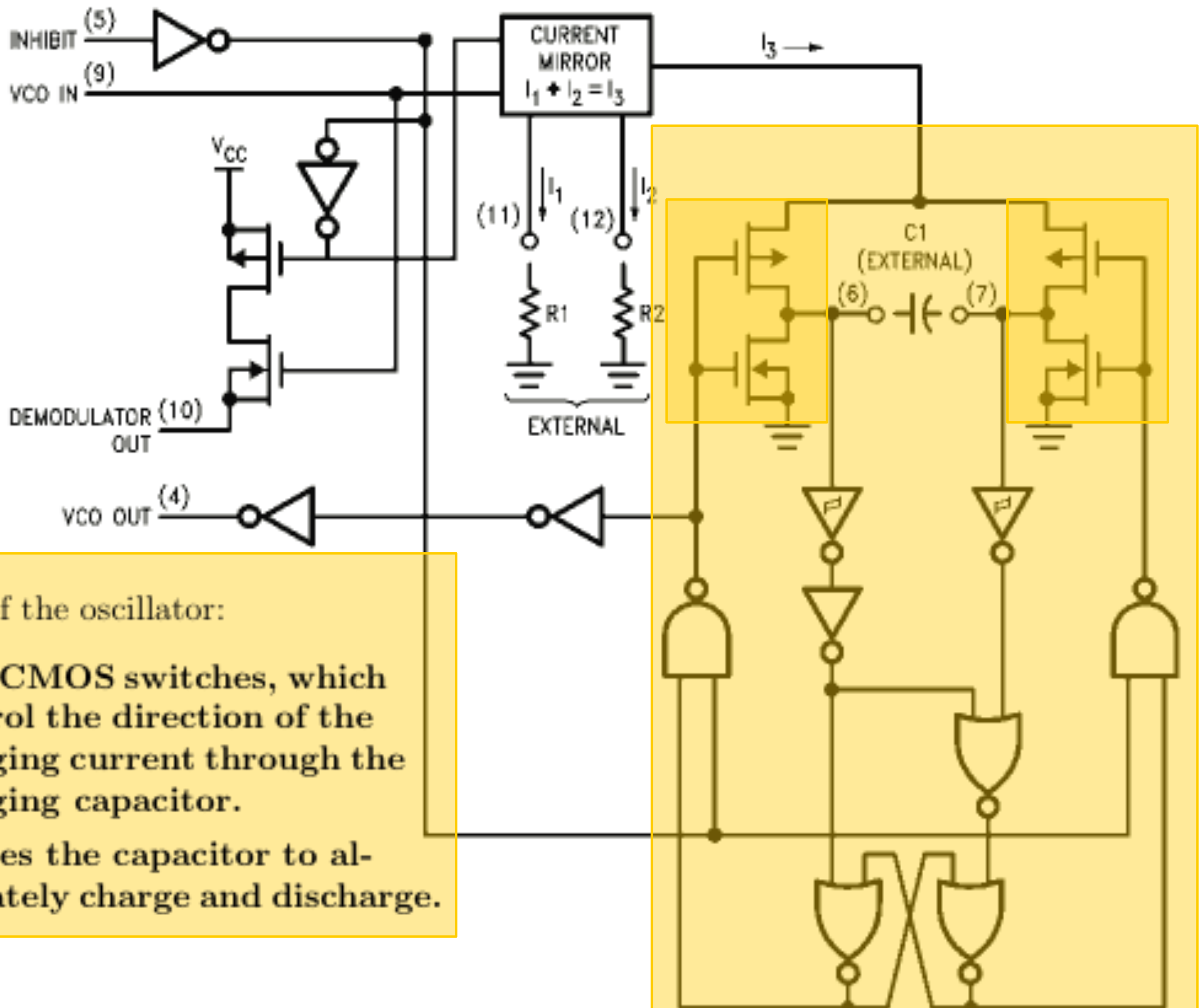


FIGURE 2. Logic Diagram for VCO

- The core of the oscillator:
  - **Two CMOS switches, which control the direction of the charging current through the charging capacitor.**
  - **Causes the capacitor to alternately charge and discharge.**

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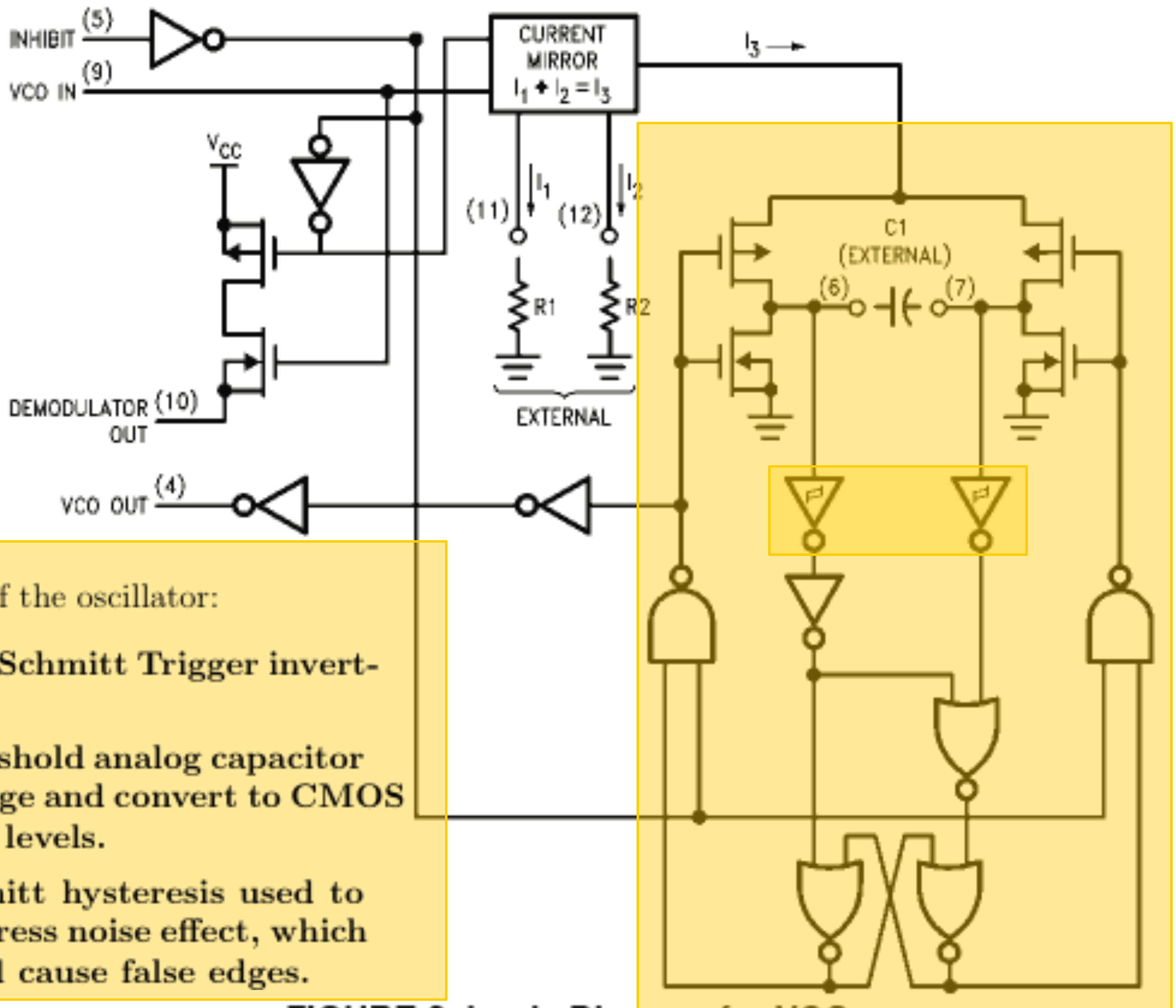
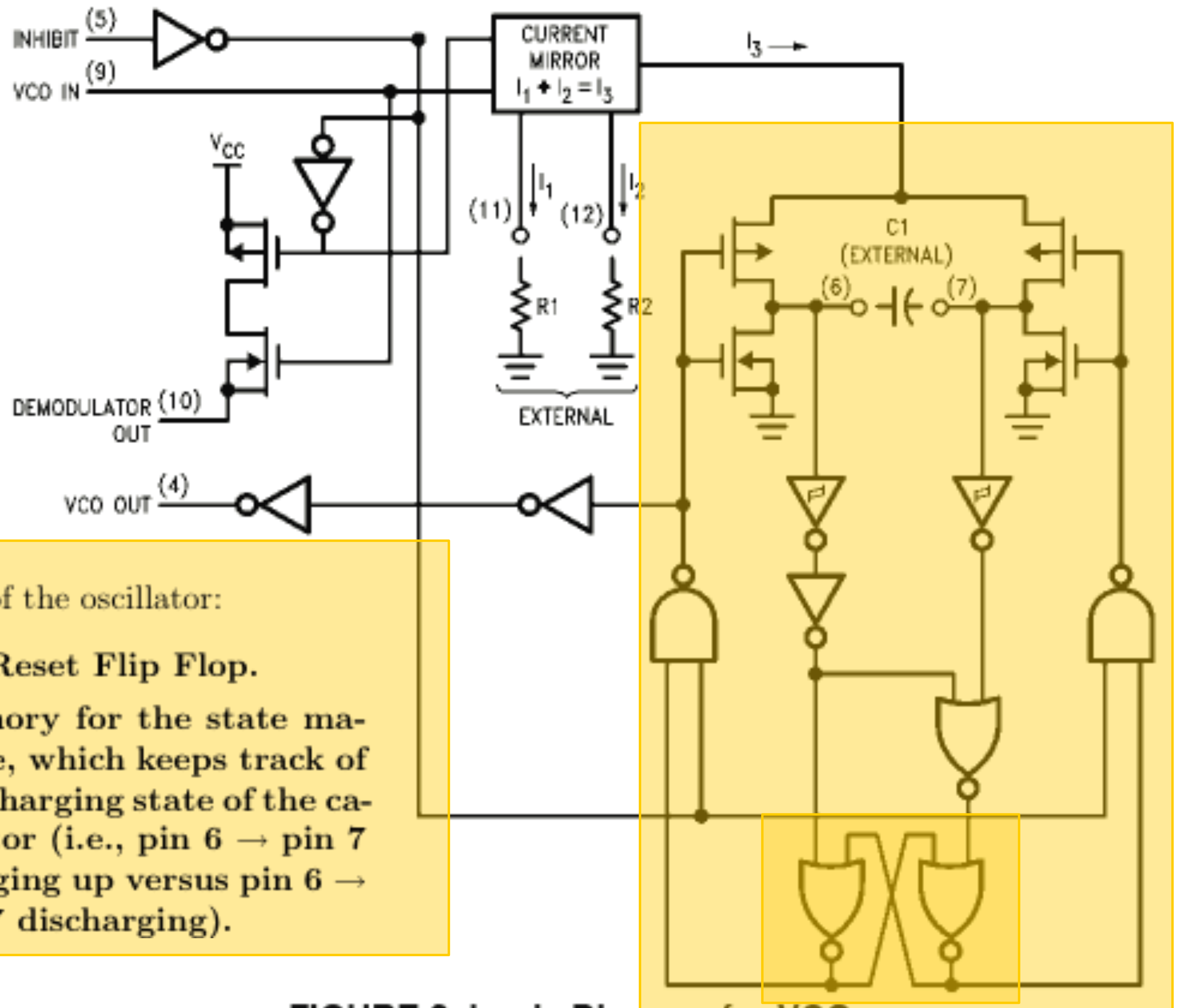
From Fairchild Datasheet (Oct. 2003)



- The core of the oscillator:
  - **Two Schmitt Trigger inverters.**
  - **Threshold analog capacitor voltage and convert to CMOS logic levels.**
  - **Schmitt hysteresis used to suppress noise effect, which could cause false edges.**

FIGURE 2. Logic Diagram for VCO

From Fairchild Datasheet (Oct. 2003)

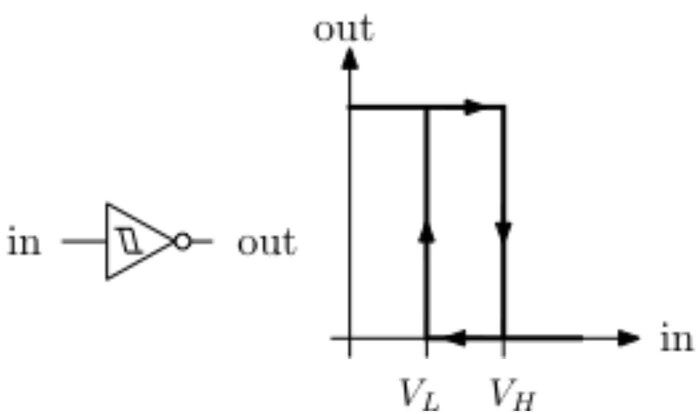


- The core of the oscillator:
  - **Set-Reset Flip Flop.**
  - **Memory for the state machine, which keeps track of the charging state of the capacitor (i.e., pin 6 → pin 7 charging up versus pin 6 → pin 7 discharging).**

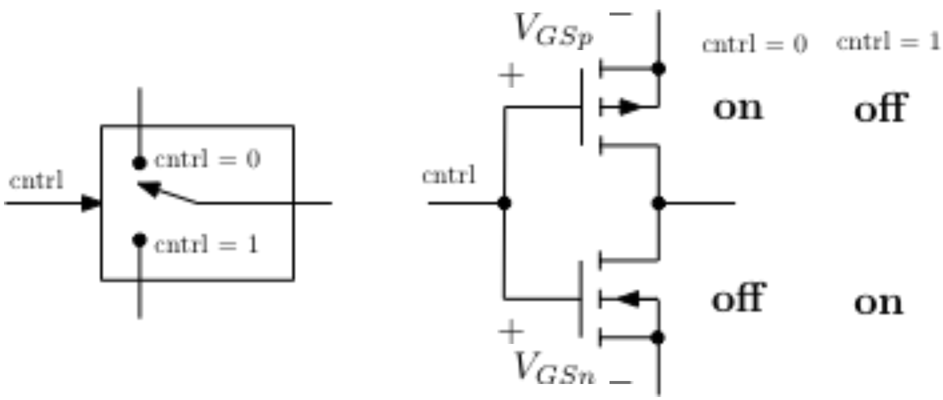
FIGURE 2. Logic Diagram for VCO

Need Simple Model for Analysis

Model for Schmitt Trigger inverter

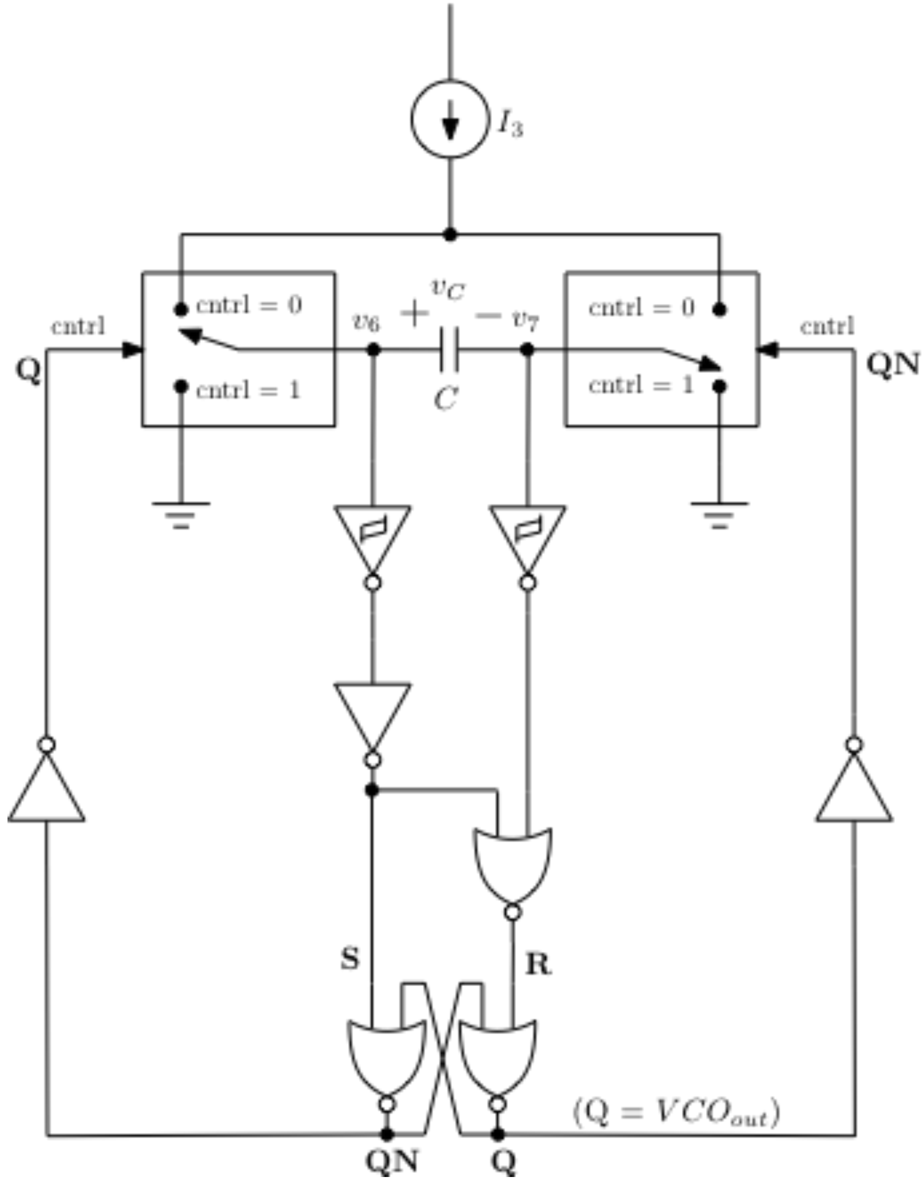


Model for CMOS switch

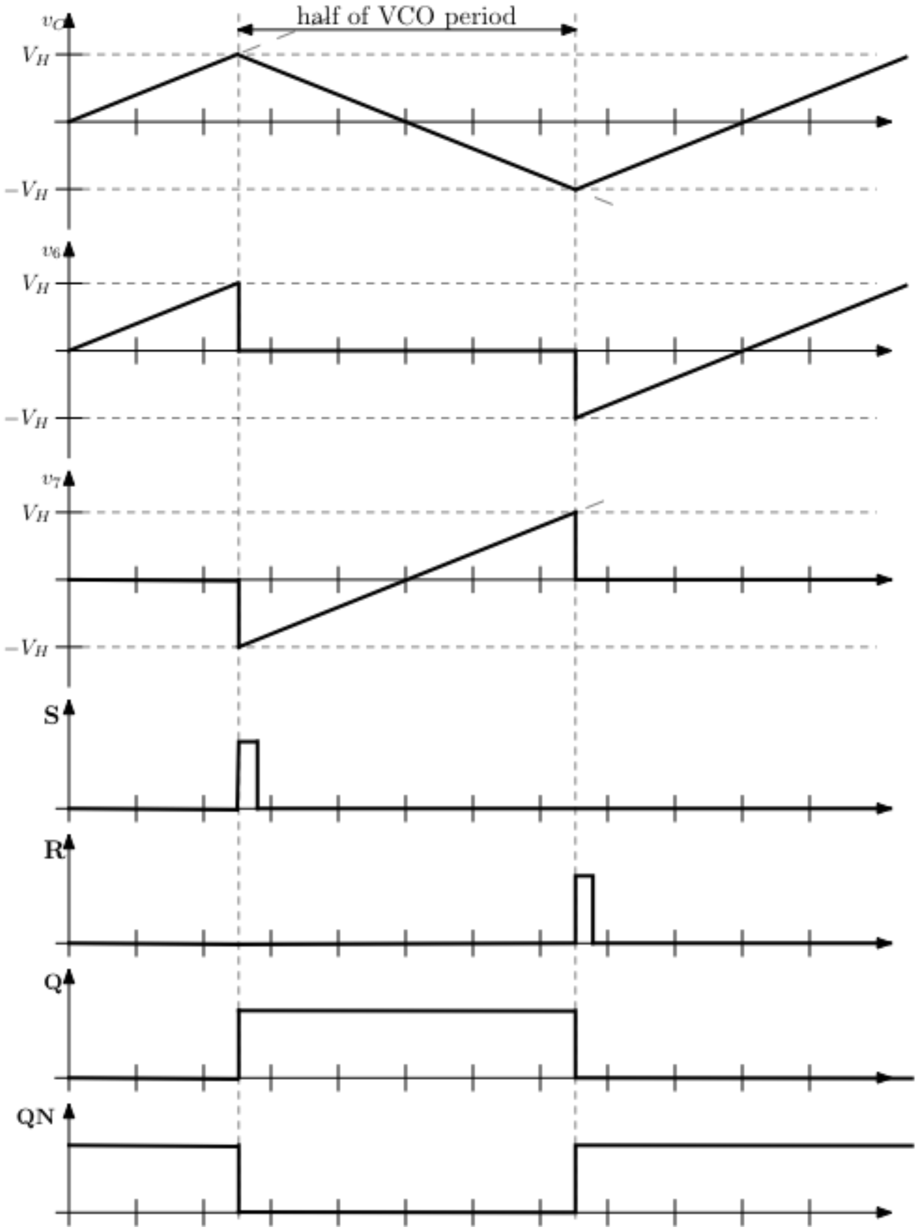


- Top transistor is p-channel enhancement mode.
  - Therefore, is on for $V_{GSp} \leq V_{tp} < 0$ V.
  - This happens when "cntrl" is low (a.k.a. 0).
- Bottom transistor is n-channel enhancement mode.
  - Therefore, is on for $V_{GSn} \geq V_{tn} > 0$ V.
  - This happens when "cntrl" is high (a.k.a. 1).

Simplest VCO Model



Waveforms for Simplest Model



Half of the Q = VCO_{out} period is time it takes to charge capacitor from $-V_H$ to V_H with a constant current I_3:

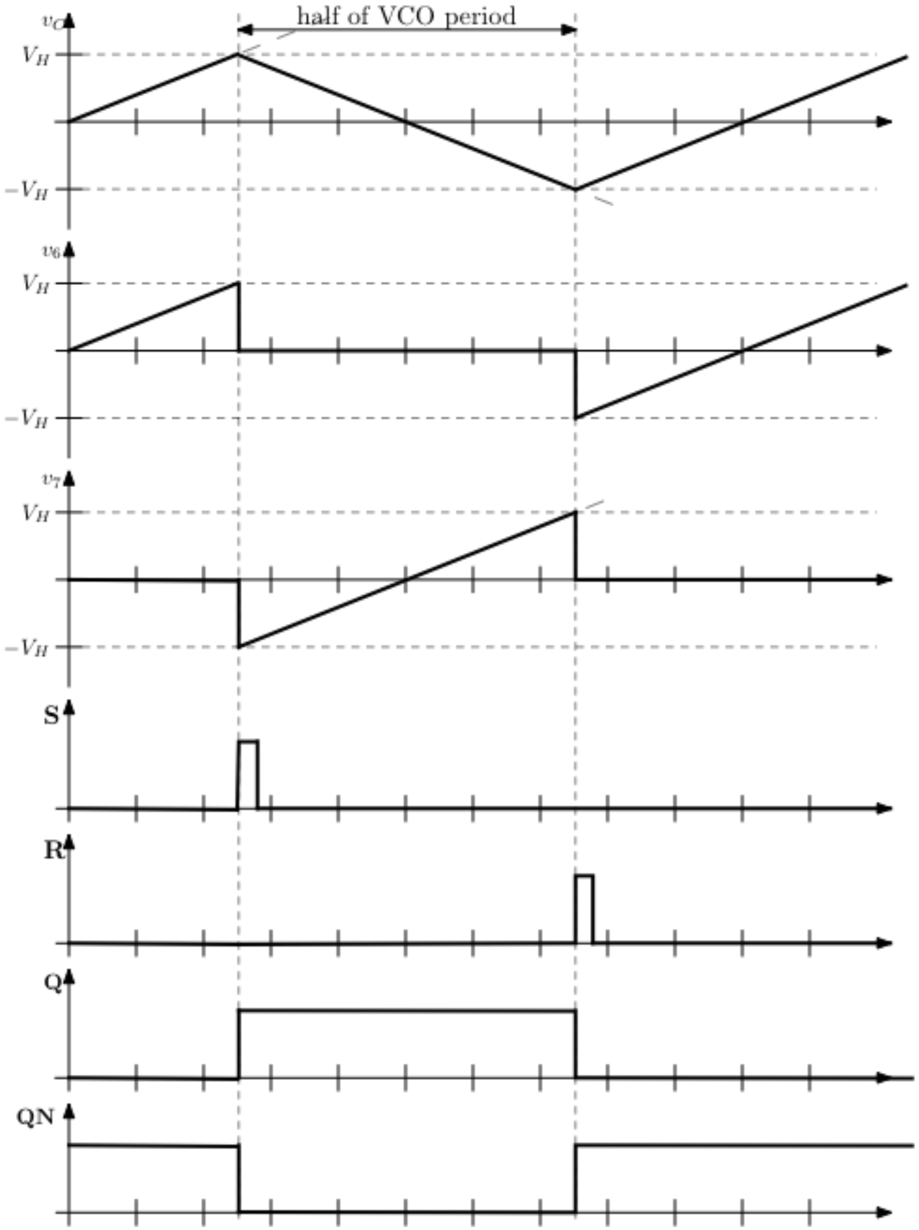
$$2V_H = \frac{I_3}{C}\frac{T_{VCO}}{2}$$

$$\downarrow$$

$$T_{VCO} = \frac{4V_H C}{I_3}$$

$$f_{VCO} = \frac{I_3}{4V_H C}$$

Waveforms for Simplest Model



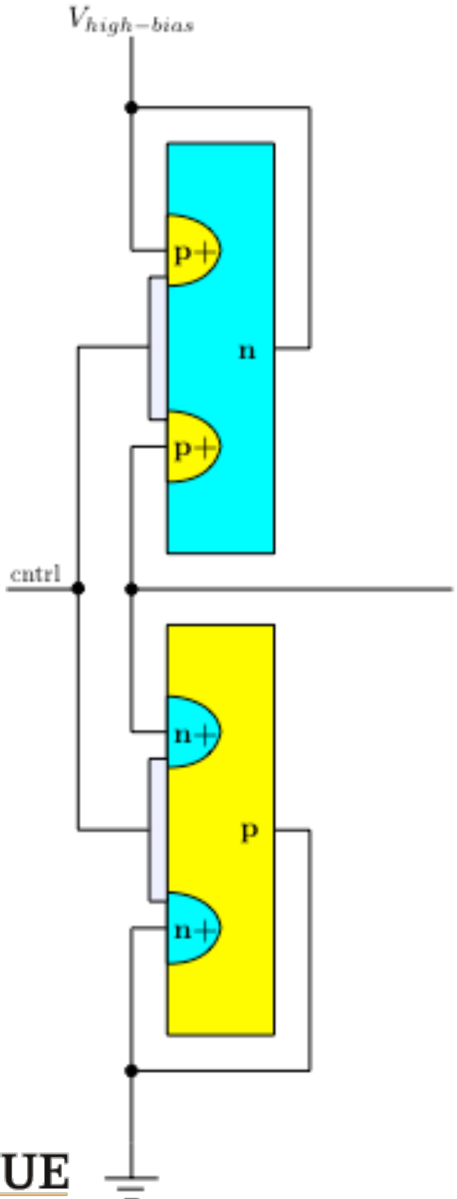
Half of the Q = VCO_{out} period is time it takes to charge capacitor from $-V_H$ to V_H with a constant current I_3:

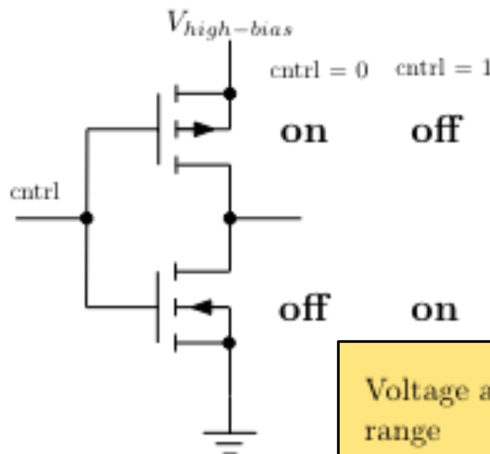
$$
\begin{aligned}
2V_H &= \frac{I_3}{C}\frac{T_{VCO}}{2} \\
&\downarrow \\
T_{VCO} &= \frac{4V_H C}{I_3} \\
f_{VCO} &= \frac{I_3}{4V_H C}
\end{aligned}
$$

Only one problem with model: It's a bit too simple and the VCO waveforms do not look quite like these.

Issue is our overly simple model for the CMOS switches.

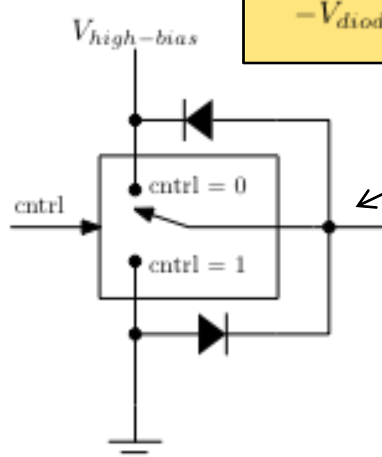
Improved Model of CMOS Switches



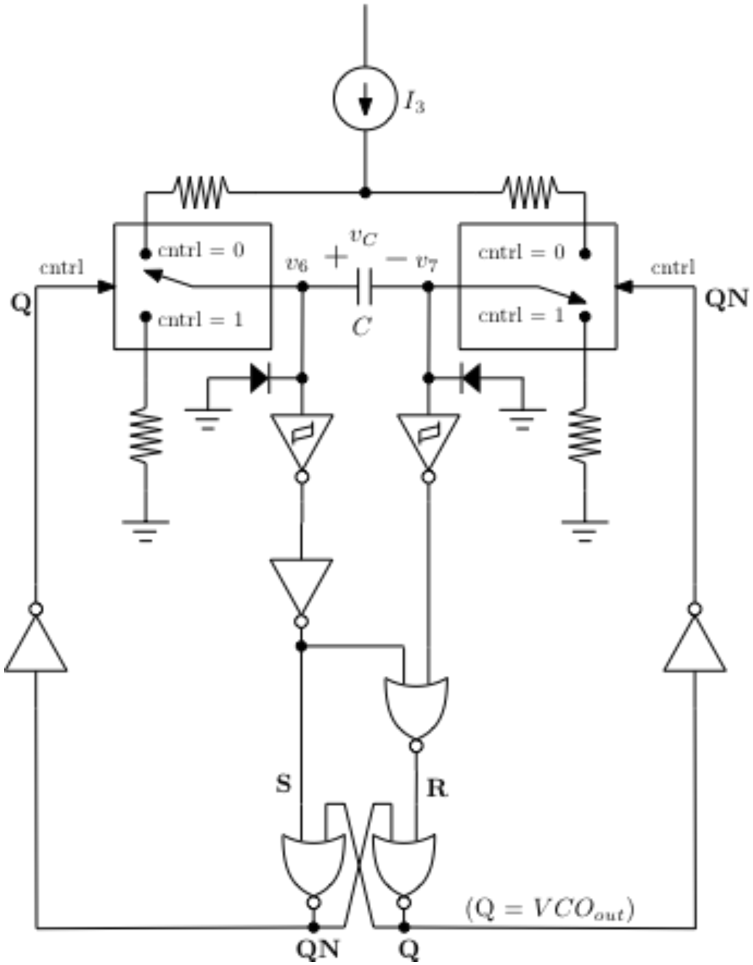


Voltage at this node is clamped by diodes to stay in the range

$$-V_{diode-drop} \leq V_{sw-node} \leq V_{high-bias} + V_{diode-drop}.$$

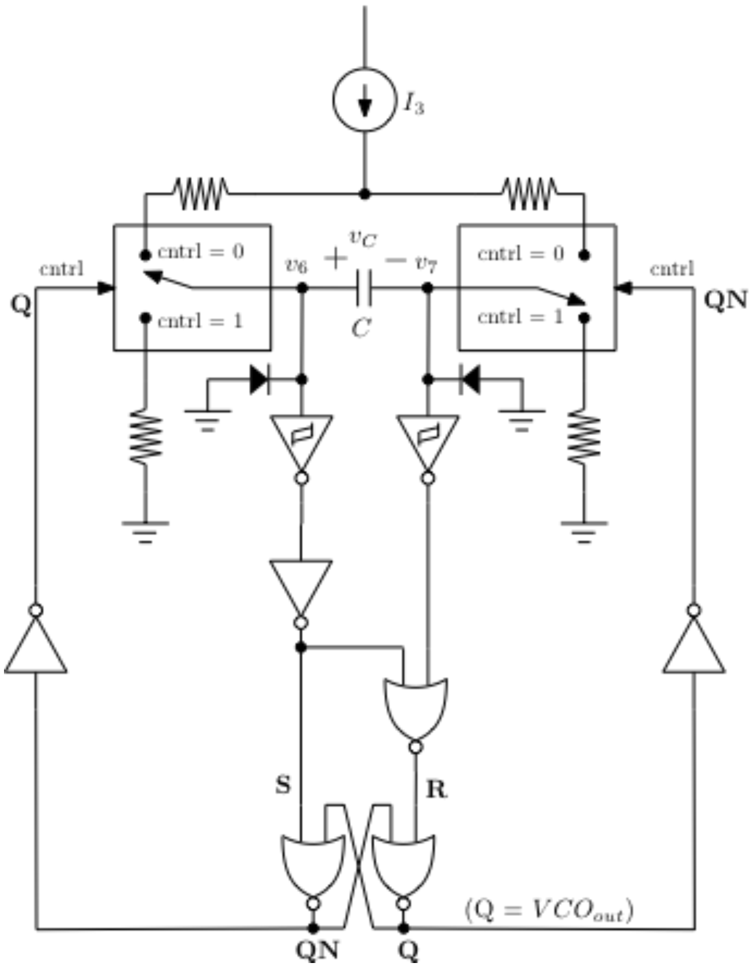


Better VCO Model



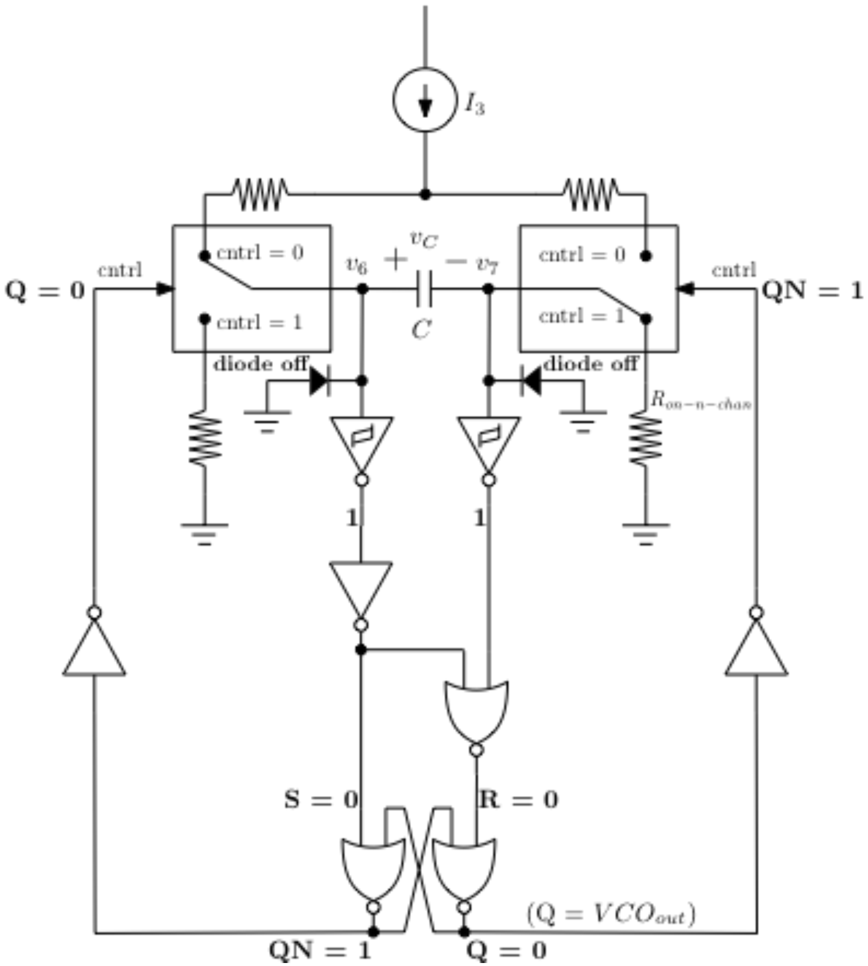
- Diodes from nMOS transistors included.
- Diodes from pMOS transitors not needed since they do not turn on in normal operation.
- nMOS on resistances are modeled ($R_{on\text{-}n\text{-}chan}$ from bottom of switches to gnd).
- pMOS on resitances have no effect since in series with I_3 source.

Better VCO Model – Summary of Operation Starting from Capacitor Uncharged and $\mathbf{Q = 0}$



1. Cap charges up until node 6 voltage reaches $V_H > 0$ threshold. Node 7 voltage small positive constant.
2. FF changes to $\mathbf{Q = 1}$ causing switches to reverse. Node 7 is clamped to -0.7 V partially discharging cap.
3. Clamping diode turns off and cap continues to discharge (i.e., charge in opposite polarity) until node 7 voltage reaches $V_H > 0$. Node 6 voltage small positive constant.
4. FF changes to $\mathbf{Q = 0}$ causing switches to reverse. Node 6 is clamped to -0.7 V partially discharging cap.
5. Clamping diode turns off. GOTO step 1.

Better VCO Model – Charging Nodes 6 → 7



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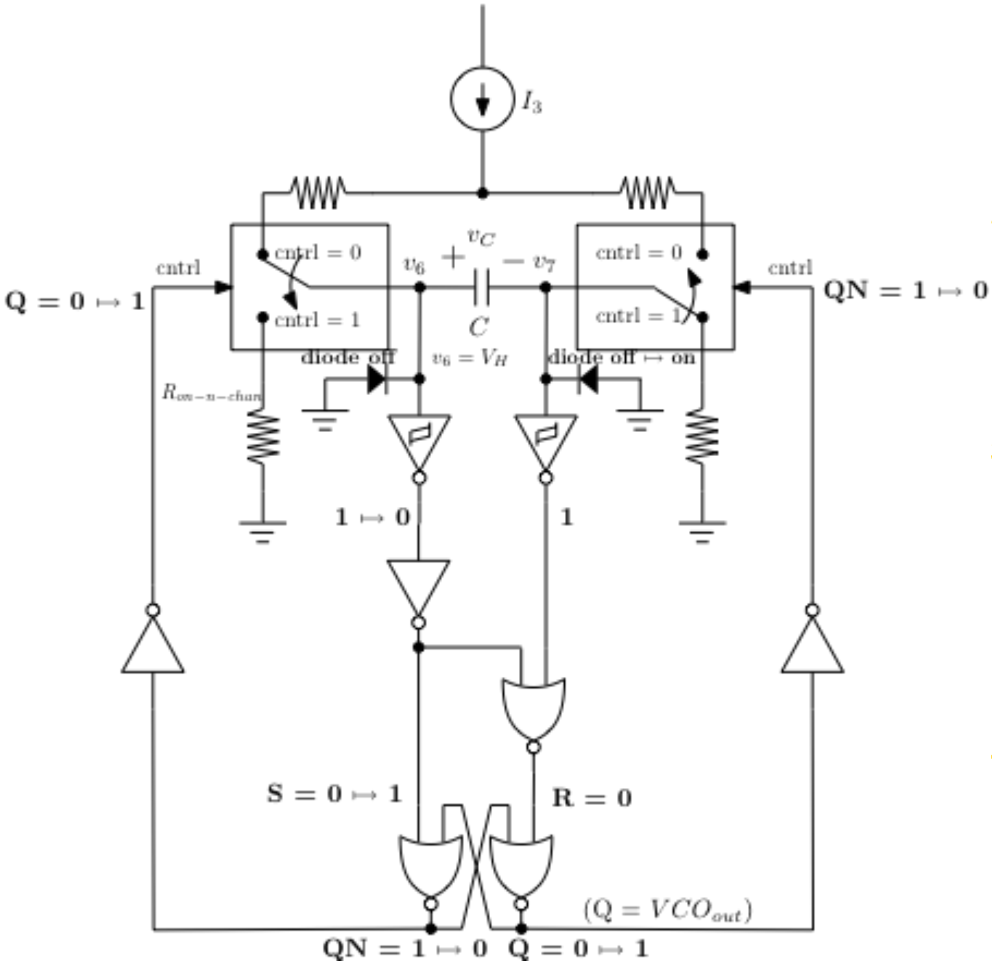
Better VCO Model – Charging Nodes 6 → 7 to Discharging Nodes 6 → 7



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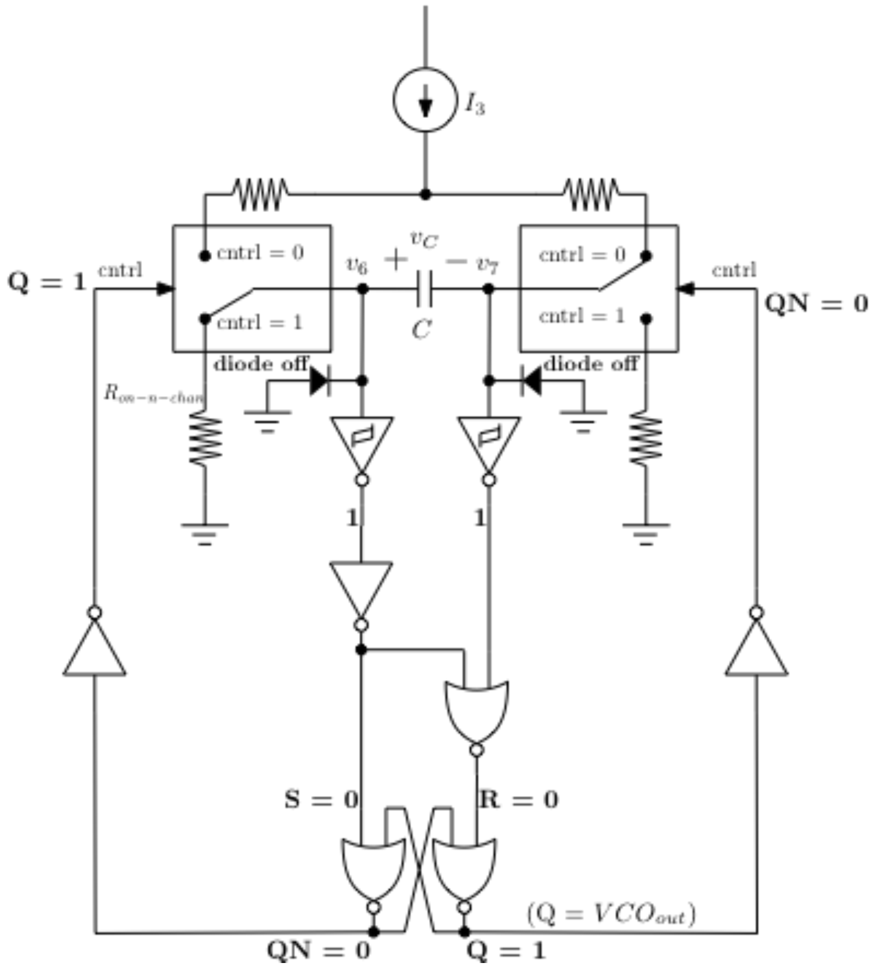
4. FF changes to $\mathbf{Q} = \mathbf{0}$ causing switches to reverse. Node 6 is clamped to -0.7 V partially discharging cap.
5. Clamping diode turns off. GOTO step 1.

Better VCO Model – Discharging Nodes 6 → 7



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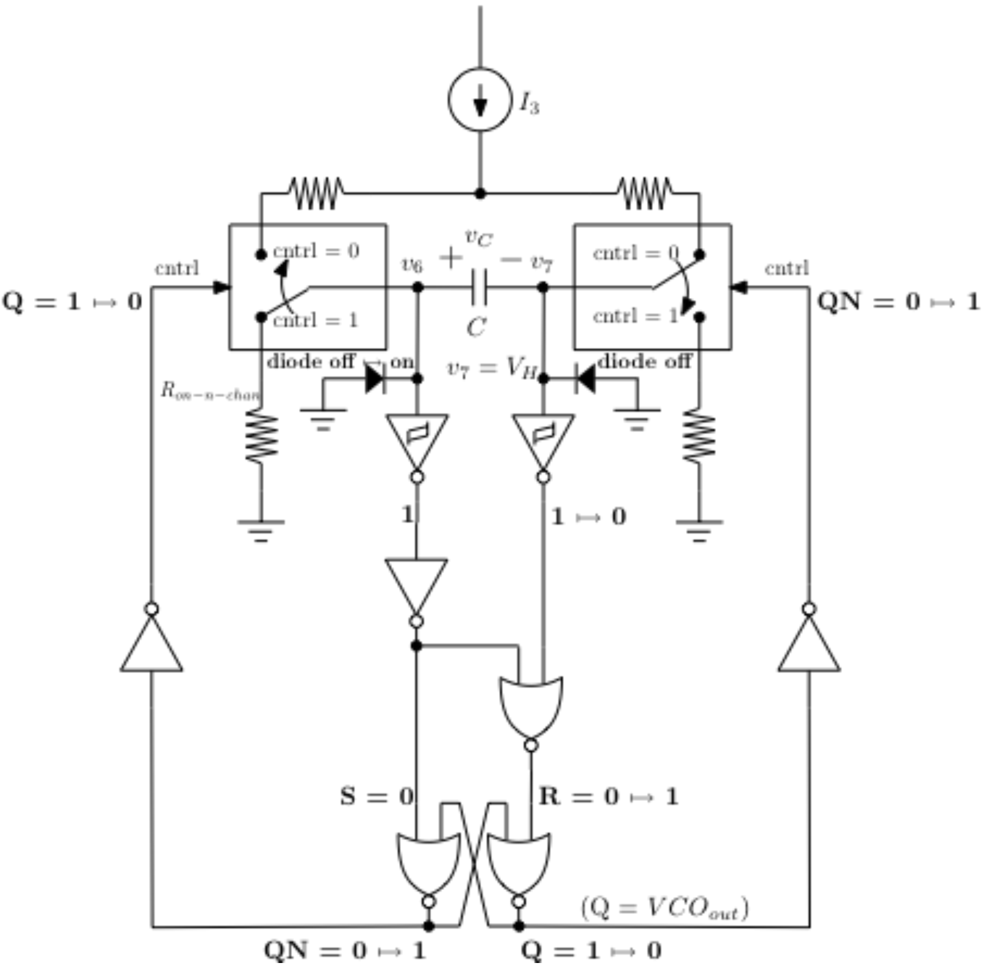
Better VCO Model – Discharging Nodes 6 → 7 to Charging Nodes 6 → 7



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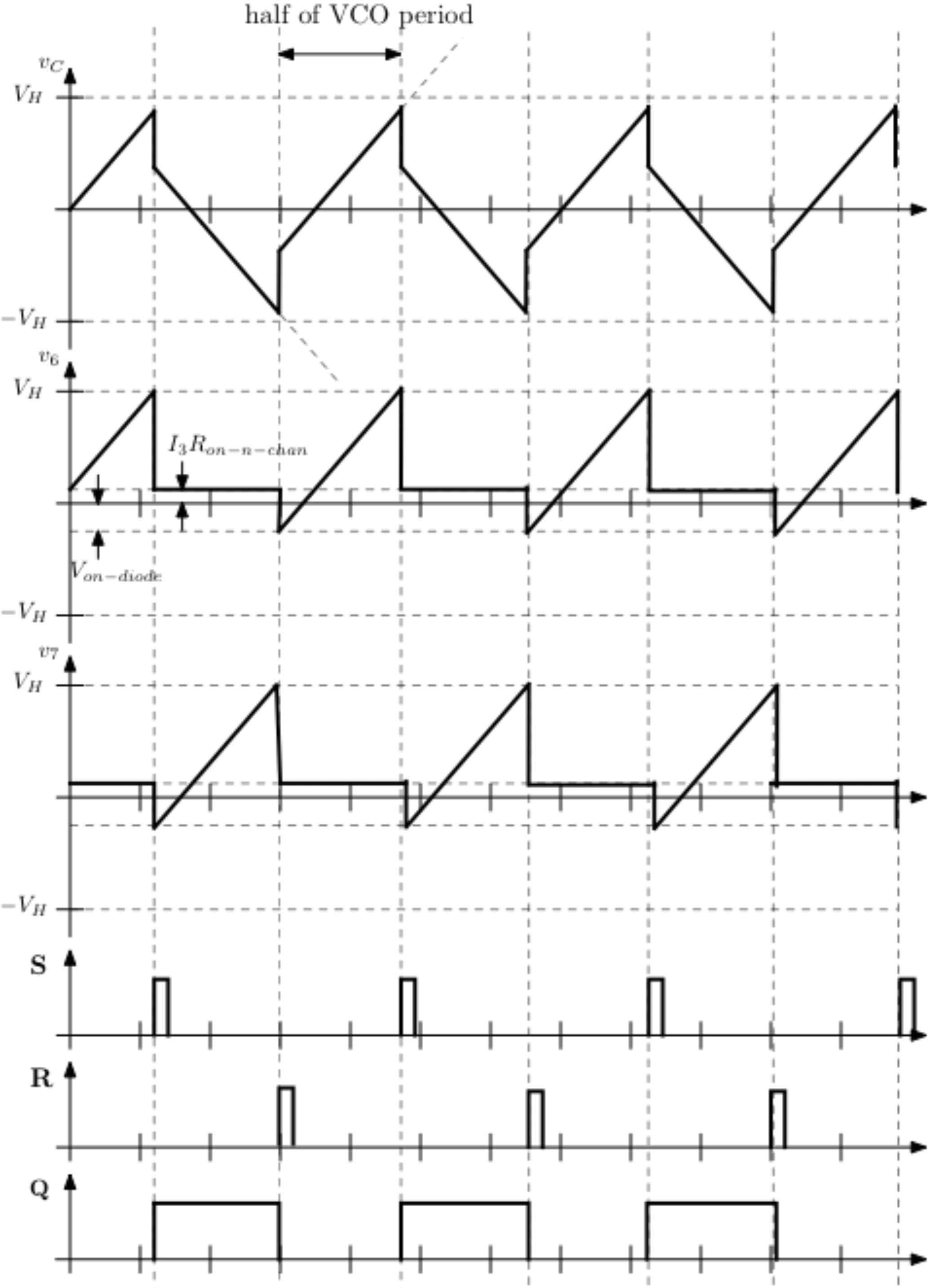
VCO Frequency Calculation



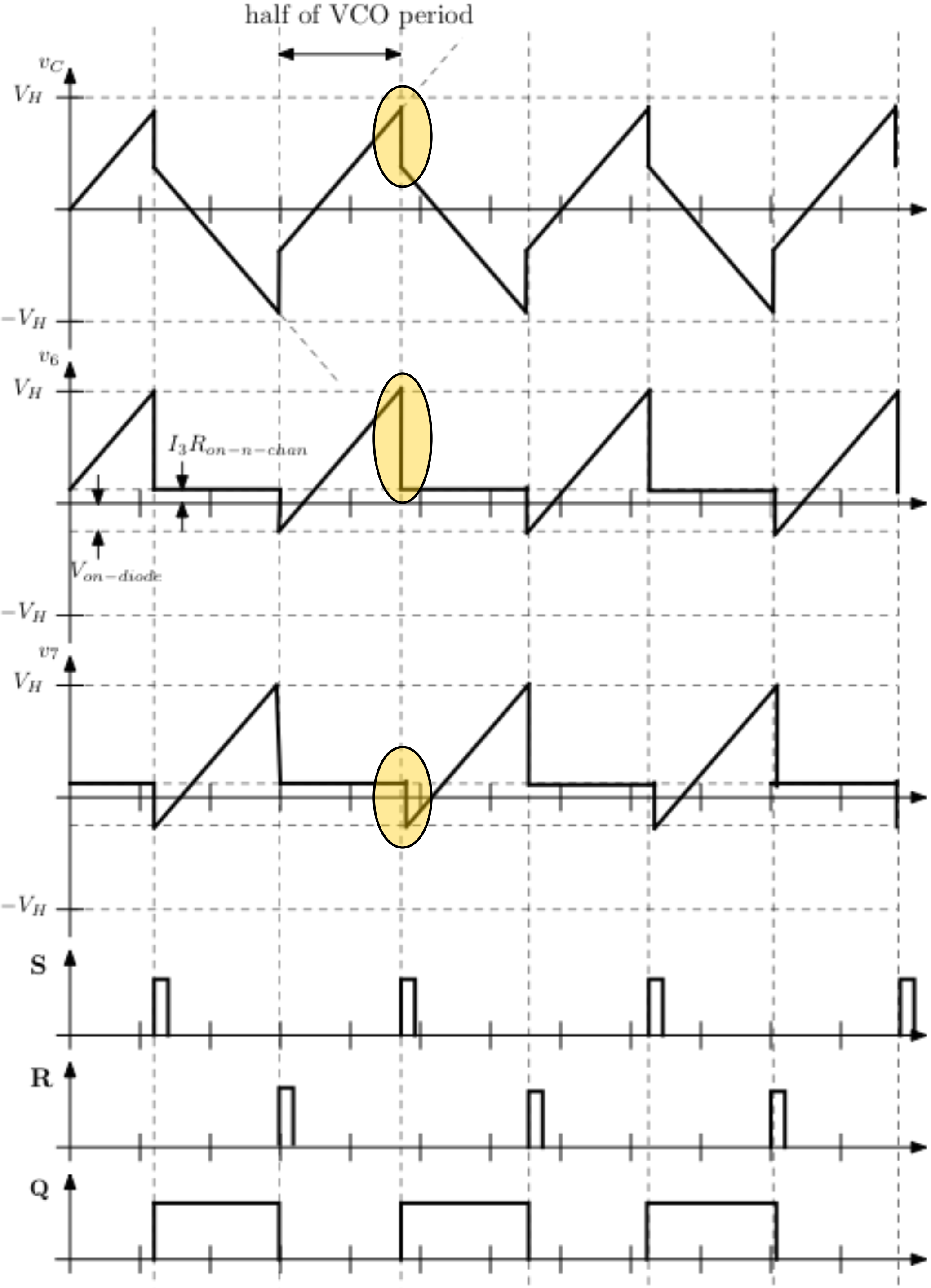
Half of $Q = VCO_{out}$ period is time it takes to charge capacitor through a voltage difference of $V_H + 0.7$ V with a constant current I_3:

$$V_H + 0.7 = \frac{I_3}{C}\frac{T_{VCO}}{2}$$

$$\downarrow$$

$$T_{VCO} = \frac{2(V_H + 0.7)C}{I_3}$$

$$f_{VCO} = \frac{I_3}{2(V_H + 0.7)C}$$



VCO Frequency Calculation

Further refinements come from modeling the time required to transition from charging to discharging, which includes two components:

- Propagation time in gates, flip-flop, and CMOS switches T_{pd}.
- Effect of diode clamping and RC decay T_{RC}.

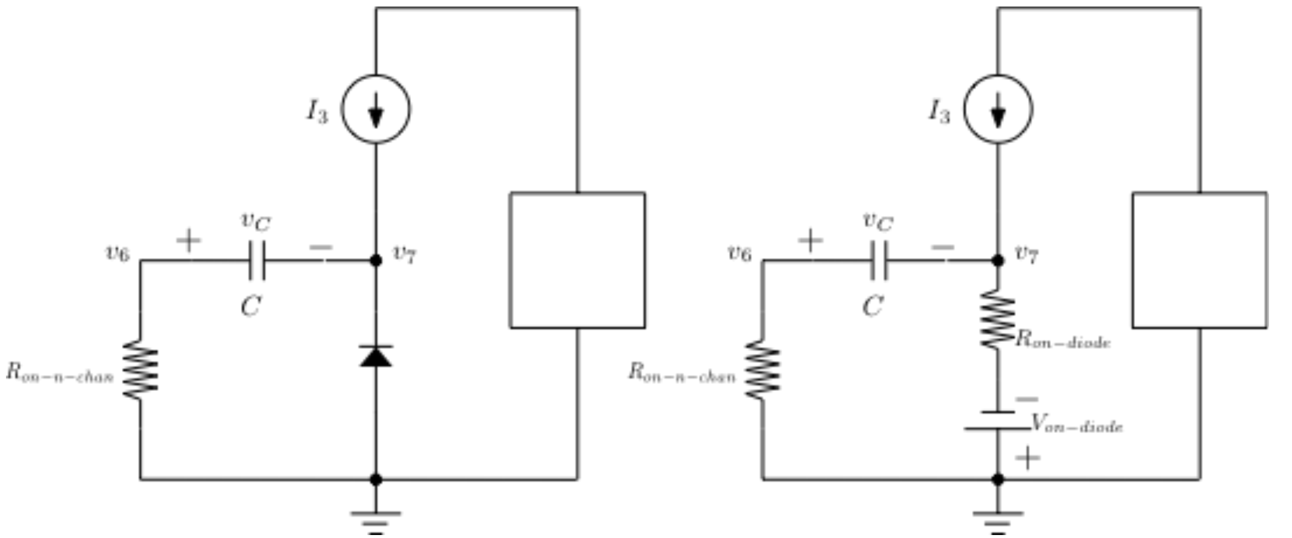
For all but the highest VCO frequencies, these effects should be minimal.

$$
\begin{aligned}
T_{VCO} &= \frac{2(V_H + 0.7)C}{I_3} + 2T_{pd} + 2T_{RC} \\
f_{VCO} &= 1/T_{VCO}
\end{aligned}
$$

Estimation of 2nd Order Refinements

- For this it is easiest to use some reasonable numbers from the datasheets:
  - T_{pd} = 10 to 14 ns.
  - V_{cc} = 5 V.
  - $R_1 = R_2$ = 10 kΩ.
  - VCO_{in} = 3 V → I_1 = 0.3 mA
  - $V_{ref} = V_{cc}$ - 0.6 V = 4.4 V → I_2 = 0.44 mA
  - $M_1 = M_2$ = 7 → I_3 = 5.2 mA
  - Voltage drop due to nMOS on resistance about 0.15 V → $R_{on\text{-}n\text{-}chan}$ = 30 Ω
  - V_H = 1.1 V
- Then can use simple model for clamping diode to calculate T_{RC}.

Calculation of T_{RC}



- For simplicity assume $R_{on-diode} = 0\ \Omega$.
- Assume switching occurs at $t = 0$. Circuit shown above is for $t > 0$.
- Summary at $t = 0^-$:
  - $v_6(0^-) = 1.1$ V
  - $v_7(0^-) = 0.15$ V
  - $i_C(0^-) = I_3 = 5.2$ mA
  - $v_C(0^-) = 0.95$ V
- Summary at $t = 0^+$: $v_C(0^+) = 0.95$ V

Calculation of T_{RC} (cont'd.)

- While the diode is forward biased can show:
  - $v_6(t) = 0.25e^{-t/1.5\text{ns}}$ V
  - $v_7(t) = -0.7$ V
  - $i_C(t) = -8.3e^{-t/1.5\text{ns}}$ mA
  - $v_C(t) = 0.7 + 0.25e^{-t/1.5\text{ns}}$ V
  - $i_{diode}(t) = 8.3e^{-t/1.5\text{ns}} - 5$ mA
- Diode turns off at the time t_* where $i_{diode}(t_*) = 0$, which is $t_* = -1.5\ln(5/8.3) = 0.76$ ns.
- At $t = t_*$:
  - $v_6(t_*) = 0.15$ V
  - $v_7(t_*) = -0.7$ V
  - $i_C(t_*) = -5$ mA
  - $v_C(t_*) = 0.85$ V
  - $i_{diode}(t_*) = 0$ mA

Calculation of T_{RC} (cont'd.)

- For $t > t_*$ the capacitor continues to discharge owing to the dc current source $I_3 = 5$ mA.

- That is
$$v_C(t) = -\left(100\frac{\text{mV}}{\text{ns}}\right)(t - 0.76\text{ns}) + 850 \text{ mV}$$

- To summarize: The above calculation yields $T_{RC} = 0.76$ ns, which is insignificant in comparison to propagation delays T_{pd}.

- Note that modeling the diode on resistance will increase the RC time.

VCO Frequency Characteristic

- For the circuit parameters previously given the nominal oscillator frequency is $f_{VCO} = 16.6$ MHz.
- If we vary the VCO input voltage over the allowed range from 1.0 V to 4.5 V we have

$$14.0 \text{ MHz} \leq f_{VCO} \leq 18.9 \text{ MHz}.$$