7.1 Review:

In the last lecture we considered various statistical methods used for evaluating the ‘goodness of fit’ of various probability density functions (PDF) with the experimental data. In particular we were interested in evaluating the tail of the distribution from a very few experimental results that are usually available. The tail of the distribution is interesting since we would like to know what % of samples will fail after a particular amount of time from the experiments done on a small number of samples for a limited amount of time. We also reviewed how to develop physics based models to get accurate estimates of the PDF. To illustrate these concepts, we discussed a generic problem of “BFRW” that could a prototype of any reliability problem defined as “a stochastic process terminated by a threshold”. From this lecture onwards we will specifically focus on the reliability problems in semiconductor devices, e.g. NBTI, HCI, TDDB, etc. in detail and apply the various techniques learned so far to describe them.

7.2 Yield vs. Reliability in Microelectronic Circuits

Yield and reliability are perhaps two of the most important aspects for the development of new technology. Yield is defined as the probability of failure of an as-processed device, while Reliability is defined as functional failure of the device during its operation (t≥0). A process with low yield (due to various extrinsic defects) is unacceptable to begin with, but even a process with high yield (low initial defects) but relatively large degradation rates (poor reliability) is unacceptably expensive in the long term. For microelectronics systems, reliability of various components is an issue of major interest since the microprocessors or memories are expected to function without failure for a long period of time (e.g. 10 years) under extreme operating conditions. We can classify these yield and reliability issues either from materials perspective or from device perspective, as discussed below.
7.3 Material Reliability

7.3.1 Bulk Material Reliability

For the bulk material, the yield may be poor due to point defects and dislocations present in the pristine semiconductor (For an excellent discussion of the intrinsic defects in semiconductor, Review Chapters 18-20 of Kittel’s book “Introduction to Solid State Physics”). On the other hand, once the device is fabricated, the operating temperature, voltage and humidity are some of the effects that create the defects in the device causing reliability problems. The bulk materials can be classified into three major categories:

**Semiconductors:** The success of any semiconductor as an mainstream IC material has always depended on its stability and reliability. For example, Galena (PbS) was one of the first semiconductor used for microelectronics application as a Schottky barrier diode for radio reception (patented by J. Bose in 1904). The stability and reliability of PbS was rather poor. Soon afterwards, therefore, vacuum tubes replaced this PbS-based detectors. Later in 1930, work began on Si/Ge at Bell Labs for a new semiconductor switch to replace failure-prone vacuum tubes. Silicon was chosen specifically because of its robustness and reliability. Silicon devices were hard to process due to higher processing temperature needed but they were found to be generally more stable than the PbS devices and eventually resulted in Silicon transistors that we use in electronics till this day. Another example that highlights the importance of reliability of bulk materials involves mid- to far-infra-red wavelength semiconductor lasers for molecular spectroscopy. These lasers were based on small bandgap lead salt semiconductors (e.g. PbTe, PbSe, etc.). Despite decades of work on this system, the material was unstable and suffered from poor reliability. Therefore, once the GaAs-based Cascade lasers were perfected, they rapidly displaced ‘lead salt’ based infra-red lasers from the marketplace.

**Insulators:** Gate insulator is an important component of any MOSFET. The difficulty in making reliable and defect-free gate insulators had thwarted the development of MOSFETs for many years, from 1940s to 1970s. The primary defects in insulators such as SiO$_2$ and Al$_2$O$_3$ involves missing O bonds that may or may not bridged by nearby Si or Al atoms, respectively. These bulk defects may
arise from processing imperfections or they may be created as transistors are turned on and off for an extended period of time. Indeed, generation of broken ‘Si-O’ bonds with continued circuit operation has been attributed to Time Dependent Dielectric Breakdown (TDBB) of gate insulators - a major reliability concern of MOSFETs. Many of these bulk defects are paramagnetic and detectable through electron spin resonance experiments (ESR). Although SiO$_2$ films has been perfected over last 40 years, the reduction of bulk defects in high-k gate dielectric (HfO$_2$, ZrO$_2$, etc.) continues to be the primary obstacle to the adoption of these insulators in mainstream high-performance Si ICs.

**Metals:** Metal layers are used as contacts, electrodes and interconnect. Modern IC have 7-9 layers of metallic interconnect. The major problems with metal is Electro migration (EM): the atoms of the metal are displaced by the “electron wind” – this creates voids in the metallic lines. Eventually, the voids grow to open-circuit the interconnects, resulting in functional failure of the IC.

### 7.3.2 Interface Reliability

Similar to the reliability of bulk materials as discussed above, the reliability of interfaces between two bulk materials is a significant concern for the semiconductor industry.

**SiO$_2$ and Si interface:** The semiconductor-oxide interface is critical in a MOSFET device and is a source of most of the major reliability problems such as Negative Bias Temperature Instability (NBTI) and Hot Carrier Degradation (HCl). One must differentiate reliability issue of NBTI and yield related issue of BTI. The bias temperature instability (BTI) due to presence of mobile Na$^+$ or K$^+$ ions was a major hurdle in the development of MOS ICs. BTI would shift the threshold voltage by as much as 20 V in a matter of 3-4 hrs in a device. However, BTI is maximized with positive voltage and minimized by negative voltage, while NBTI has the opposite voltage dependence.

**Ge – Si interface:** Another well-known interface-problem arises from interface between two semiconductors like Si on Ge or AlGaAs on GaAs, etc. The Ge and Si semiconductors are not lattice matched since the bulk lattice constants (lattice spacing etc.) are different for both these materials. When Ge layer is grown on top of Si crystal some defect lines may get formed which
traverse through entire crystal causing poor quality crystals unsuitable for device applications. It was found that the defects are not formed if the thickness of the Ge layer is below a critical thickness (1985). The Ge layer of higher thickness would form defects to relieve the stress due to lattice mismatch.

**Metal/Dielectric interface:** There are 7-9 layers of metal interconnects (Al or Cu) on the modern IC. These metal layers have traditionally been separated by dielectrics like SiO2 ($\varepsilon \sim 3.9$) or more recently by dielectrics like Black diamond with $\varepsilon=2.7-2.9$. Such interfaces are susceptible to delamination effects due to Stress Migration (SM). During stress migration, the different expansion coefficients of the metal and the insulators cause parts of some of the thin layers to peel off from each other causing shorts between adjacent metal interconnect layers.

### 7.4 Device Specific Reliability

In the discussion above, we have classified reliability issues in terms of material properties and differentiated between bulk and interface reliability. Another way to classify the reliability issues would be to look at individual devices and list their reliability issues. Since semiconductor devices
contain both bulk materials (e.g. substrate, oxides, etc.) as well as interfaces among them, we would anticipate a subset of both bulk and interface reliability issues would be relevant in this discussion.

7.4.1 MOSFET-based Logic Transistor

There are three major reliability concerns for MOSFET-based logic transistors: NBTI, HCI, and TDDB. NBTI and HCI are related to unsatisfied Si bonds at the Si/SiO2 interface, as shown in the figure above. These interface traps are passivated by annealing the sample in H\textsubscript{2} where each interface trap is annealed by one H atom through Si-H bond.

1. **NBTI - Negative bias Temperature Instability** (1960s and now): The hydrogen which attaches easily to Si dangling bond are also easily detached with electric field stress and temperature, recreating the original interface trap. This is a problem mainly in PMOS transistors and since PMOS was the dominant MOS transistor in 1960s and early 1970s, this problem was predominant at that time. But after the NMOS took over this problem went away and even after the advent of single poly CMOS with buried channel, NBTI was not really a big problem. But interest in NBTI was reignited by advent of dual poly CMOS with surface channel pMOS transistors as well as continued thinning of gate dielectrics.

2. **HCI – Hot Carrier Injection**: This problem appeared as the channel length was reduced below one micron but the operating voltage remained fixed to 5V due to compatibility issues with emitter coupled logic (ECL). The carriers reaching the boundary of channel and drain are hot due to high electric field and they knock out electrons in the Si-H bond near the drain region breaking the bond in the process and creating an interface trap. This issue is not as important these days because of reduction of the supply voltage.

![HCI schematic](image-url)
3. **TDDB – Time dependent dielectric breakdown:** Randomly generated defects get aligned and form a percolating path from gate to channel through the gate oxide as shown in the figure below.

![Fig. 4. Random defects generated by TDDB forming a continuous leakage path.](image)

The TDDB arises from bulk, broken ‘SiO’ bonds and has mainly two types:

a. **HBD - Hard breakdown:** Up until late 1990s, the high $V_{DD}$ resulted in significant transient current through the oxide as soon as the percolation path shorted the substrate to the gate. The corresponding increase in the local temperature was high enough to cause formation of additional defects around the percolation path, resulting in unacceptable level of gate leakage. Sometimes the heating was significant enough to melted of Silicon, completely destroying the transistor in the process. HBD was the dominant mode of breakdown until just a few years ago (circa 2000).

b. **SBD - Soft breakdown (97 - now)** – When the supply voltage was reduced, HBD was no more possible as the transient short-circuit current was not high enough to melt the Si or even to form new defects around the percolation path. Although the gate leakage current would go slightly up as a result of a breakdown but the device would still be able to operate. Without this transition from HBD to SBD, Moore’s law could not continue.
3. **Radiation Damage**: High energy particles present in outer space (neutrons) or some of the packaging material (alpha particle) can lead to IC failure. Radiation induced damage has always been a significant problem for NASA and the defense industry. And this is becoming an important issue for even core semiconductor technology.

4. **Electro static discharge** (ESD): A very high transient voltage (> several volts) can be generated on a device designed to withstand only 1V due to many reasons e.g. a person touching the device. The duration of the pulse is very short but the device may fail as a result of ESD. ESD is really a form of transient TDDB and will be discussed at the same time TDDB issues are considered.

### 7.4.2 Semiconductor Flash Memory

Semiconductor memory is an important component of modern microelectronics. In Flash memories, the absence or presence of stored charge in the floating gate (white region sandwiched between gate insulators, see Fig. below) changes the threshold voltage of a transistor, and as such indicates logic levels 1 or 0. Flash devices have their own specific reliability issues: The high voltage used to inject charges in the floating gate makes gate/drain junction susceptible to HCI damage. Radiation may eject the trapped electrons from the floating nodes, with the corresponding loss of the information stored at the node. And finally, Stress induced leakage current (SILC, precursor to TDDB) caused by formation of bulk oxide defects is a major problem for Flash transistors. The SILC-related defects do not completely short the floating gate to the channel but the stored charge may be lost due to leakage, eventually resulting in memory failure. The bits with such excessive leakage is called “Anomalous bits” and even a small fraction of such bits may render a technology unsuitable for practical applications.

![Fig. 5 Schematic diagram of flash memory](image-url)

Oxide thickness: 7~8nm
In this course, we will not have time to Flash memory related reliability issues. However, if we understand the reliability issues of logic transistors, you may often be able to translate them not only to Flash memories, but to other components like Dynamic Random Access Memory (DRAM), I/O transistors, etc.

7.4 Conclusions:
In this lecture we discussed the concepts of ‘yield’ vs. ‘reliability’. We also differentiated between material aspects of reliability with reliability concerns for specific semiconductor devices. From next lecture, we will consider each of these reliability phenomenon in detail. We will begin with NBTI phenomenon.