32.1- Background and Mechanism

Hot carrier injection is another degradation mechanism observed in MOSFETs. The main source of the hot carriers is the heating inside the channel of the MOSFET during circuit operation and not at the “anode” as happens in the anode-hole injection model. These energetic carriers can lead to impact ionization within the substrate and the generated electrons or holes inside the channel or the heated carriers themselves can be injected in to the gate oxide. During this process, the injected carriers can generate interface or bulk oxide defects and as a result, the MOSFET characteristics like threshold voltage, transconductance, etc. degrade over time.

Hot carrier stress conditions are inherent in CMOS circuit operation. Figure 1(a) shows a CMOS inverter with input terminal A and output terminal B. When $V_A$ is high ($V_{DD}$), the NMOS experiences TDDB stress whereas the PMOS is OFF. As the gate terminal of the NMOS, $V_G=V_A$, switches from high to low (= 0 V), the drain bias, $V_D=V_B$, begins to increase. When $V_G \sim V_D/2$ (not $V_{DD}/2$!), the NMOS goes through the maximum hot carrier stress condition (explanation is provided below). Eventually, when $V_A$ becomes low, the NMOS is OFF and the PMOS undergoes NBTI and TDDB. It is the high-to-low transient of $V_A$ (not the stable DC part) that contributes to HCI during inverter operation.

Figure 1: (a) CMOS inverter, (b) high-to-low transient of the $V_A$ along with the transition of $V_B$, and (c) drain current of the NMOSFET during the transient.
The reason why hot carrier degradation peaks at $V_G \sim V_D/2$ can be understood by looking at the energy band diagrams shown in figure 2. When the NMOS stressed under $V_G \sim 0$ and $V_D = V_{DD}$ (Fig. 2(a)), the horizontal (source-to-drain) energy band (red lines) are bent significantly near the drain side and, hence, there is a high electric field which can accelerate electrons towards the drain. However, since the transistor is not ON, the electron density in the channel is very small. The electrons which can enter the high-field region can gain energy and cause impact ionization. The holes generated from impact ionization can be injected into the oxide due to favorable electric field between gate-to-drain (Fig. 2a, bottom), and constitute the gate current (see figure 3, Region I). The hot electrons, on the other hand, will be repelled by the electric field and very little fraction of them can enter the gate as seen in the gate-drain band diagram (figure 2(a), bottom).

![Figure 2: NMOSFET energy bands for three cases at $V_D = V_{DD}$: (a) $V_G \sim 0$ (b) $V_G \sim V_D/2$ (c) $V_G \sim V_D$. Middle schematic shows the horizontal energy bands (source-to-drain) and the bottom one depicts the bands in the vertical direction (gate-to-substrate).](image)

When the gate bias exceeds the threshold voltage so that $V_G \sim V_D/2$ (Fig. 2(b)), the number of channel electrons increases significantly since the barrier $\Phi_B$ is reduced. The horizontal electric field near the drain is reduced slightly due to the gate-induced vertical field, and the hot electrons can undergo interaction with phonons in this region and subsequently lose energy. Thus, the holes generated through impact ionization by these electrons in the drain region are of lower energy. This along with the fact that electric field is reduced close to the drain. As a result both the efficiency of holes generation as well as injection probability of the holes into the oxide is reduced. This results in reduction in hole component to the gate current as seen in figure 3(top). The hole and electron components of the gate current have opposite
polarity, therefore the increasing electron component eventually cancels the hole component (see $I_{G,Net} = 0$ in figure 3(top)) and then dominates the gate current (Region II in figure 3(top)).

As the gate voltage is increased further towards $V_G = V_D$ (Fig. 2(c)), the channel electric field close to the drain region reduces because

$$E_x = \frac{V_D - V_{D,SAT}}{l},$$

where $V_{D,SAT}$ is the saturation voltage and $l$ is the pinch-off length (100 – 300 nm) near the drain. The $V_{D,SAT}$ increases with $V_G$ and thus, the field which accelerates electrons decreases with increase in $V_G$. Although the number of electrons increases with $V_G$, their energy (i.e., hot carriers) decreases, so impact ionization efficiency diminishes. Thus, with increase in gate voltage, while $V_G < V_D$, the electron current increases while the hole current decreases as shown in figure 3(top). If the gate bias exceeds $V_D$, the picture is similar to the previous case. The electron density gets higher but the hot electrons that can degrade the MOSFET is reduced.

*Figure 3: Electron and hole components of the gate current (top), net gate current (middle) and type of degradation (bottom) in different regimes of $V_G$. The magnitudes of the degradation components are arbitrary.*
Overall, the amount of hot carriers injected into the gate reflects a competition between two mechanisms: Given a fixed $V_D$, the number of electrons which can potentially impact ionize, increases with the gate voltage. However, at the same time, the energy they gain from the electric field near the drain decreases following (1). This leads to a bell-shaped degradation curve for the MOSFETs as shown in figure 3 (Region II).

The hot carriers directed towards the gate oxide can cause degradation by breaking the chemical bonds. As discussed in the previous lectures, hot holes generally break Si-O bonds, therefore in the regime where hot holes are present, the degradation is mostly due to broken (interface and bulk) Si-O (Region I in figure 3). In the $V_G \sim V_D/2$ regime (Region II), the number of hot electrons increases significantly, resulting in increase in density of broken Si-H bonds (generating $N_{IT}$, justified by isotope experiments). For high $V_G \geq V_D$, the hot carrier density decreases and, hence, the degradation is reduced. If the $V_G$ is high enough, the electrons injected into the gate can be trapped in the oxide and can cause shift in threshold voltage ($V_T$).

32.2 Experimental observations of HCI

32.2.1 Time-dependence:

Hot carrier degradation has been studied widely to assess the reliability implications. The degradation was found to be mainly interface traps (for $V_G \sim V_D/2$) related by the isotope experiment. The deuterium-passivated MOSFETs showed a distinctly smaller magnitude (2-3 times) of degradation compared to hydrogen passivation as schematically shown in figure 4. This implies that the damage is due to interface trap generation by Si-H bond breaking, similar to NBTI. Furthermore, NMOS HCI also shows power-law ($\sim t^n$) time dependence, with time exponents in the range of 0.3 to 0.70. PMOS, however, show $-\log t$ behavior reflecting a hole-trapping saturation induced shift in the degradation region.

Figure 4: HCI shows power-law time dependence. The degradation is dominantly interface trap related. From the experiments done on deuterium doped Si, the source of $N_{IT}$ was determined to be the breaking of Si-H bonds, at $V_G \sim V_D/2$ condition.
32.2.2 Voltage dependence

When operating voltages ($V_{DD}$) are increased, for a given gate voltage, the carrier gets hotter and hence, the ionization efficiency increases, leading to greater effect of HCI degradation (figure 5). The voltage acceleration is similar to AHI for thick oxides ($\sim e^{A/V}$). By using this trend, accelerated degradation experiment results can be extrapolated to operating conditions.

![Figure 5: Schematic of voltage dependence of HCI. The degradation increases with increase in $V_{DD}$. The acceleration is similar to the case of AHI.](image)

32.2.3 Temperature dependence

Another observation of HCI is the temperature dependence. Two factors are relevant: As the stress temperature decreases, there is a small increase in bandgap of Si (from 1.1 eV at 300K to about 1.15 eV at 100 K), implying lower impact ionization and, hence, lower degradation. This trend is countered by the fact that at lower temperatures phonon scattering of channel electrons is also reduced which leads to increase in the average energy of the electrons and as such an increase in the impact ionization rate. On balance, impact-ionization increases with lower temperature. Thus, for equal amount of applied stress, a MOS device at lower temperature will have larger number of hot carriers being injected leading to hole ionization and hence leading to larger device degradation. This enhancement of degradation at lower temperatures is shown in figure 6 for $V_{DD} > 2.5$-3V.

![Figure 6: HCI degradation increases significantly as temperature decreases. The scattering of channel electrons cools the carriers that can break chemical bonds.](image)
32.3 Summary

Degradation due to hot carrier injection and its mechanism are discussed. The degradation is mainly due to Si-H breaking and interface trap generation at maximum hot carrier stress conditions \((V_G \sim V_D/2)\). The time-, voltage-, and temperature dependences are also presented. By using the fact that both NBTI and HCI are related to Si-H bond breaking and show power-law behavior (with different time exponents), in the next lectures, the R-D model will be extended for HCI, and, recovery and AC characteristics will be discussed. Additionally, the physics of “\(k_F\)” due to hot carriers in the context of HCI will be discussed.