ECE-606 Homework No. 11 Assigned: Nov. 27 Due: Dec. 4

1) Consider an MOS capacitor on a p-type silicon substrate. The oxide capacitance is 2 x 10^{-7} F/cm^2, the metal-semiconductor work function is -1V and a positive charge Q_F = 8 x 10^{-8} C/cm^2 resides at the interface. There is no charge in interface states. Using the above information calculate the following quantities.

   a. Flat-band voltage

   b. Electric field in oxide when the capacitor is biased at flat-band

   c. If the acceptor density is 10^{16} cm^{-3}, calculate the surface potential that would be required to make the electric field in the oxide exactly equal to zero.

2) Solve SDF 17.2

3) Solve SDF 17.9

4) In a short channel MOSFET, the threshold voltage decreases with decreasing channel length and increasing drain-source bias. Explain these two effects and describe how you can minimize it.

5) For a MOSFET operating in the sub-threshold regime, the reduction in gate voltage needed to reduce the drain current by one decade is defined as the "sub-threshold swing. The units of *S* are mV/decade.

   Using this definition, prove that the smallest value of *S* attainable at room temperature (300K) is 60mV/decade. What is the typical range of *S* in a modern MOSFET?

   Bonus: Which modern device has a sub-threshold swing lower than 60mv/decade? Explain.

6) Explain concisely the following terms generally associated with short-channel MOSFETs.

   a. Drain-induced-barrier-lowering (DIBL)

   b. Gate-induced-drain-leakage (GIDL)

   c. Lightly-doped-drain (LDD)

7) For the fabrication of an n-channel MOSFET, the starting material is a p-type silicon wafer of (100) orientation. Write down the process steps needed to fabricate a self-aligned MOSFET for integrated circuits.