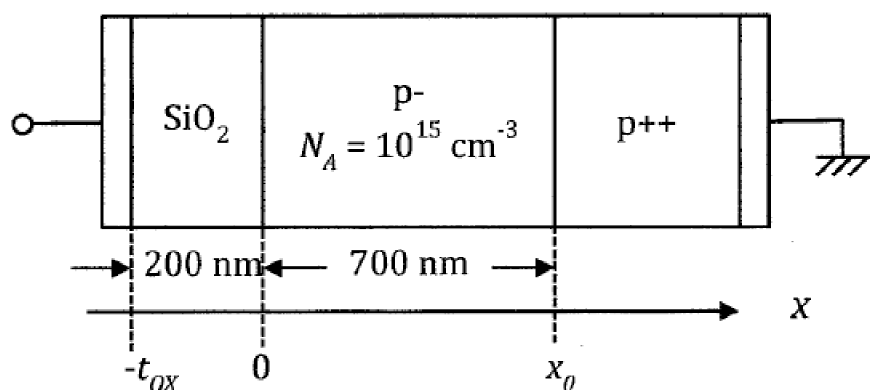
ECE-606 Homework No. 10 Assigned: Nov. 20 Due: Nov. 27

1) An MOS capacitor is fabricated on a lightly doped p-type silicon layer on a **p+** silicon substrate as shown in the figure below. The **p-** layer is 700 nm thick and is uniformly doped with acceptors at a density of 10^{15} cm^{-3}. The oxide thickness is 200 nm. The **p+** substrate is so heavily doped that is the surface depletion region should reach it, any penetration of the depletion layer in to the substrate can be considered negligible.



Compute the surface potential required to produce a depletion width of 500 nm.

2) Solve SDF 16.12

3) Solve SDF 16.13

4) Many complications arise as MOSFET devices are miniaturized. The class of effects that alter device behaviour due to device miniaturization are known as short-channel effects. Itemize the most important features that arise in a short-channel MOSFET.

5) An ideal MOS diode is fabricated on a p-type silicon substrate having a doping concentration of N_A = 10^{16} cm. What is the work function of the silicon substrate at room temperature?

The following data about silicon is given below.
$\mathbf{E_g = 1.1}$ **eV**, $\boldsymbol{\chi}$ **= 4.05 V**, $\mathbf{n_i = 1.5 \times 10^{10}}$ $\mathbf{cm^{-3}}$ at 300 K. The threshold voltage at this temperature is **26 mV**.

6) For the device considered in Q5, calculate the hole concentration, electron concentration and the charge density at the semiconductor surface for Ψ_s = 100 mV.

7) Consider the device in Q5 again: If the gate oxide thickness is 1000 A, calculate the maximum depletion width and threshold voltage. Dielectric constant for silicon and silicon dioxide is 11.9 and 3.9 respectively.