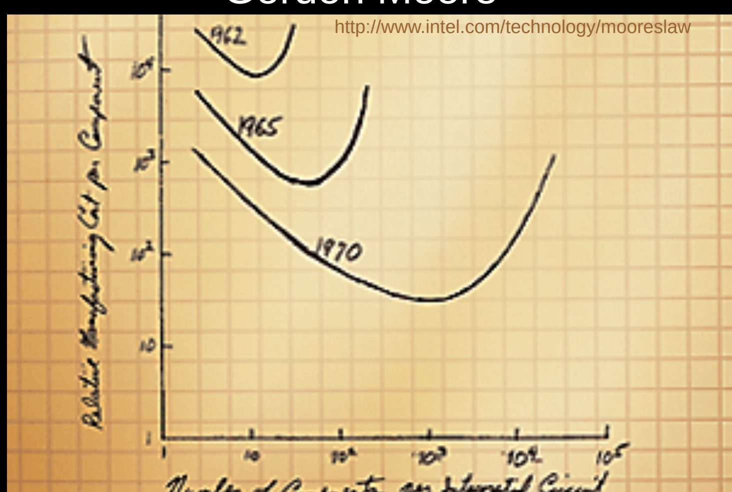
nanoHUB.org

ECE606: Solid State Devices
Lecture 26
The Single Atom Transistor
Future Transistors
New Modeling Tools (NEMO)
nanoHUB: Cloud Computing - Software as a Service

Gerhard Klimeck
gekco@purdue.edu

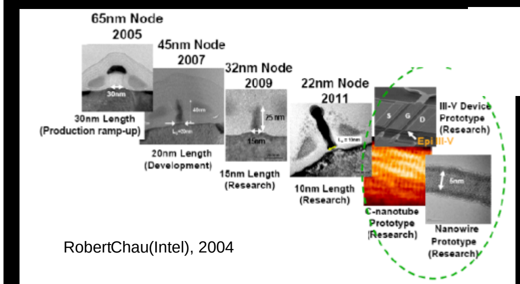
1965
Gordon Moore

Relative Manufacturing Cost per Component

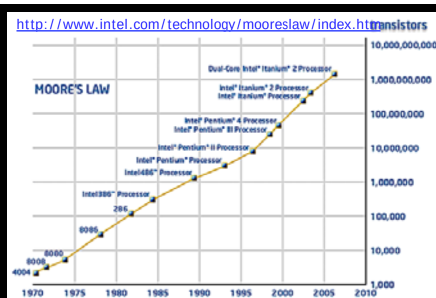


Number of Components per Integrated Circuit

Intel in 2012



RobertChau(Intel), 2004



Device Size:
Tens of nanometers
Stanford SUPREM

Device Integration:
>2 Billion
Berkeley SPICE

Berkeley

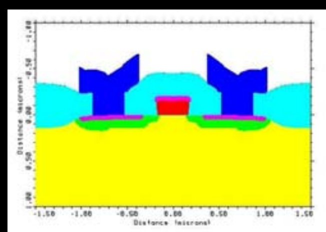
Simulation Program with Integrated Circuit Emphasis.

SPICE Pioneers today at Mentor Graphics:
Ellis Cohen - "unspoken hero of SPICE"
Thomas Quarles – SPICE3 – C - expandable

from: Larry Nagel, BCTM '96

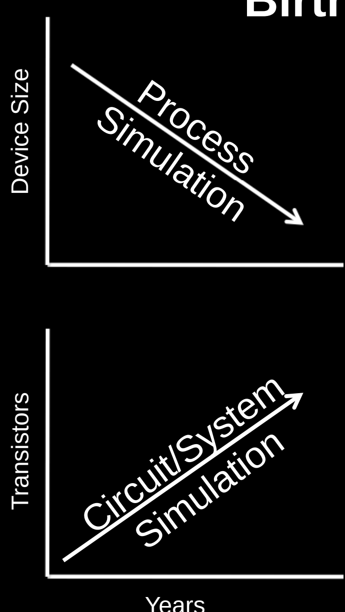
- Started as a class project
- Developed as a teaching tool
- Quality control: pass Pederson
- Dissemination:
  - Public domain code
  - Pederson carried tapes along
  - Students took it along to industry and academia
- Released 1972

Stanford
Stanford University PRocEss Modeling

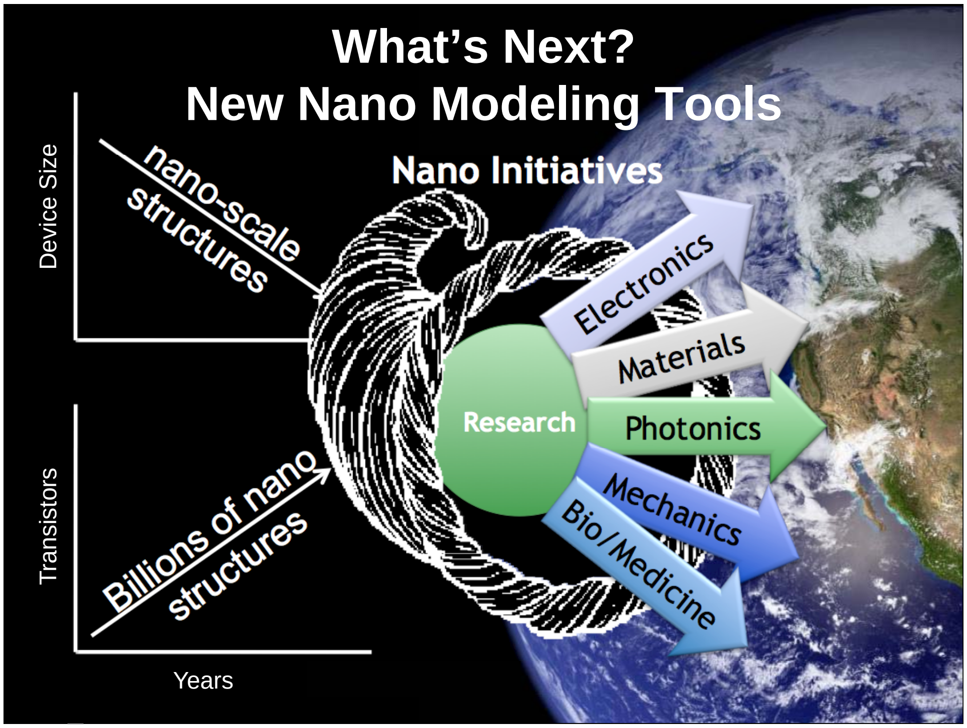


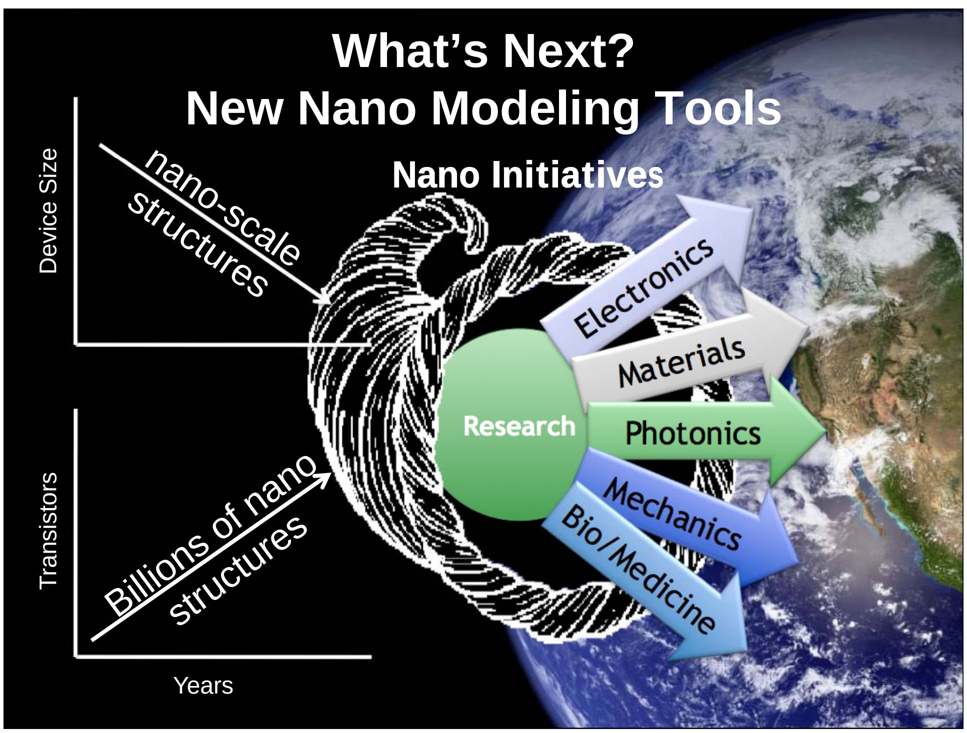
- Stanford wanted to mimic Berkeley success
- Combine various existing models
- Dissemination:
  - Public domain code
  - Community workshops
  - Students took it along to industry and academia

Birth of an Industy



Intel Capitalization:
$85B
Total Industry:
$280B


What's Next?
New Nano Modeling Tools
Nano Initiatives
Device Size
nano-scale structures
Transistors
Billions of nano structures
Years
Research
Electronics
Materials
Photonics
Mechanics
Bio/Medicine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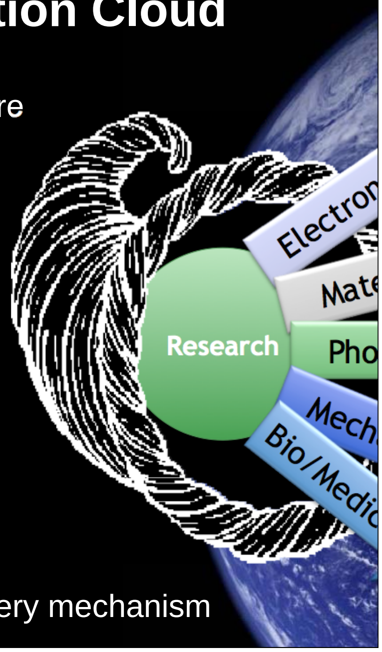
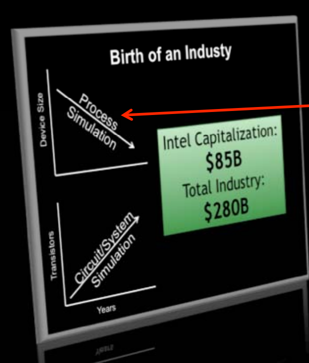
nanoHUB: A Science Simulation Cloud

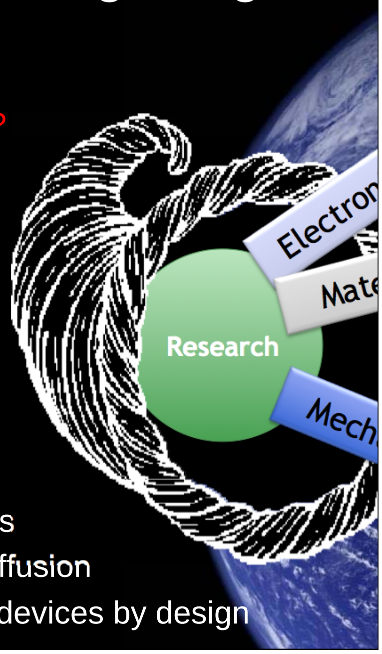
- Services:
  - Modeling and Simulation Software
  - Seminars, tutorials, classes
- Goals:
  - Knowledge transfer
    - Use in class rooms
  - Knowledge generation
    - Use in research
    - Use by experimentalists
  - Economic impact
    - Use in Industry
  - Professional Development / Community building
- Software as a service - A new delivery mechanism



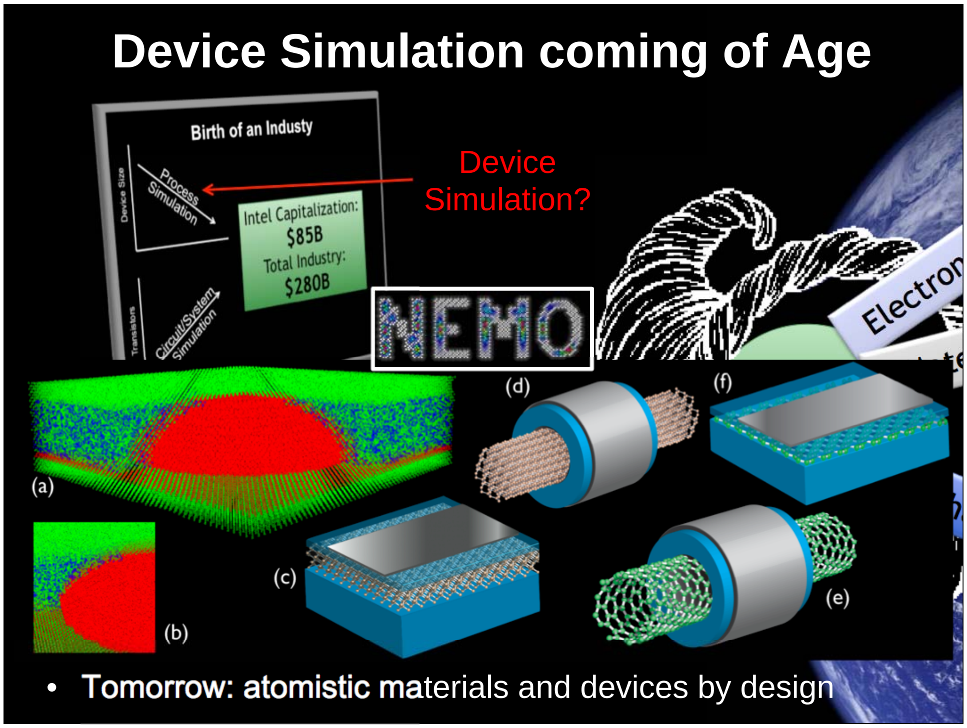
Device Simulation coming of Age



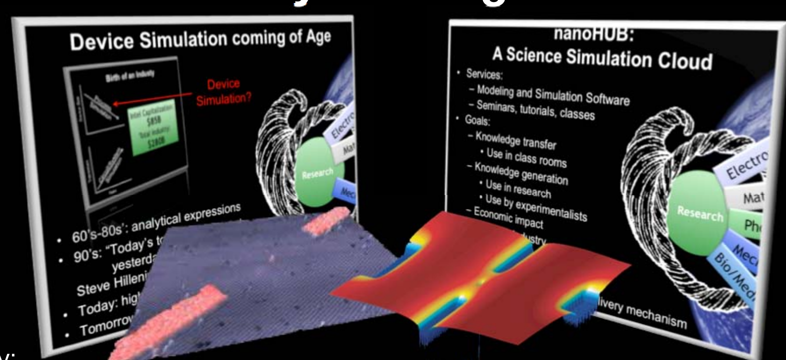
Device Simulation?



- 60's-80s': analytical expressions
- 90's: "Today's tools simulate yesterday's transistors", Steve Hillenius, Bell Labs
- Today: highly parameterized drift diffusion
- Tomorrow: atomistic materials and devices by design



Key Messages



Today:

- Drift Diffusion fit to atomistic model

Tomorrow:

- Quantum at the core
- 5nm transistors with metals by design

Future:

- Wires: 1 atom tall, 4 atoms wide
- Transistor made of one P atom
- Quantum computing

Today:

- Software as a service delivered to thousands in an open science gateway
- No code rewrite needed

Tomorrow:

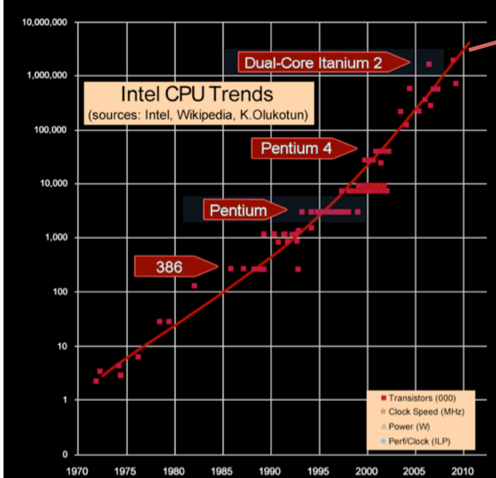
- Vendors embrace software as a service

The single-atom transistor

Presentation Outline

- Why?
  - A power problem
  - Near term solution
  - Continuum invalid
    => finite atoms/electrons
- What is it?
  - Coulomb diamond
  - How is it built?
- How to model this?
  - NEMO
- Where to study this?
  - nanoHUB.org

Moore's Law Forever?

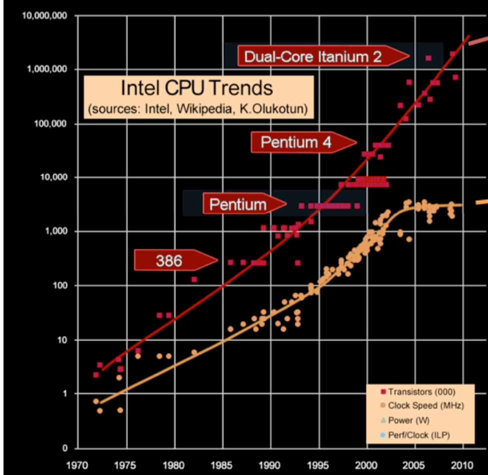


Number of transistors:
Moore's law is continuing

http://jai-on-asp.blogspot.com

2005: free lunch is over, updated 2009

CPU's are not getting faster!



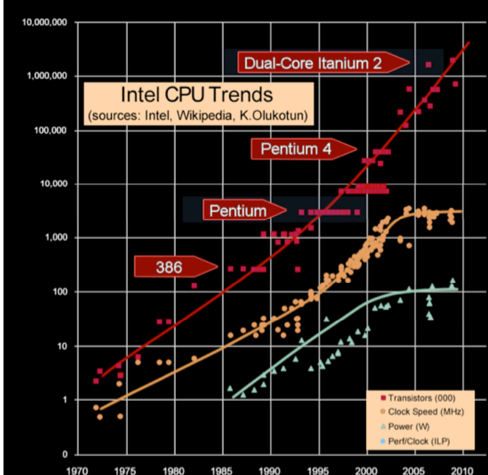
Number of transistors:
Moore's law is continuing

Clock speed:
no longer scaling

http://jai-on-asp.blogspot.com

2005: free lunch is over, updated 2009

Power is the Limit!



Number of transistors:
Moore's law is continuing

Clock speed:
no longer scaling

Power:
today's limitation
~100W

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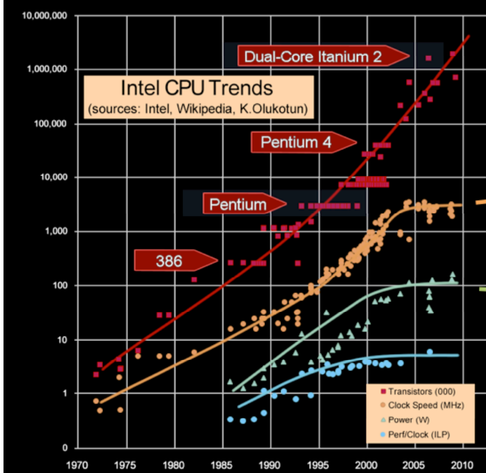
2005: free lunch is over, updated 2009

Limited Performance Improvements



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2005: free lunch is over, updated 2009

Number of transistors:
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Clock speed:
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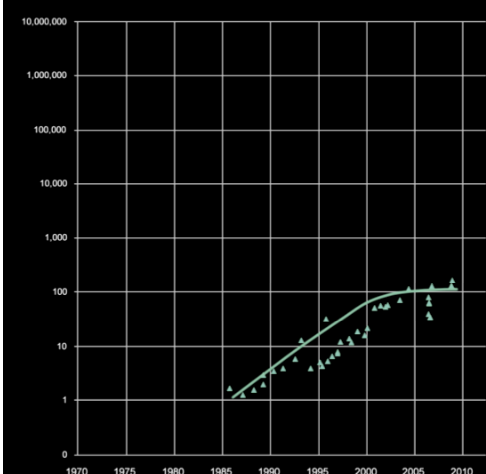
Power:
today's limitation
~100W

Performance Gain:
limited

Supply voltage (Vdd) stopped scaling at around 2003

What is Special about 100W ?



http://jai-on-asp.blogspot.com

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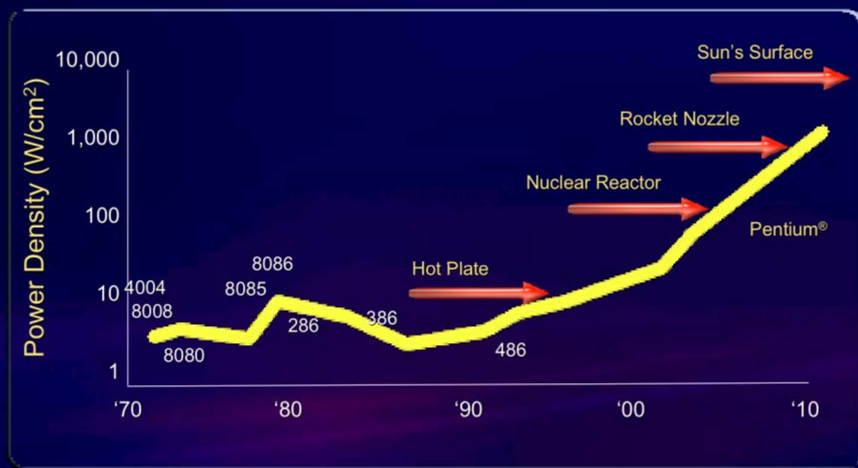
Power:
today's limitation
~100W

Intel Projection from 2004

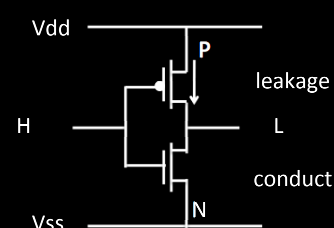
How do we burn power?

Switching Circuits & Leakage => Transistors



Intel Developer Forum, Spring 2004 - Pat Gelsinger

CMOS Inverter



Dynamic / Switching Power:

- Charging a capacitor network

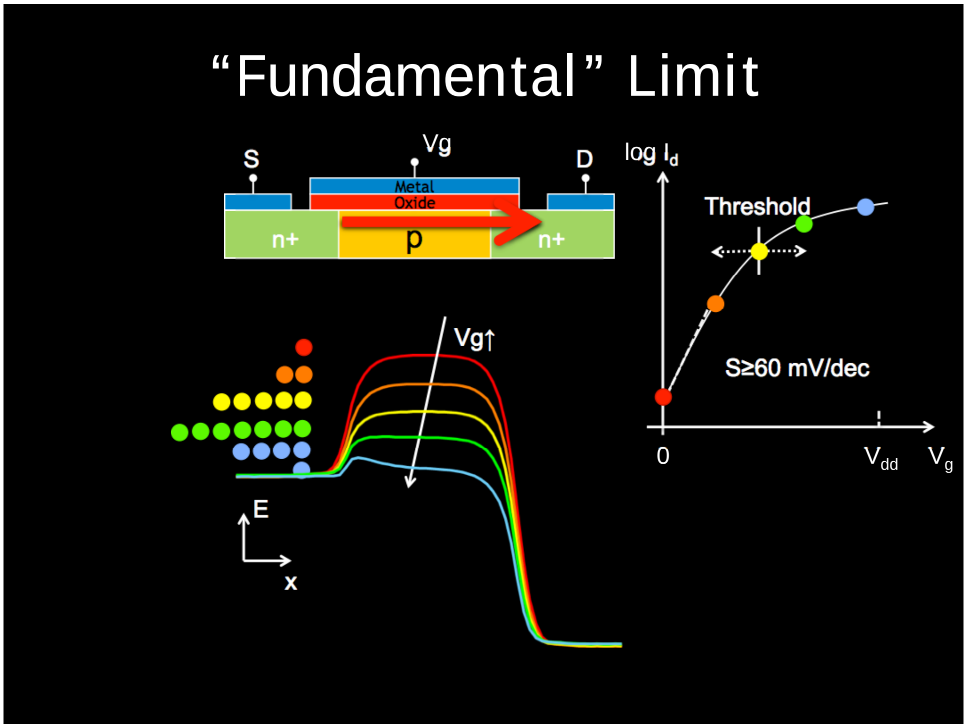
$$P \propto f\, C_L\, V_{dd}^2$$

- Reduce frequency ☹
- Reduce capacitance
  => device size ☺
- Reduce voltage ☺

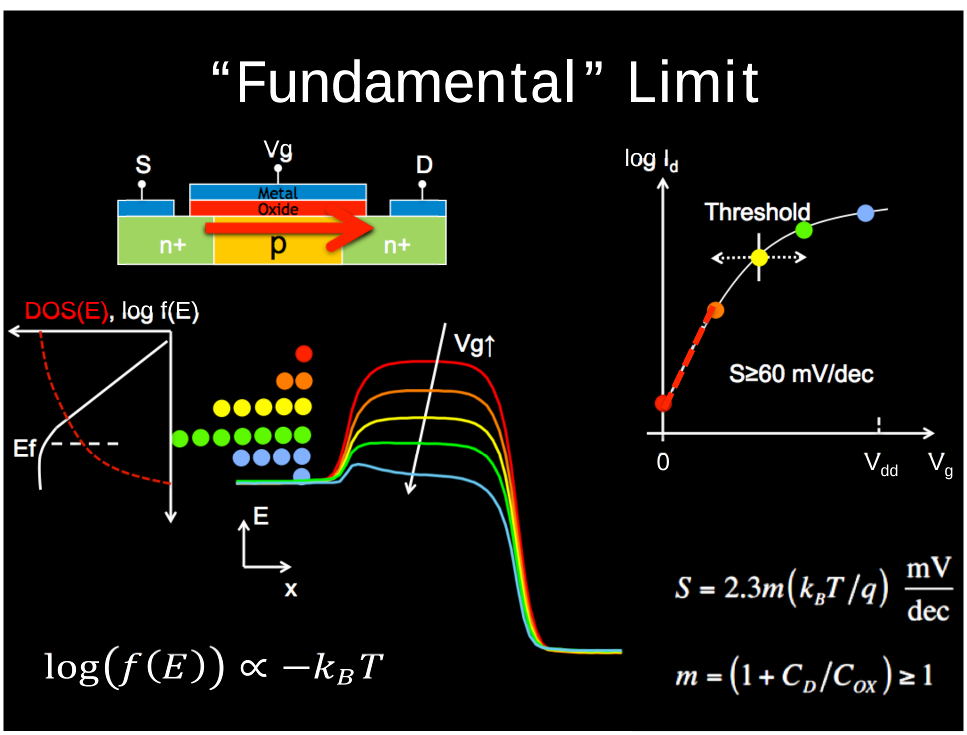
Static Power:

- Leakage through transistors

$$P \propto I_{OFF} \propto 1/\exp\,(V_{dd})$$ ☹



“Fundamental” Limit
Vg
S
D
Metal
Oxide
n+
p
n+
log I_d
Threshold
S≥60 mV/dec
0
V_{dd}
V_g
Vg↑
E
x



“Fundamental” Limit
Vg
S
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Metal
Oxide
n+
p
n+
log I_d
Threshold
S≥60 mV/dec
0
V_{dd}
V_g
DOS(E), log f(E)
Ef
Vg↑
E
x
$\log(f(E)) \propto -k_B T$
$S = 2.3m(k_B T/q)\ \frac{\text{mV}}{\text{dec}}$
$m = (1 + C_D/C_{ox}) \geq 1$

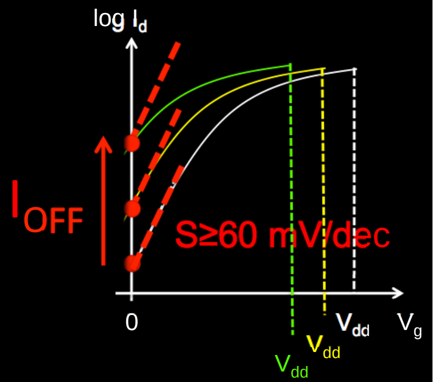
Device Scaling for Performance

Dynamic / Switching Power:

➢Charging a capacitor network

$$P \propto f \;\; C_L \, V_{dd}^2$$

➢ Reduce supply voltage

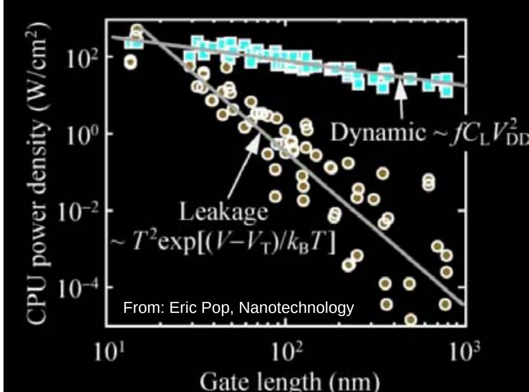


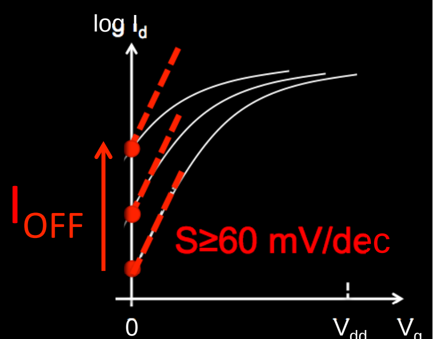
Static Power:

➢Leakage through transistors

$$P \propto I_{OFF} \propto 1/\exp\,(V_{DD})$$

Device Scaling for Performance





Static Power:

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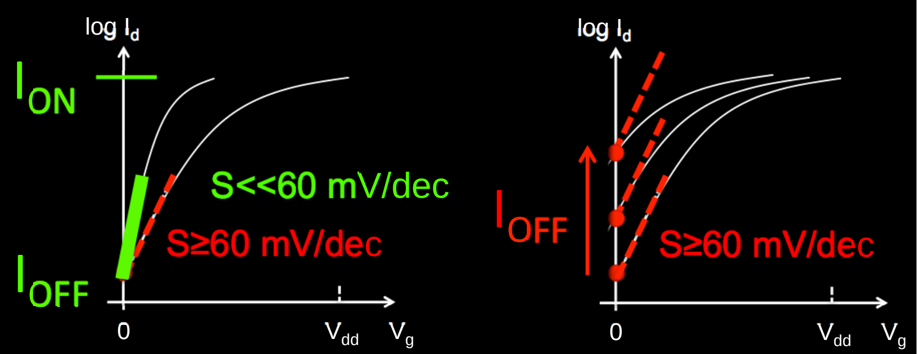
Device Scaling for Performance

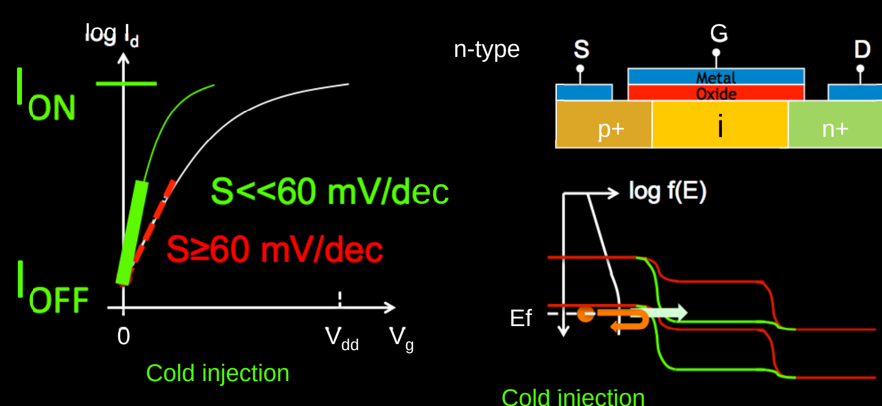


Static Power:

➢Leakage through transistors

$P \propto I_{OFF} \propto$ ~~$1/\exp(V_{DD})$~~

Need a Different Switch



Static Power:

➢Leakage through transistors

$P \propto I_{OFF} \propto$ ~~$1/\exp(V_{DD})$~~

The single-atom transistor

Presentation Outline

- Why?
  - A power problem
  - Near term solution
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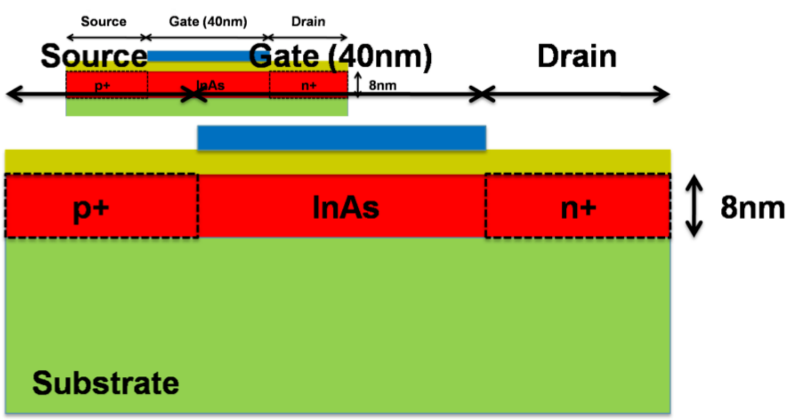
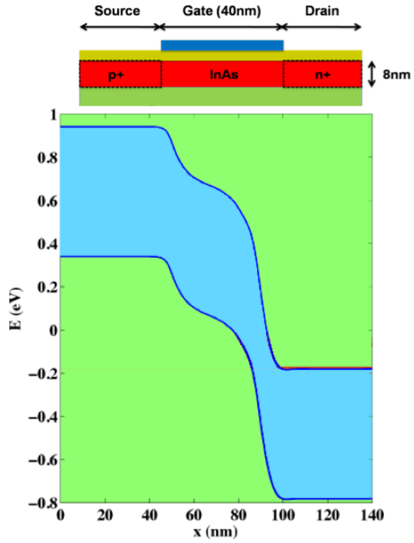
Ultra-Thin-Body (8nm) InAs BTBT Device



- Do not need phonons for direct current
- Highly non-parabolic conduction band
- Realistic valence band features

UTB Band Edges

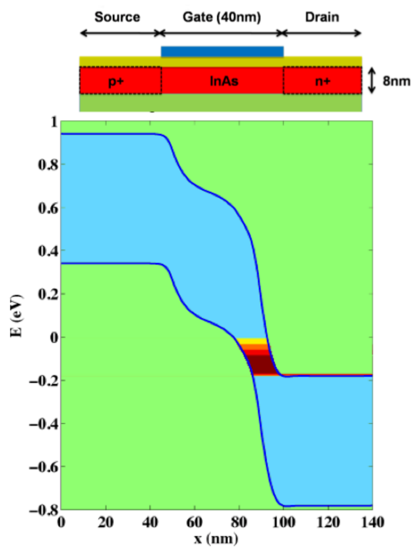


- 1D quantization
  => Bandgap raised from bulk
  0.37eV => ~0.6eV
- Realistic Poisson Solution
  Doping $1x10^{18}/cm^3$
- High doping regions flat bands
- Central gate region good control

- Doping $1x10^{18}/cm^3$

Gerhard Klimeck

UTB: Current Hotspots in Energy



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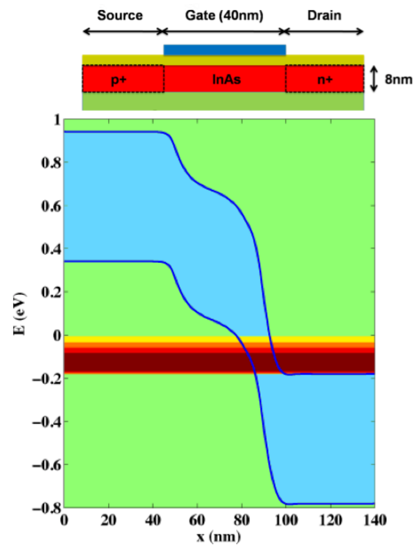
- Bandgap "narrow" at
  - Certain energies
  - Certain biases

Gerhard Klimeck

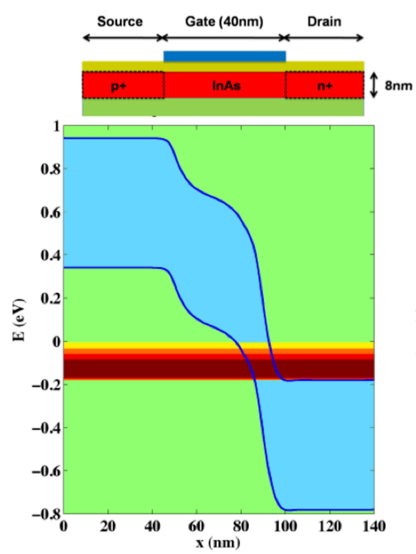
UTB Current Density in Energy



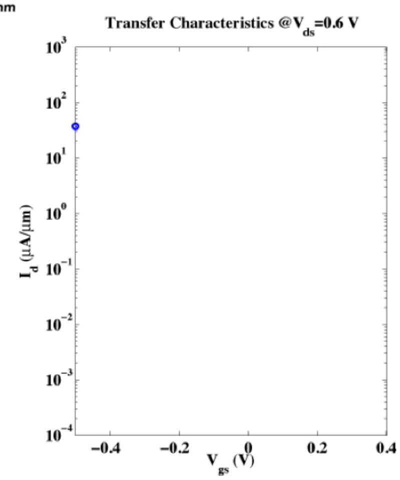
- 1D quantization
  => Bandgap raised from bulk
  0.37eV => ~0.6eV
- Realistic Poisson Solution
  Doping 1x10^{18}/cm^3
- High doping regions flat bands
- Central gate region good control
- Bandgap "narrow" at
  - » Certain energies
  - » Certain biases
- 2 energy regions of current flow
  - » Low Ec / high Ev
  - » High Ec / low Ev

PURDUE UNIVERSITY Gerhard Klimeck

UTB Current as a function of Gate Voltage



- Current vs. Gate Voltage



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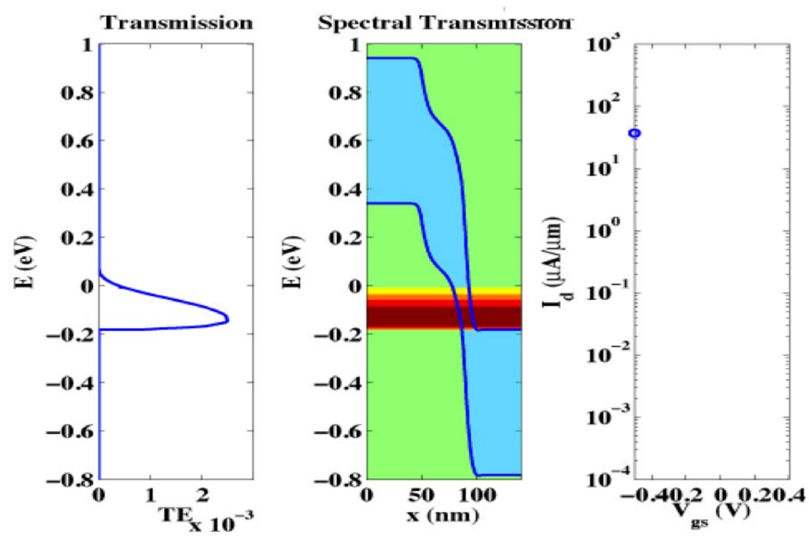
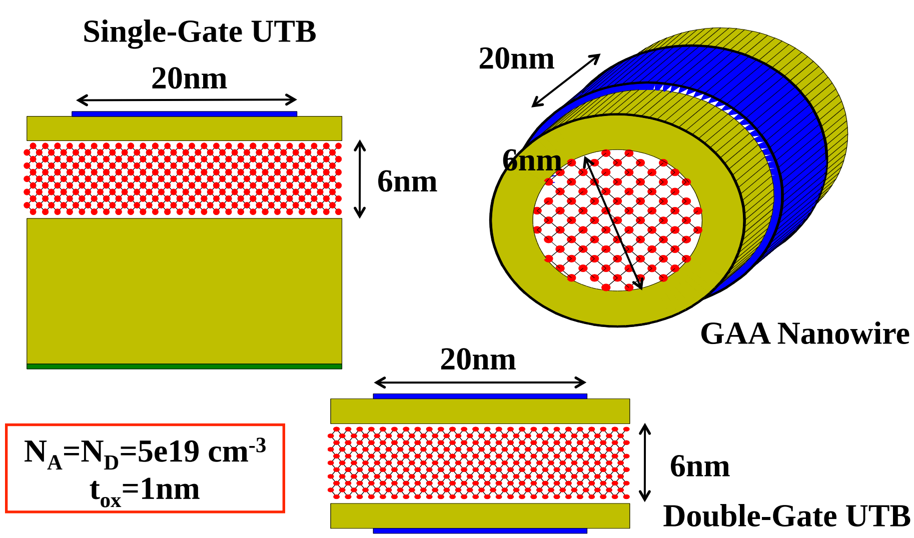
Strong Energy Dependence in T(E,k=0)



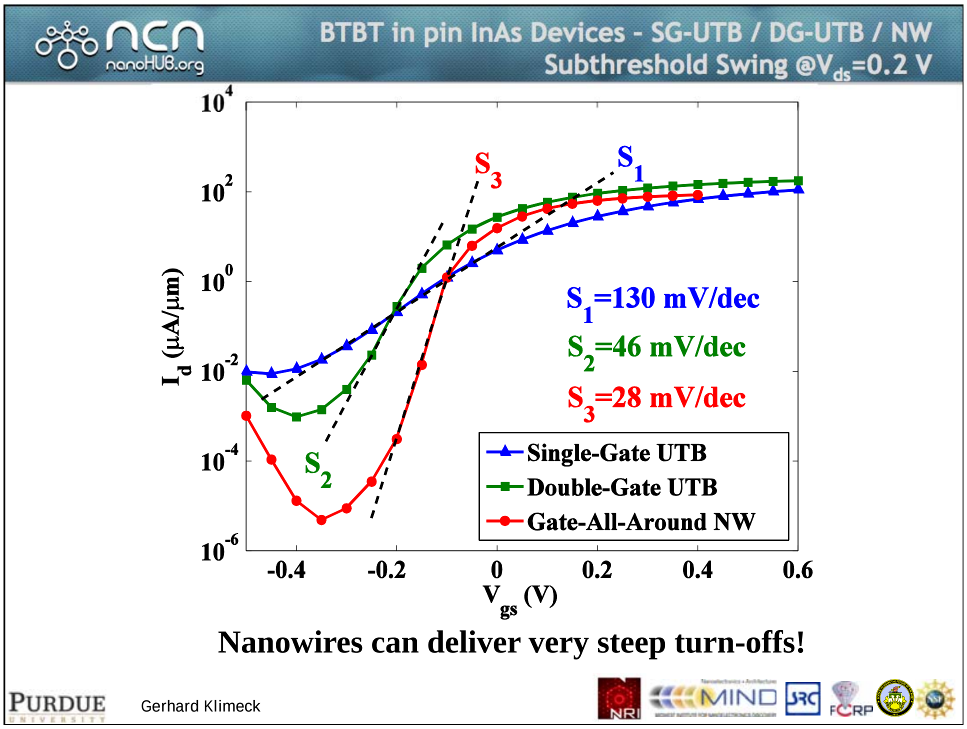
- Strong energy dependence in T(E,k=0)

Purdue Gerhard Klimeck

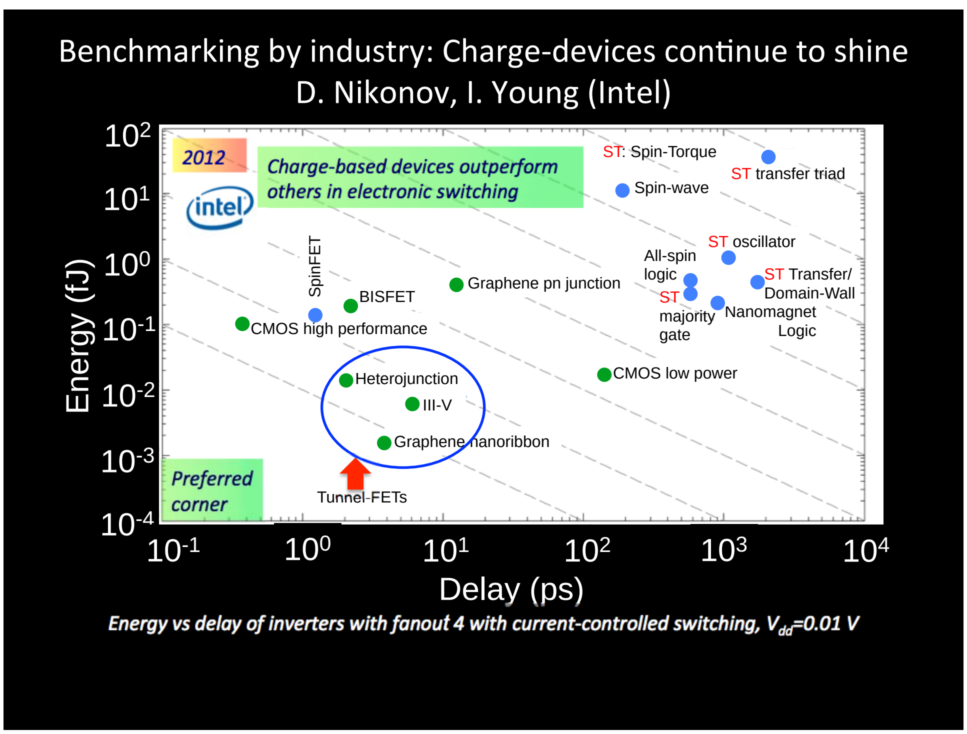
Application to pin InAs UTB and Nanowire



Purdue Gerhard Klimeck



BTBT in pin InAs Devices - SG-UTB / DG-UTB / NW
Subthreshold Swing @V_ds=0.2 V
nanoHUB.org
S1=130 mV/dec
S2=46 mV/dec
S3=28 mV/dec
Single-Gate UTB
Double-Gate UTB
Gate-All-Around NW
Id (μA/μm)
Vgs (V)
Nanowires can deliver very steep turn-offs!
PURDUE
Gerhard Klimeck



Benchmarking by industry: Charge-devices continue to shine
D. Nikonov, I. Young (Intel)
2012
Charge-based devices outperform others in electronic switching
ST: Spin-Torque
Spin-wave
ST transfer triad
ST oscillator
All-spin logic
ST majority gate
ST Transfer/ Domain-Wall
Nanomagnet Logic
SpinFET
BISFET
Graphene pn junction
CMOS high performance
CMOS low power
Heterojunction
III-V
Graphene nanoribbon
Tunnel-FETs
Preferred corner
Energy (fJ)
Delay (ps)
Energy vs delay of inverters with fanout 4 with current-controlled switching, V_dd=0.01 V

Power Problem:
Tunneling Transistors
to the Rescue!

For a little while!

The single-atom transistor

Presentation Outline

- Why?
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  - Continuum => finite atoms
- What is it?
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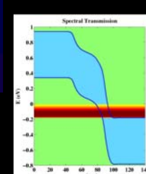
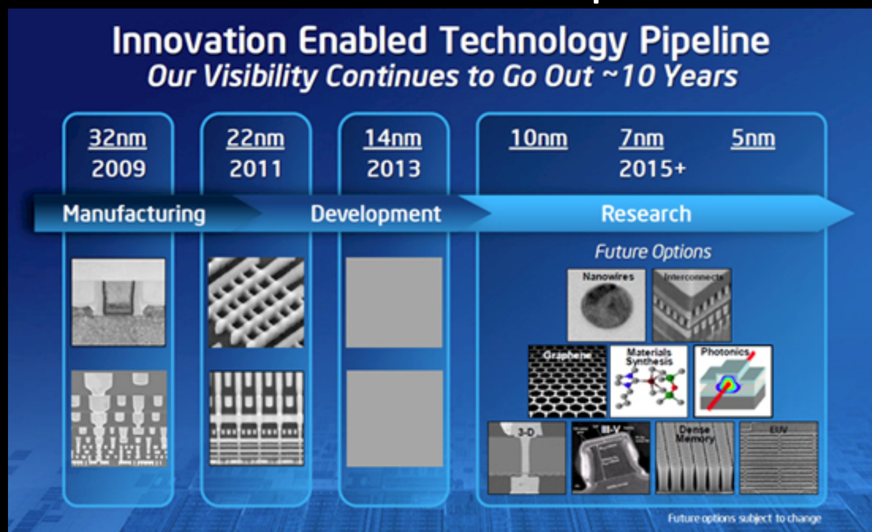
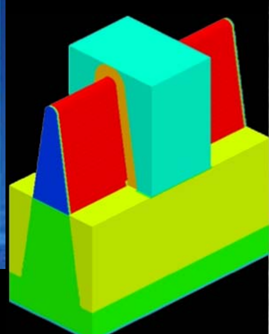


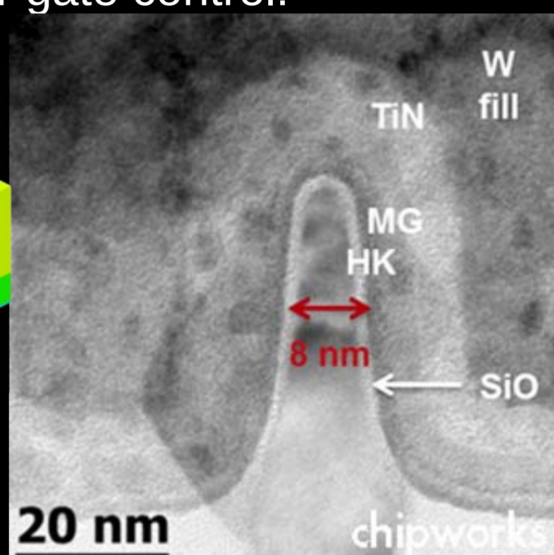
Intel Roadmap



Today: non-planar 3D devices
Better gate control!



Intel 22nm finFET



http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

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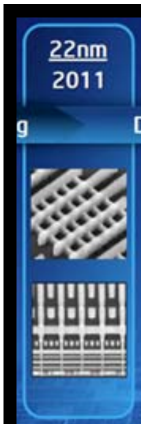

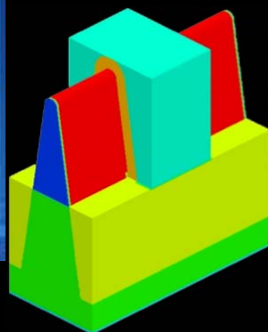

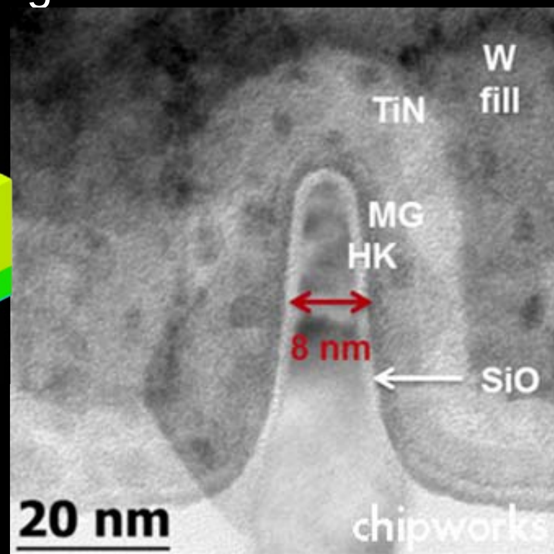

22nm = 176 atoms

8nm = 64 atoms

http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

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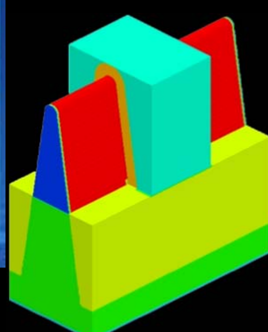
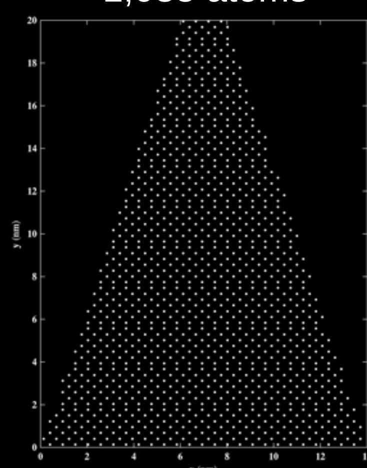


1,085 atoms



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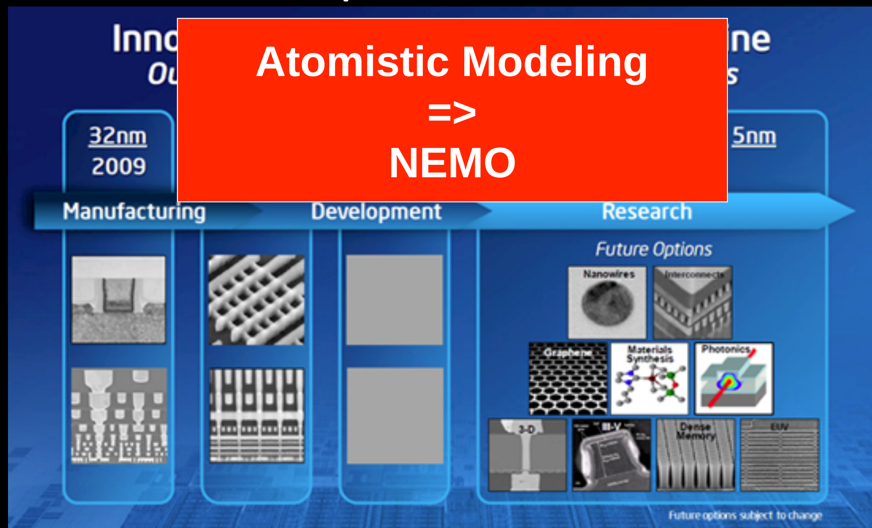
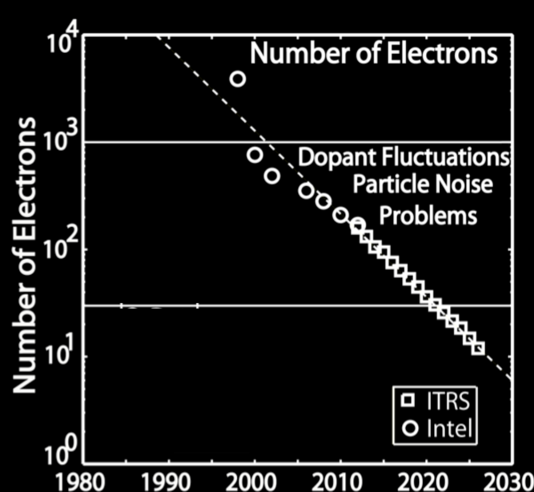
http://www.goldstandardsimulations.com/index.php/news/blog_search/simulation-analysis-of-the-intel-22nm-finfet/
http://www.chipworks.com/media/wpmu/uploads/blogs.dir/2/files/2012/08/Intel22nmPMOSfin.jpg

Roadmap of finite atoms!



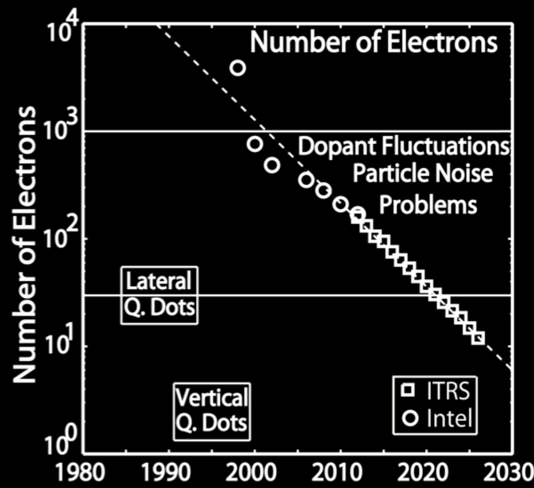
nm Node	22	14	10	7	5
Node atoms	176	122	80	56	40
Critical atoms	64	44(?)	29(?)	20(?)	14(?)
Electrons	160-190	64-80	30-38	18-23	11-15

Roadmap of finite electrons!



nm Node	22	14	10	7	5
Node atoms	176	122	80	56	40
Critical atoms	64	44(?)	29(?)	20(?)	14(?)
Electrons	160-190	64-80	30-38	18-23	11-15

Quantum Dot Research



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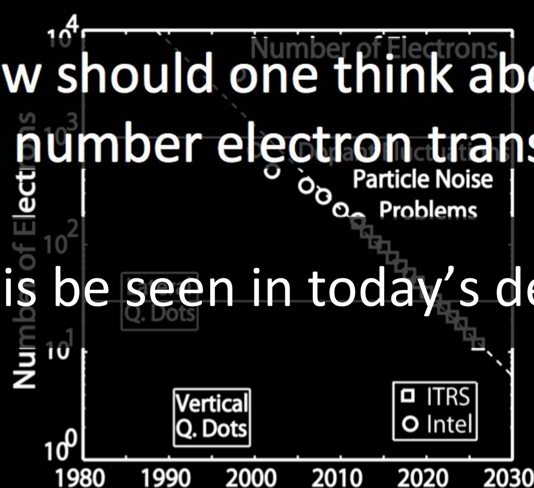
Roadmap of finite electrons!

How should one think about finite number electron transport?

Can this be seen in today's devices?



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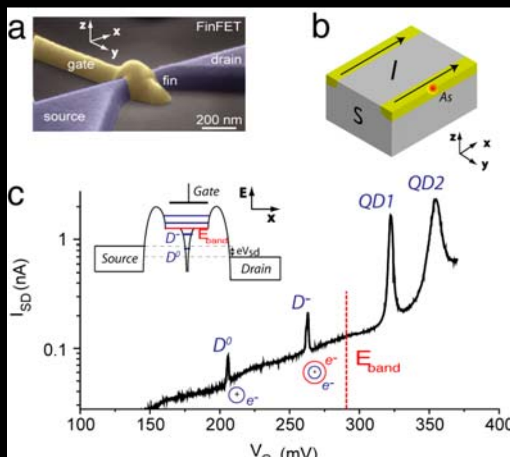
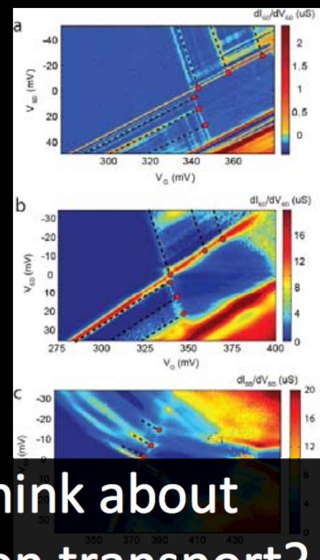
FinFETs with finite electrons



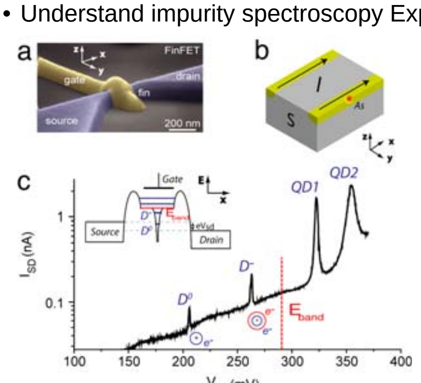


How should one think about finite number electron transport?

- IMEC ... Nature Physics (2008)
- Each device has a specific fingerprint => Metrology of As vs P impurities

Metrology with multimillion atom simulations Excited States are Critical!

- Understand impurity spectroscopy Expt.



Questions:

- How deep are the impurities?
- Are the impurities "As" or "P" ?

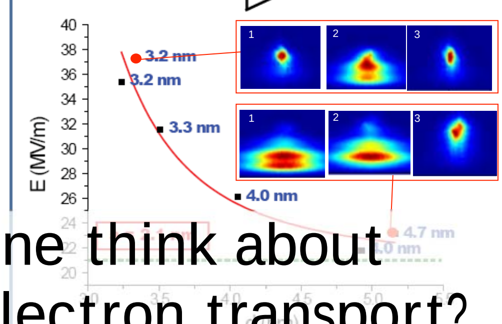
Results / Impact:

- Understand state hybridization
- Understand depth and identify "As"

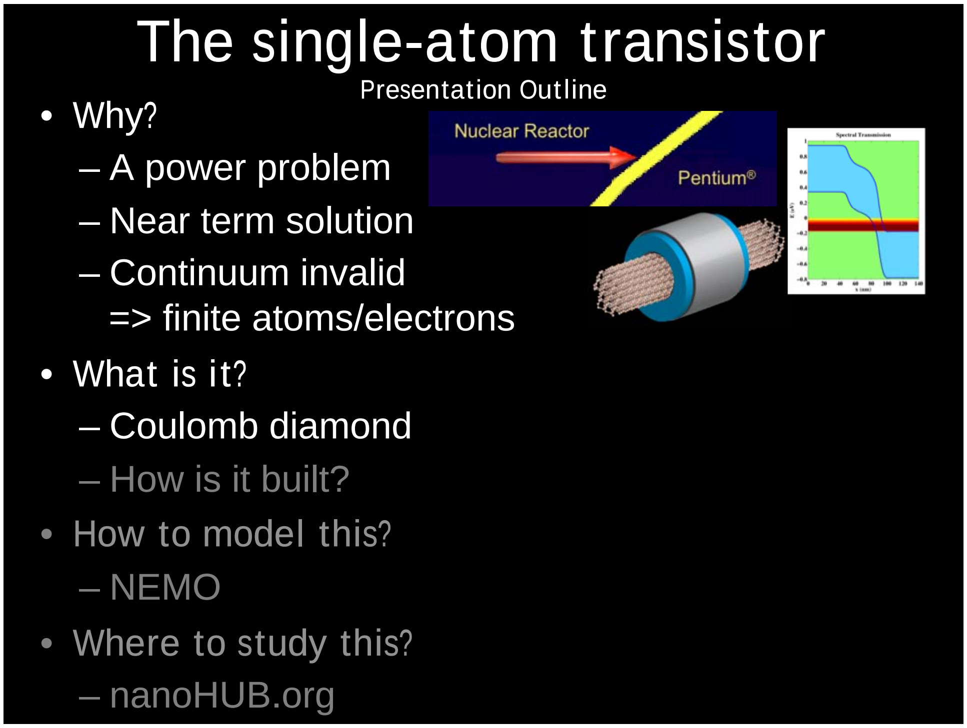
Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET

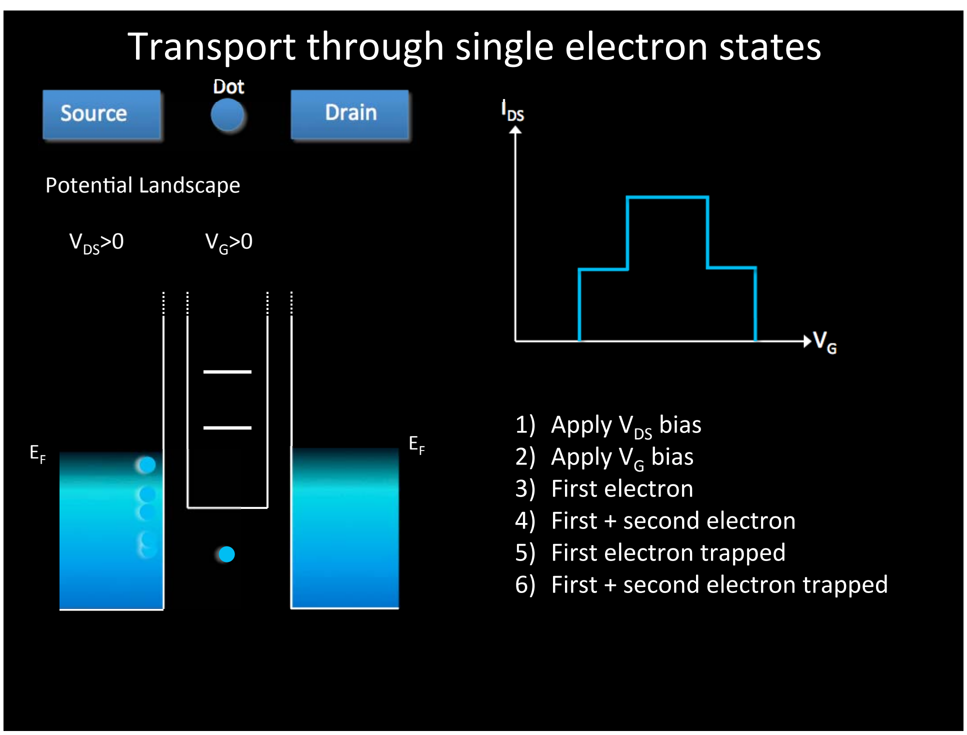
G. P. LANSBERGEN[1]*, R. RAHMAN[2], C. J. WELLARD[3], I. WOO[2], J. CARO[1], N. COLLAERT[4], S. BIESEMANS[4], G. KLIMECK[2,5], L. C. L. HOLLENBERG[3] AND S. ROGGE[1]

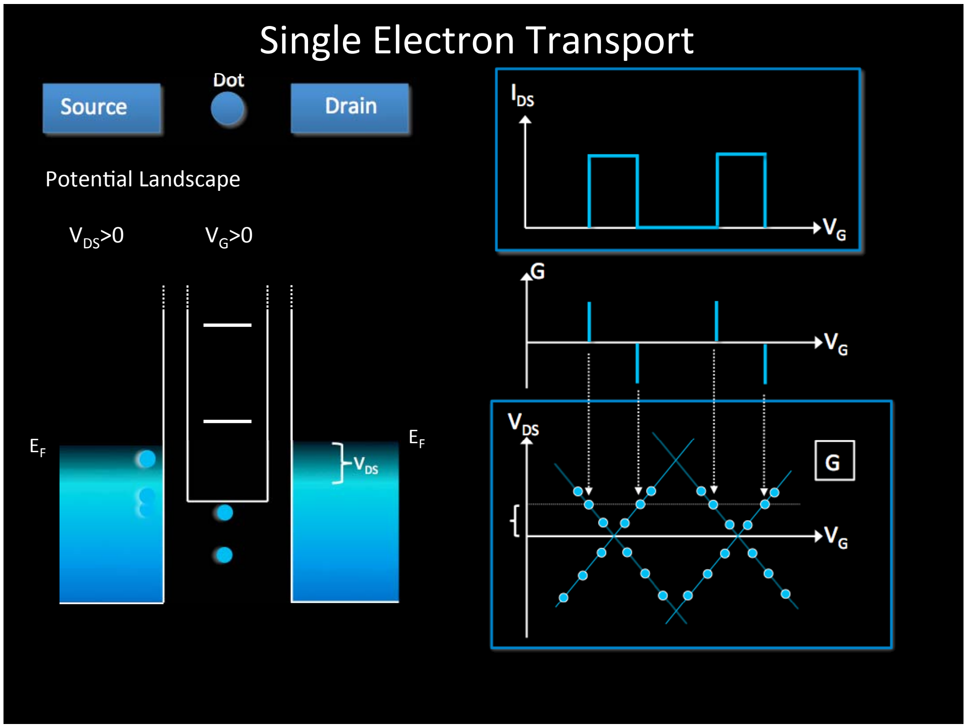
nature physics

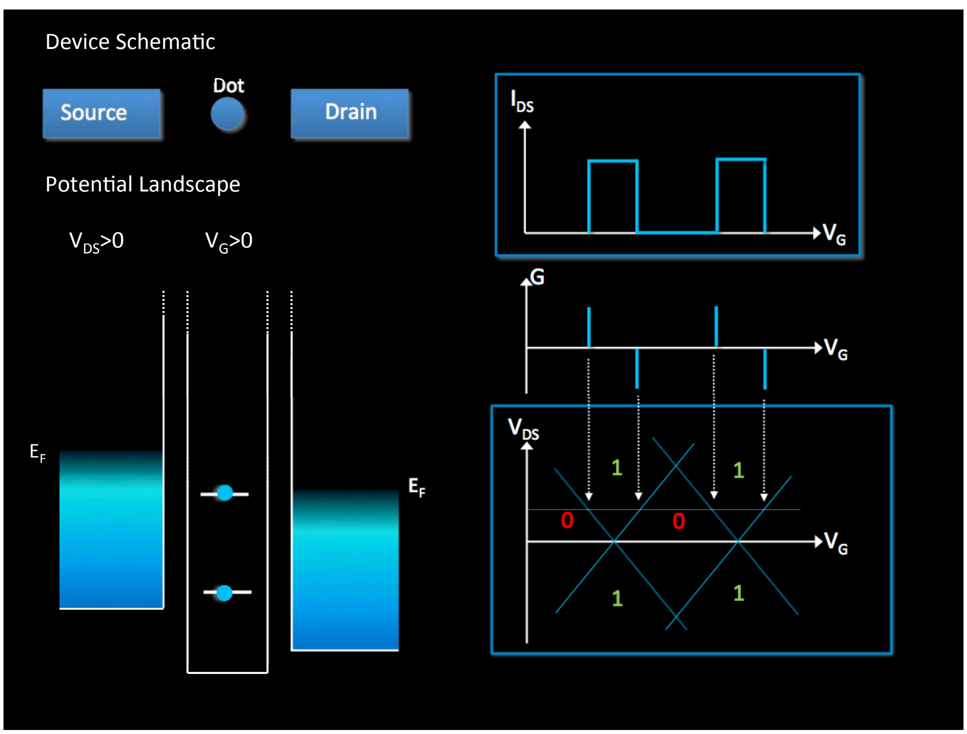


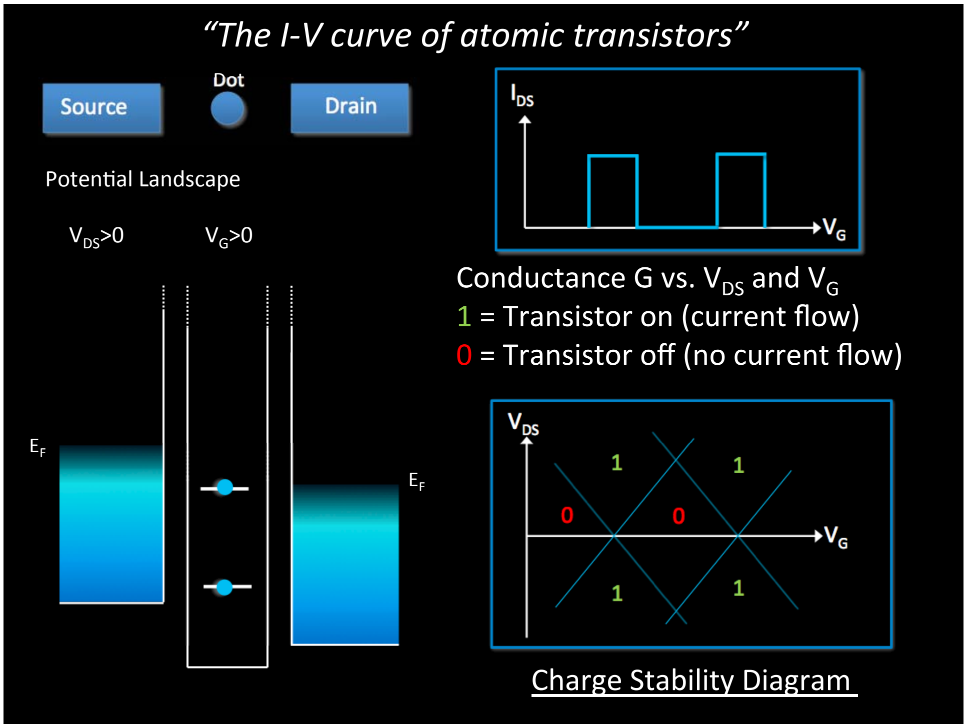
How should one think about finite number electron transport?

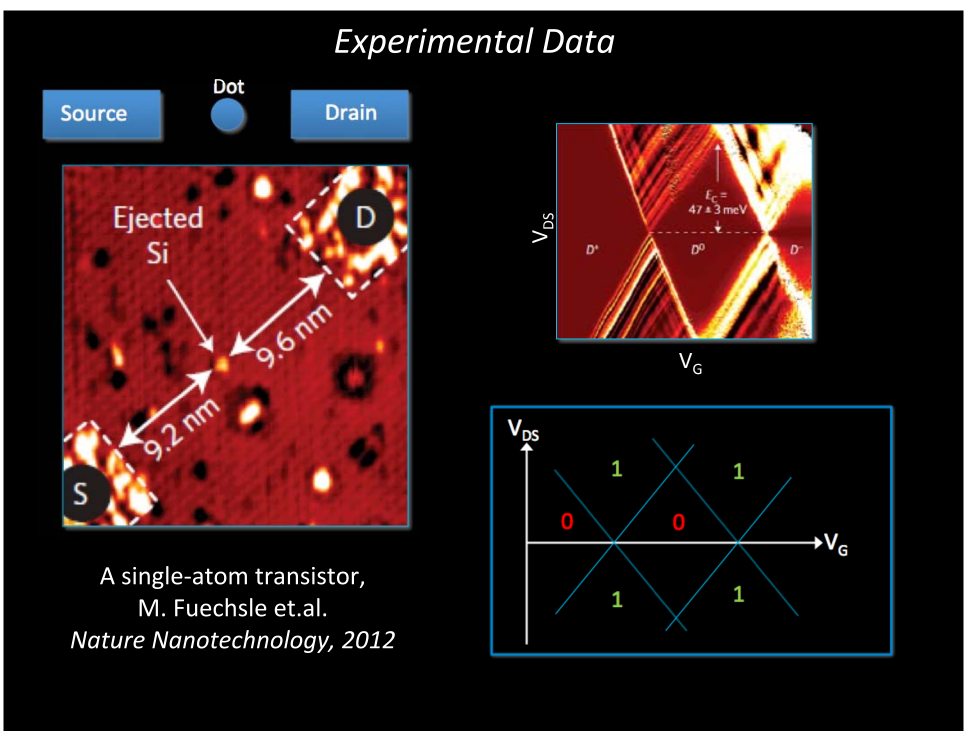

The single-atom transistor
Presentation Outline
• Why?
– A power problem
– Near term solution
– Continuum invalid
=> finite atoms/electrons
• What is it?
– Coulomb diamond
– How is it built?
• How to model this?
– NEMO
• Where to study this?
– nanoHUB.org
Nuclear Reactor
Pentium®

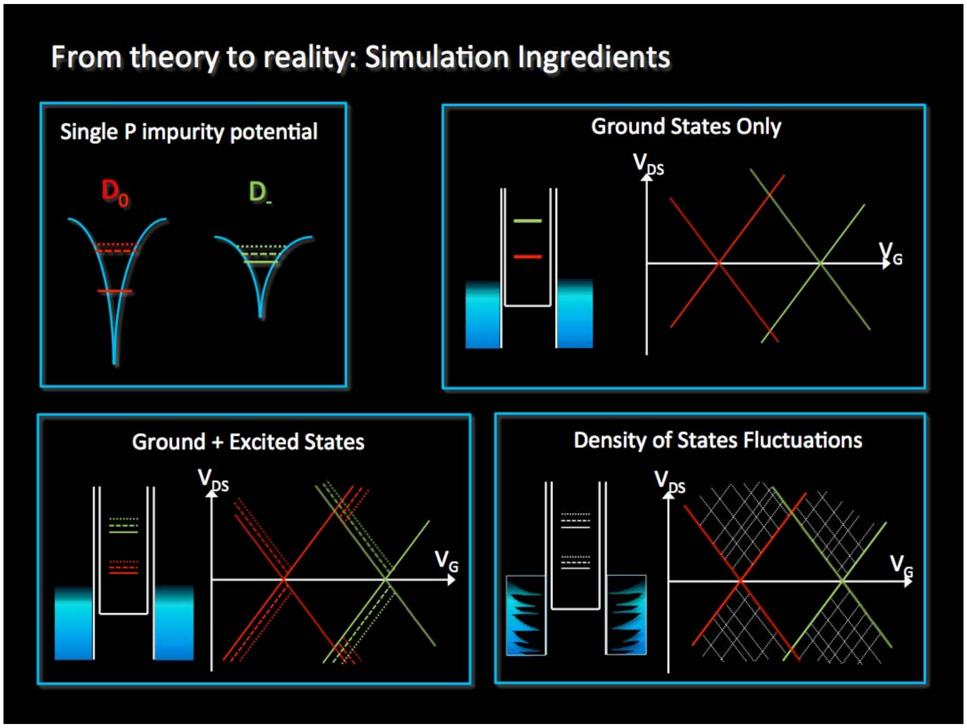

Transport through single electron states
Source
Dot
Drain
Potential Landscape
V_{DS}>0
V_G>0
E_F
E_F
I_{DS}
V_G
1) Apply V_{DS} bias
2) Apply V_G bias
3) First electron
4) First + second electron
5) First electron trapped
6) First + second electron trapped

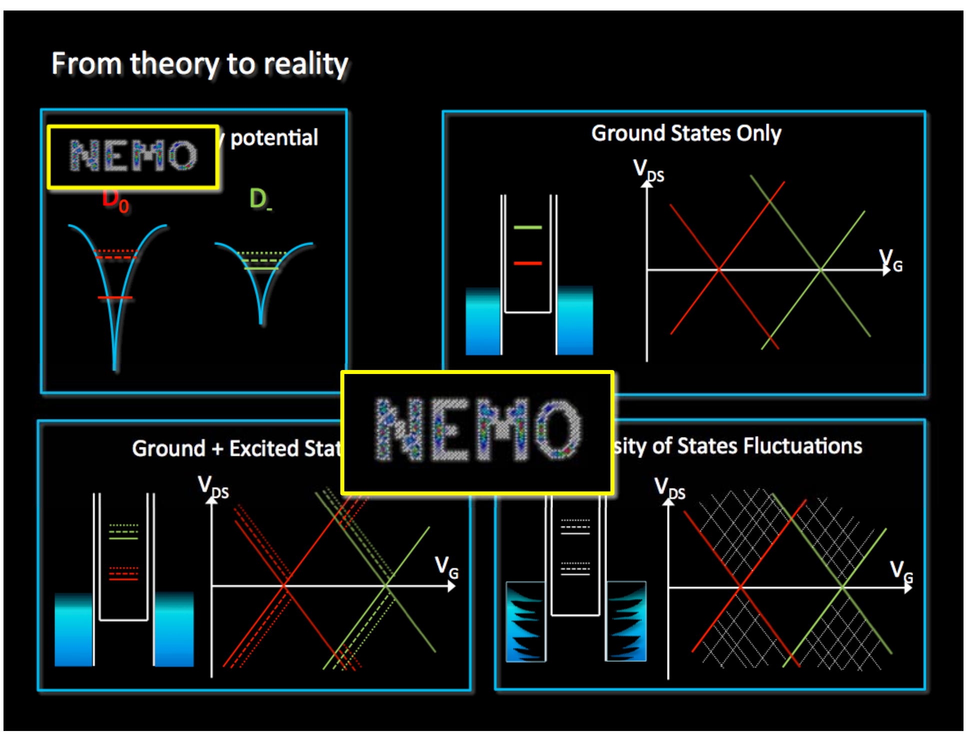

Single Electron Transport
Source
Dot
Drain
Potential Landscape
VDS>0
VG>0
EF
EF
VDS
IDS
VG
G
VG
VDS
G
VG

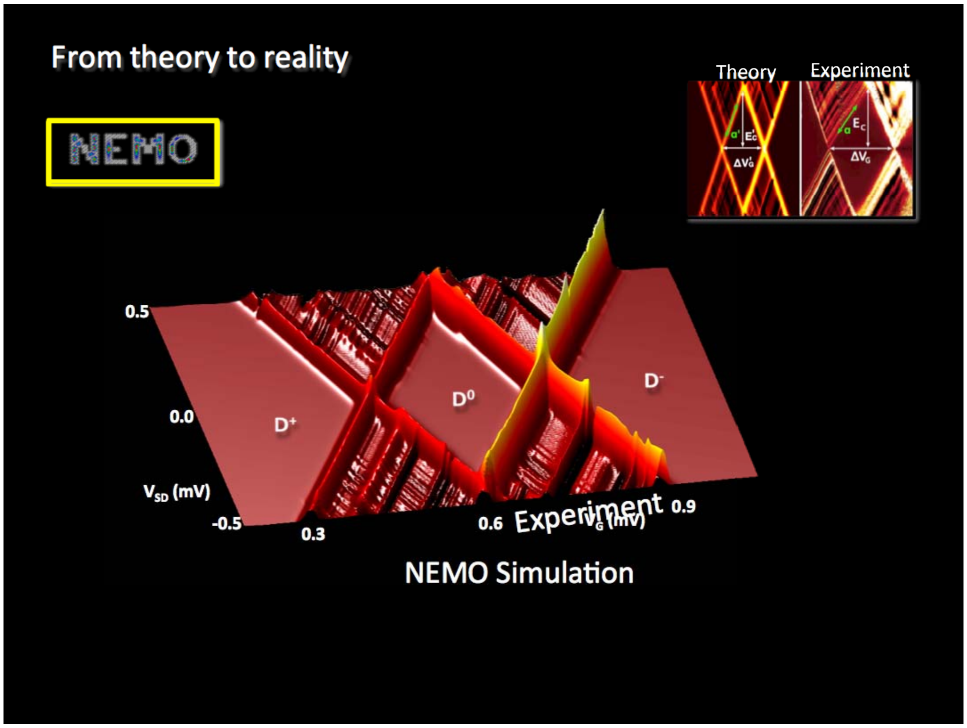

Device Schematic
Source
Dot
Drain
Potential Landscape
VDS>0
VG>0
EF
EF
IDS
VG
G
VG
VDS
1
1
0
0
VG
1
1

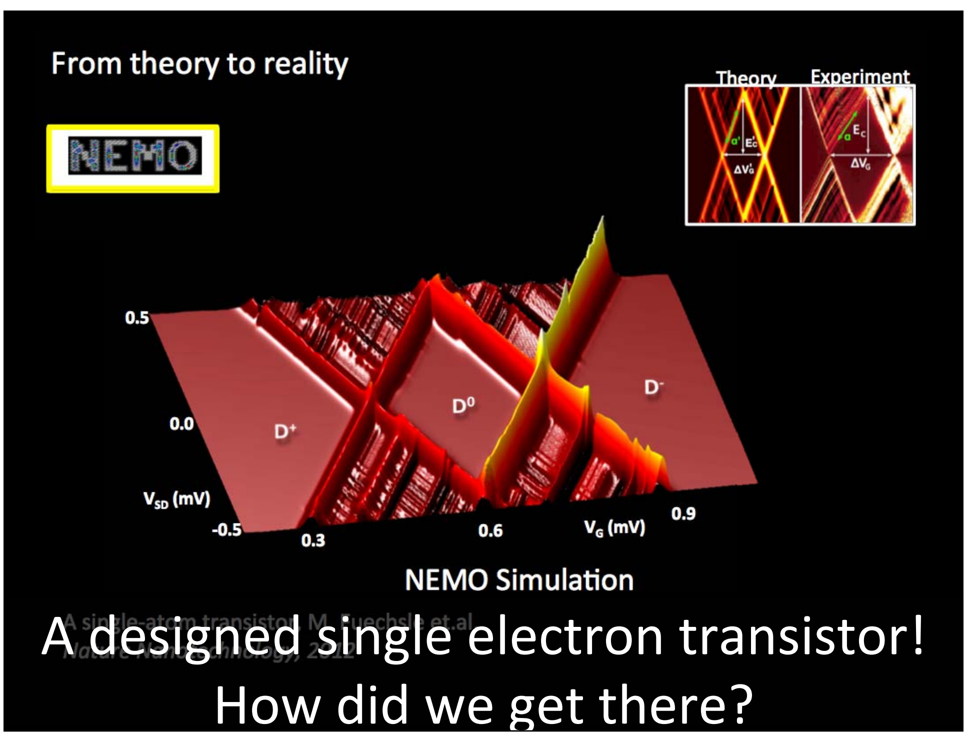

"The I-V curve of atomic transistors"
Source
Dot
Drain
Potential Landscape
V_{DS}>0
V_G>0
E_F
E_F
I_{DS}
V_G
Conductance G vs. V_{DS} and V_G
1 = Transistor on (current flow)
0 = Transistor off (no current flow)
V_{DS}
1
1
0
0
V_G
1
1
Charge Stability Diagram


Experimental Data
Source
Dot
Drain
Ejected
Si
D
9.6 nm
9.2 nm
S
V_{DS}
V_G
V_{DS}
1
1
0
0
V_G
1
1
A single-atom transistor,
M. Fuechsle et.al.
Nature Nanotechnology, 2012


From theory to reality: Simulation Ingredients
Single P impurity potential
D0
D-
Ground States Only
VDS
VG
Ground + Excited States
VDS
VG
Density of States Fluctuations
VDS
VG


From theory to reality
NEMO
potential
D0
D-
Ground States Only
VDS
VG
NEMO
Ground + Excited Stat
VDS
VG
sity of States Fluctuations
VDS
VG


From theory to reality
NEMO
Theory
Experiment
0.5
0.0
V_{SD} (mV)
-0.5
0.3
0.6
0.9
D^+
D^0
D^-
Experiment
V_G (mV)
NEMO Simulation


From theory to reality
NEMO
Theory
Experiment
0.5
0.0
V_{SD} (mV)
-0.5
0.3
0.6
V_G (mV)
0.9
D^+
D^0
D^-
NEMO Simulation
A designed single electron transistor!
How did we get there?

The single-atom transistor

Presentation Outline

- Why?
  - A power problem
  - Near term solution
  - Continuum invalid
    => finite atoms/electrons
- What is it?
  - Coulomb diamond
  - How is it built?
- How to model this?
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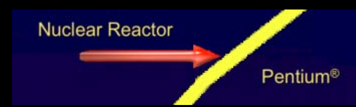
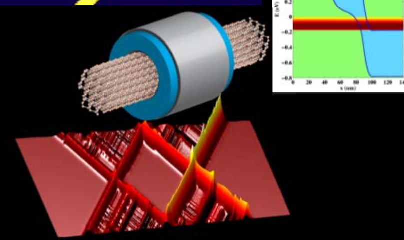




CENTRE FOR
QUANTUM COMPUTATION &
COMMUNICATION TECHNOLOGY
AUSTRALIAN RESEARCH COUNCIL CENTRE OF EXCELLENCE

A designed single electron transistor!
How did we get there?

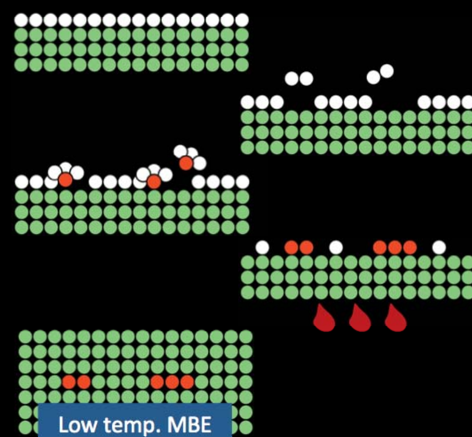
Experimental Efforts: STM Lithography

Objectives
- Precise donor placement
- Place "many" donors in ultra-scaled region

Scanning Tunneling Microscopy
- Device surface imaging
- Control/pattern at atomic scales

  Eagler et al, Nature (1990)
- Densely P δ-doped Si (Si:P) device
  - Doping control ~ 5×10^{-10}(m)
  - Up to 1/2.9ML (1 P atom per every 2.9 Si atoms)

Fabricating single ML thick P doped planes using STM lithography

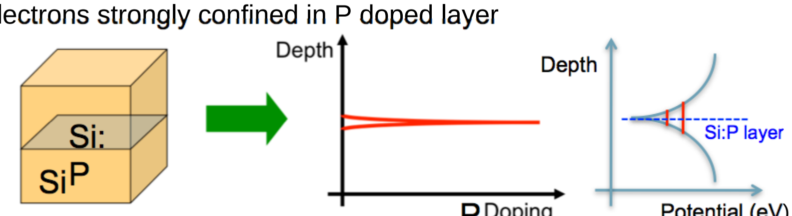


Ruess et al., Nano Lett. (2004)

Picture edited

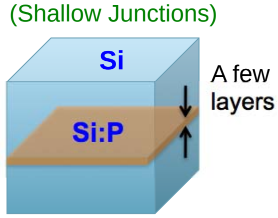
Si:P System

- **Densely Phosphorus δ-doped Si (Si:P) device**
  - » Thin densely P doped layer in low-doped/intrinsic Si bulk
  - » Electrons strongly confined in P doped layer

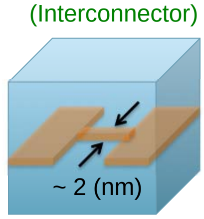


- **Prototype: Novel Structures/ Nanoscale Devices**

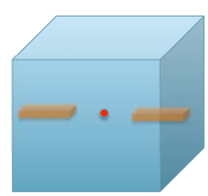
2-D electron reservoirs (Shallow Junctions)



Ultra-narrow NW channel (Interconnector)



Single donor device with NW leads



Collaboration with UNSW: Experimental Devices

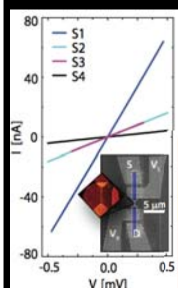
NETWORK FOR COMPUTATIONAL NANOTECHNOLOGY

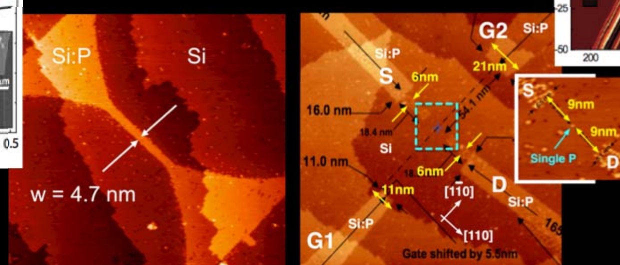
CENTRE FOR QUANTUM COMPUTATION & COMMUNICATION TECHNOLOGY
AUSTRALIAN RESEARCH COUNCIL CENTRE OF EXCELLENCE

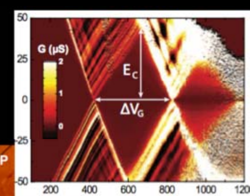
Modeling

Experiment, Theory

Si:P Systems



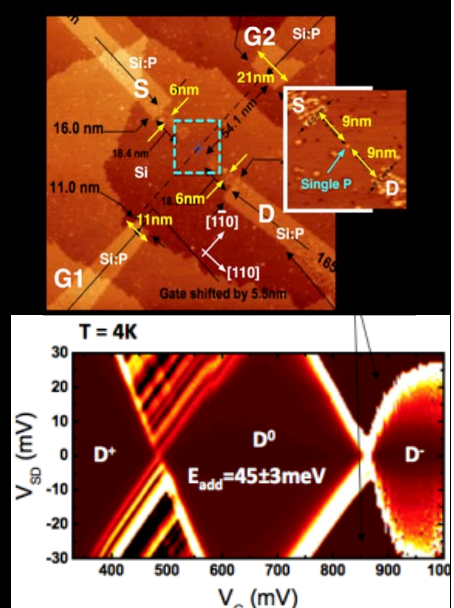




Questions, questions, questions

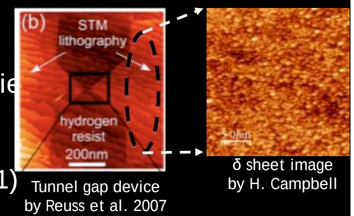
Single impurity device?

- Explain the coupling of the channel donor to the Si:P leads
- "quantify" the controllability of planar Si:P leads on the channel confinement
- Why does the Coulomb diamond extend into the D- regime?
- Why are there the conductance streaks at the Coulomb diamond edges?



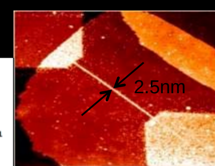
Answers…. Some…

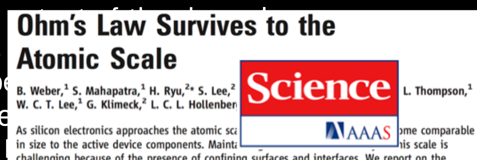
- 2d layers – quantum well
  - Detailed bandstructure
  - Validate methodology against other theorie
  - Overall potential landscape
  - Robustness against disorder
  - S. Lee et al, Phys. Rev. B 84, 205309 (2011)
- Si:P Nanowires
  - Ohmic conduction
  - Spatial
  - Details
  - B. Webe
- Si:P Single
  - D^0 and
  - Validate single impurity
  - M. Fuechsle et al,



Tunnel gap device by Reuss et al. 2007

δ sheet image by H. Campbell

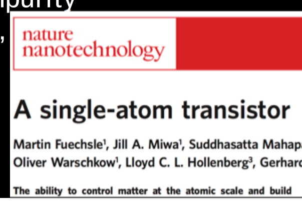




Ohm's Law Survives to the Atomic Scale

B. Weber,[1] S. Mahapatra,[1] H. Ryu,[2*] S. Lee,[2] … L. Thompson,[1] W. C. T. Lee,[1] G. Klimeck,[2] L. C. L. Hollenber…

As silicon electronics approaches the atomic sc… …me comparable in size to the active device components. Maint… …his scale is challenging because of the presence of confining surfaces and interfaces. We report on the

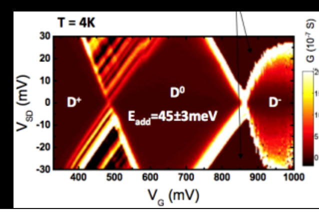


nature nanotechnology

A single-atom transistor

Martin Fuechsle[1], Jill A. Miwa[1], Suddhasatta Mahapa… Oliver Warschkow[1], Lloyd C. L. Hollenberg[3], Gerhard…

The ability to control matter at the atomic scale and build



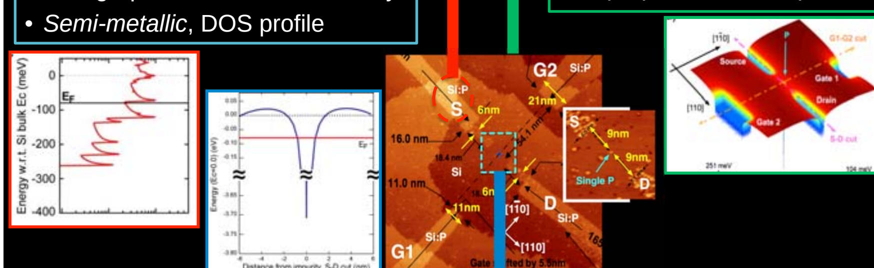
A multi-scale modeling procedure

1. Contact modeling

- Atomistic modeling on the leads
- Charge-potential self-consistency
- *Semi-metallic*, DOS profile

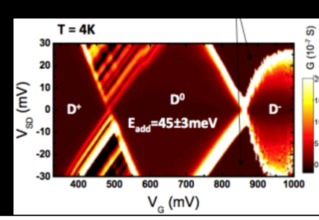
2. Potential profile

- Semi-classical potential profile
- Superpose w. donor potential



3. Charge filling

- Potential profile → Hamiltonian
- Compute eigenstates w.r.t E_F at every V_G
- Transition, charging energy and gate modulation



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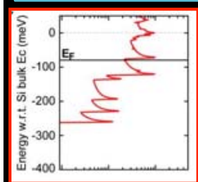

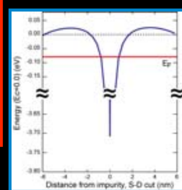

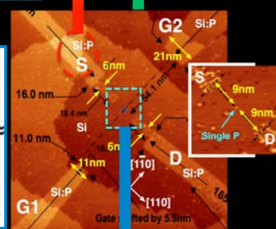

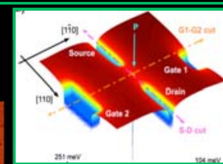

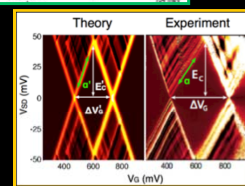

3. Charge filling
- Potential profile → Hamiltonian
- Compute eigenstates w.r.t E_F at every V_G
- Transition, charging energy and gate modulation

4. Coulomb diamond
- DOS profile of S/D and Charge filling information
- Rate equation formalism

The single-atom transistor

Presentation Outline

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  - Near term solution
  - Continuum invalid
    => finite atoms/electrons
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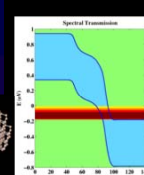
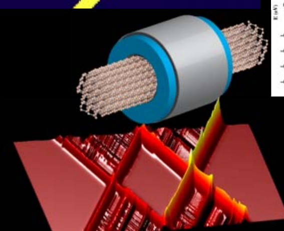
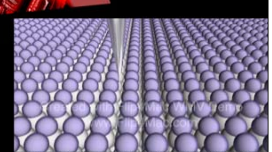
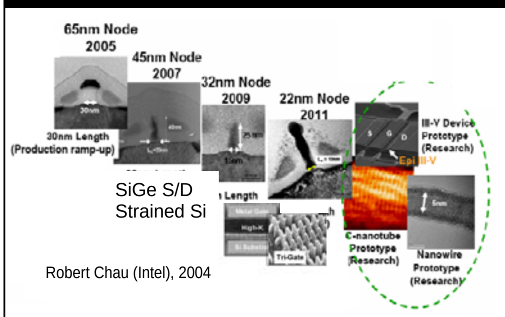




NEMO



Industrial Device Trends and Challenges



Observations:

- 3D spatial variations on nm scale
- Potential variations on nm scale
- New channel materials (Ge, III-V)

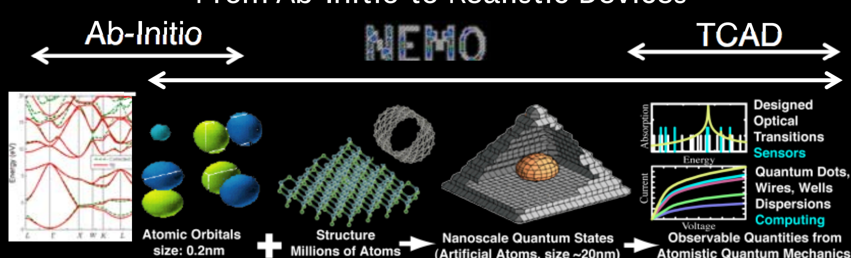
Questions / Challenges

- Strain ?
- Quantization?
- Crystal orientation?
- Atoms are countable; does granularity matter? Disorder?
- New material or new device?

Assertions of importance

- High bias / non-equilibrium
- Quantum mechanics
- Atomistic representation
  - Band coupling, non-parabolicity, valley splitting
  - Local (dis)order, strain and orientation

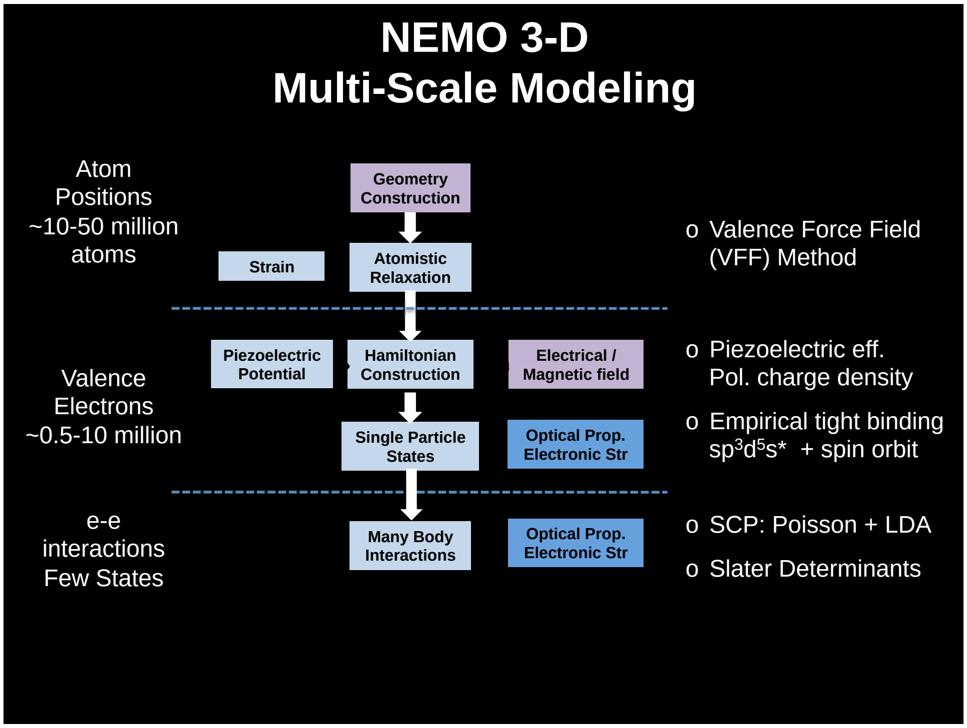
NEMO5 - Bridging the Scales
From Ab-Initio to Realistic Devices

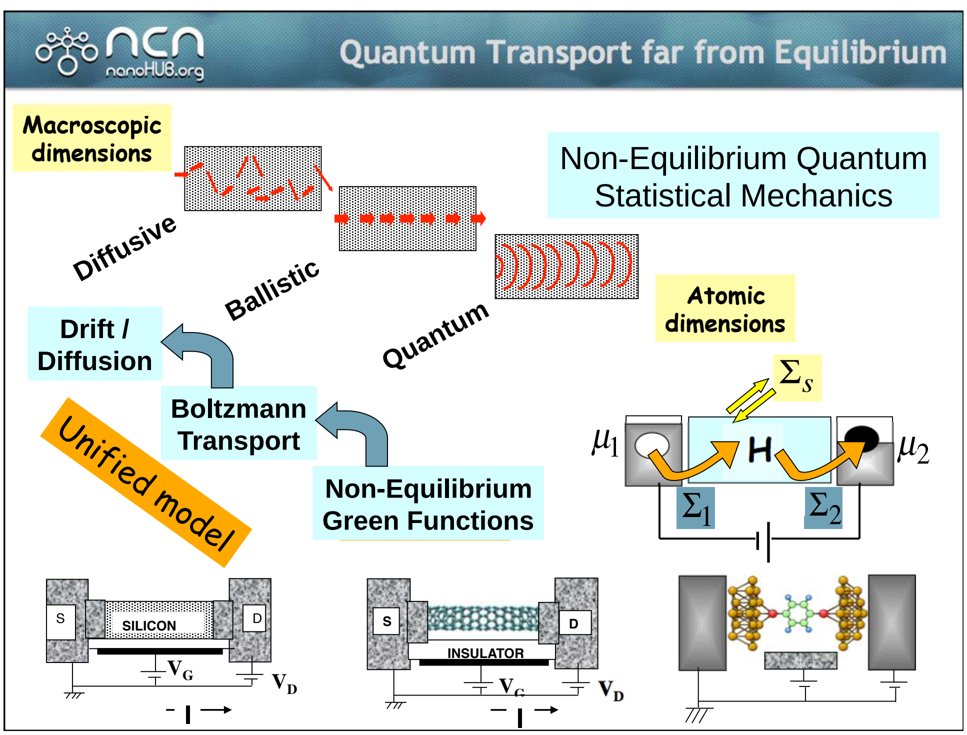


Goal:
- Device performance with realistic extent, heterostructures, fields, etc. for new / unknown materials

Problems:
- Need ab-initio to explore new material properties
- Ab-initio cannot model non-equilibrium.
- TCAD does not contain any real material physics

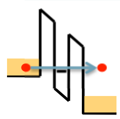
Approach:
- Ab-initio:
  - Bulk constituents
  - Small ideal superlattices
- Map ab-initio to tight binding (binaries and superlattices)
- Current flow in ideal structures
- Study devices perturbed by:
  - Large applied biases
  - Disorder
  - Phonons


NEMO 3-D
Multi-Scale Modeling
Atom Positions ~10-50 million atoms
Geometry Construction
Strain
Atomistic Relaxation
o Valence Force Field (VFF) Method
Valence Electrons ~0.5-10 million
Piezoelectric Potential
Hamiltonian Construction
Electrical / Magnetic field
o Piezoelectric eff. Pol. charge density
Single Particle States
Optical Prop. Electronic Str
o Empirical tight binding $sp^3d^5s^*$ + spin orbit
e-e interactions Few States
Many Body Interactions
Optical Prop. Electronic Str
o SCP: Poisson + LDA
o Slater Determinants


ncn nanoHUB.org
Quantum Transport far from Equilibrium
Macroscopic dimensions
Non-Equilibrium Quantum Statistical Mechanics
Diffusive
Ballistic
Quantum
Atomic dimensions
Drift / Diffusion
Boltzmann Transport
Non-Equilibrium Green Functions
Unified model
Σ_s
μ_1
H
μ_2
Σ_1
Σ_2
S
SILICON
D
V_G
V_D
I
S
INSULATOR
D
V_G
V_D
I

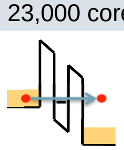
A Journey Through Nanoelectronics Tools NEMO and OMEN

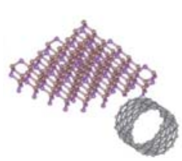
	NEMO-1D
Transport	Yes
Dim.	1D
Atoms	~1,000
Crystal	[100] Cubic, ZB
Strain	-
Multi-physics	-
Parallel Comp.	3 levels 23,000 cores



A Journey Through Nanoelectronics Tools NEMO and OMEN

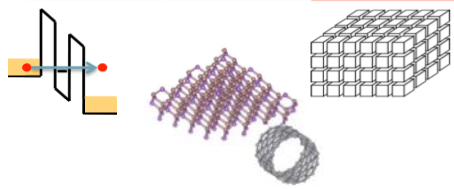
	NEMO-1D	NEMO-3D
Transport	Yes	-
Dim.	1D	any
Atoms	~1,000	50 Million
Crystal	[100] Cubic, ZB	[100] Cubic, ZB
Strain	-	VFF
Multi-physics	-	
Parallel Comp.	3 levels 23,000 cores	1 level 80 cores





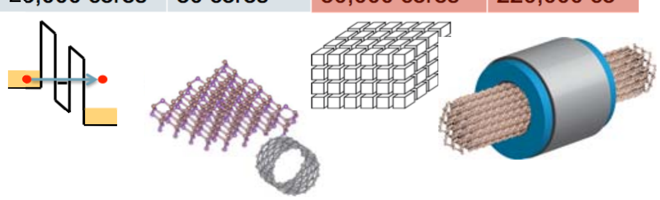
A Journey Through Nanoelectronics Tools NEMO and OMEN

	NEMO-1D	NEMO-3D	NEMO3Dpeta
Transport	Yes	-	-
Dim.	1D	any	any
Atoms	~1,000	50 Million	100 Million
Crystal	[100] Cubic, ZB	[100] Cubic, ZB	[100], Cubic,ZB, WU
Strain	-	VFF	VFF
Multi-physics	-		
Parallel Comp.	3 levels 23,000 cores	1 level 80 cores	3 levels 30,000 cores



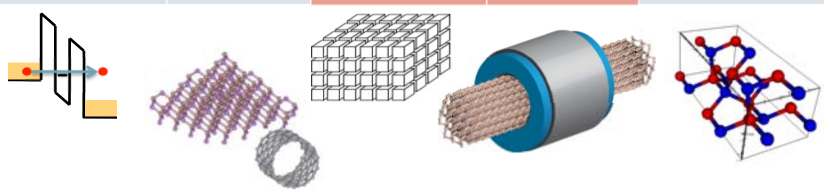
A Journey Through Nanoelectronics Tools NEMO and OMEN

	NEMO-1D	NEMO-3D	NEMO3Dpeta	OMEN
Transport	Yes	-	-	Yes
Dim.	1D	any	any	any
Atoms	~1,000	50 Million	100 Million	~140,000
Crystal	[100] Cubic, ZB	[100] Cubic, ZB	[100], Cubic,ZB, WU	Any Any
Strain	-	VFF	VFF	-
Multi-physics	-			
Parallel Comp.	3 levels 23,000 cores	1 level 80 cores	3 levels 30,000 cores	4 levels 220,000 co



A Journey Through Nanoelectronics Tools NEMO and OMEN

	NEMO-1D	NEMO-3D	NEMO3Dpeta	OMEN	NEMO5
Transport	Yes	-	-	Yes	Yes
Dim.	1D	any	any	any	any
Atoms	~1,000	50 Million	100 Million	~140,000	100 Million
Crystal	[100] Cubic, ZB	[100] Cubic, ZB	[100], Cubic,ZB, WU	Any Any	Any Any
Strain	-	VFF	VFF	-	MVFF
Multi-physics	-				Spin, Classical
Parallel Comp.	3 levels 23,000 cores	1 level 80 cores	3 levels 30,000 cores	4 levels 220,000 co	4 levels 100,000 cores



Core Code / Theory Development

- NEMO-1D (Texas Instruments '94-'98, JPL '98-'03)
  - »Roger Lake, R. Chris Bowen, Dan Blanks
- NEMO3D (NASA JPL, Purdue, '98-'07)
  - »R. Chris Bowen, Fabiano Oyafuso, Seungwon Lee
- NEMO3D-peta (Purdue, '06-'11)
  - »Hoon Ryu, Sunhee Lee
- OMEN (ETH, Purdue, '06-'11)
  - »Mathieu Luisier
- NEMO5 (Purdue, '09-'12)
  - »Michael Povolotsky, Hong-Hyun Park, Sebastian Steiger, Tillmann Kubis,Jim Fonseca,Arvind Ajoy,Bozidar Novakovic, Rajib Rahman
  - »Junzhe Gang, Kaspar Haume, Yu He, Ganesh Hegde, Yuling Hsueh, Hesam Ilatikhameneh, Zhengping Jiang, SungGeun Kim, Daniel Lemus, Daniel Mejia, Kai Miao, Samik Mukherjee, Seung Hyun Park, Ahmed Reza, Mehdi Salmani, Parijat Sengupta, Saima Sharmin, Archana Tankasala, Daniel Valencia, Yaohua Tan, Evan Wilson

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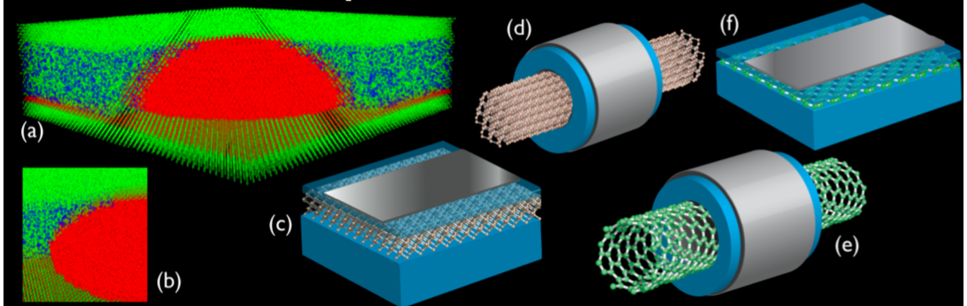
Compute Intensive: NEMO/OMEN



18 years development
- Texas Instruments
- NASA JPL
- Purdue

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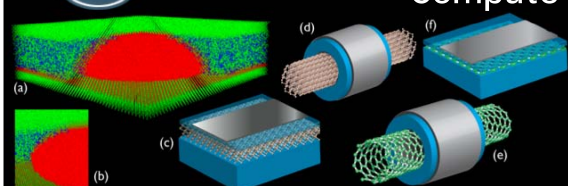
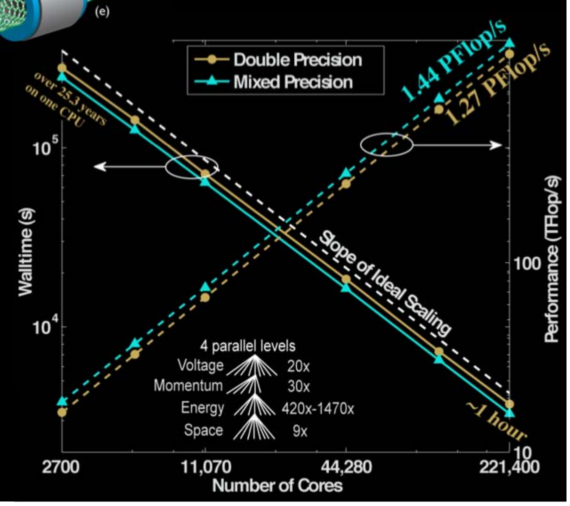
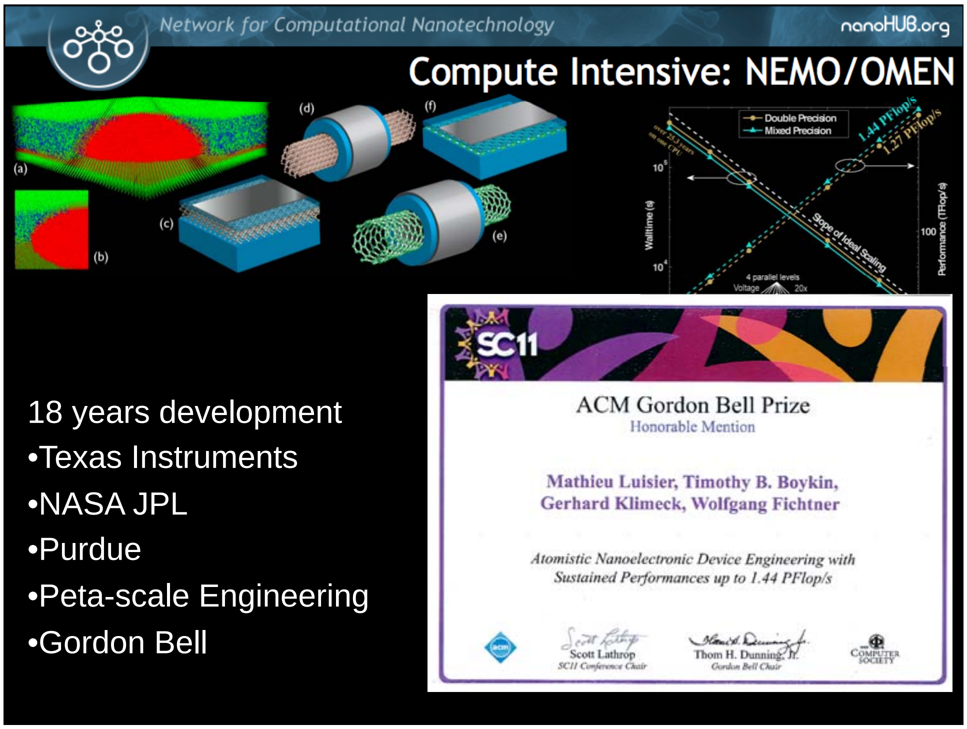
Compute Intensive: NEMO/OMEN

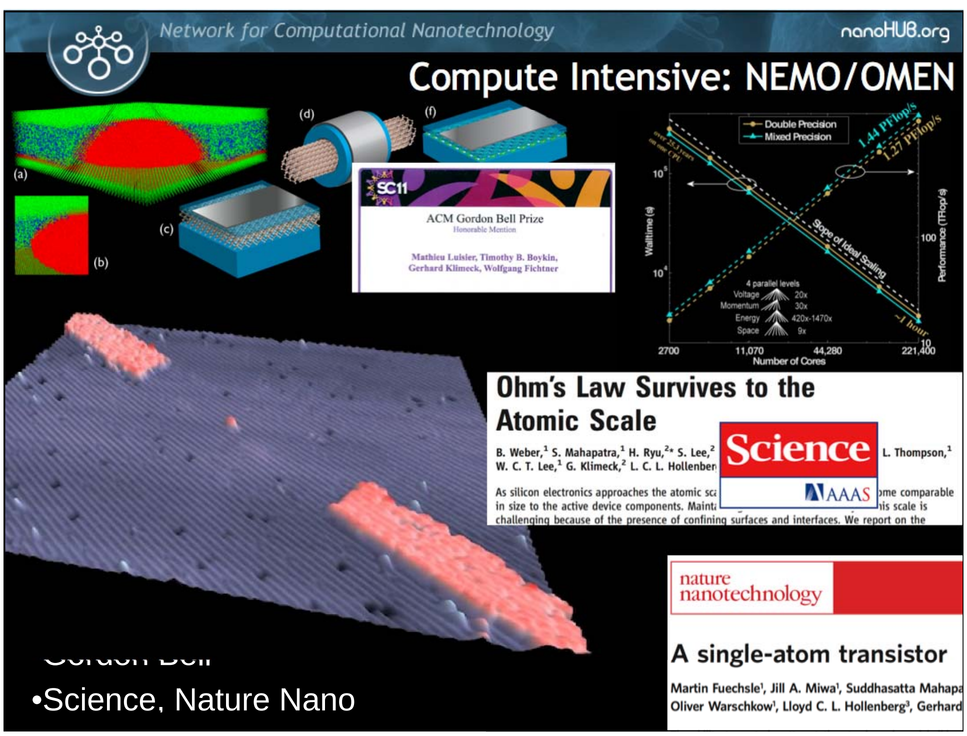


18 years development
- Texas Instruments
- NASA JPL
- Purdue
- Peta-scale Engineering

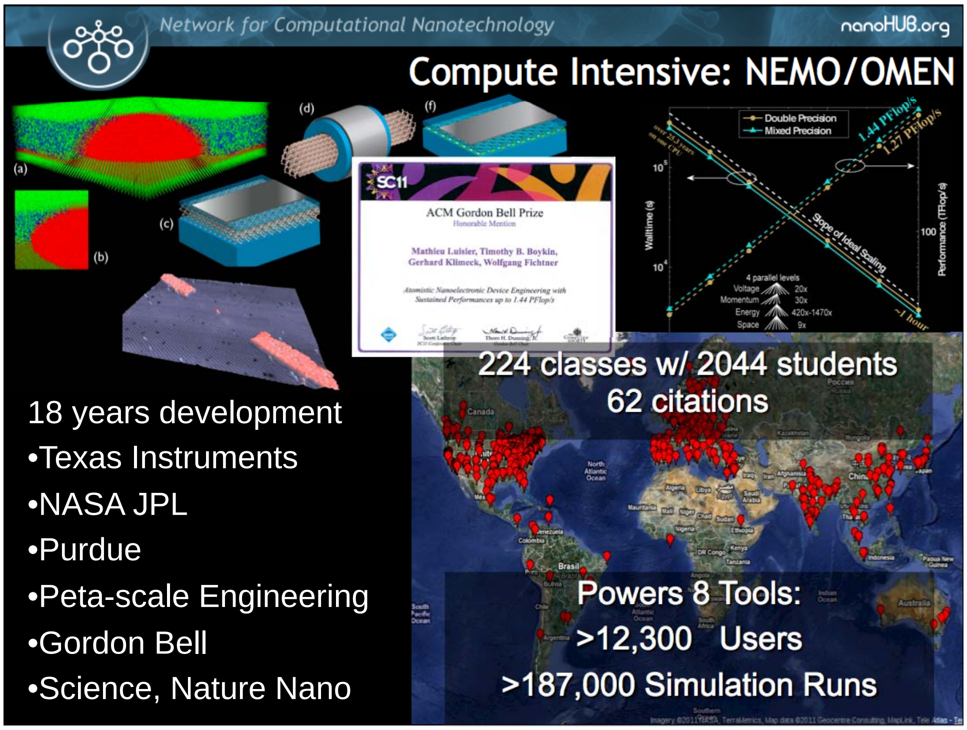




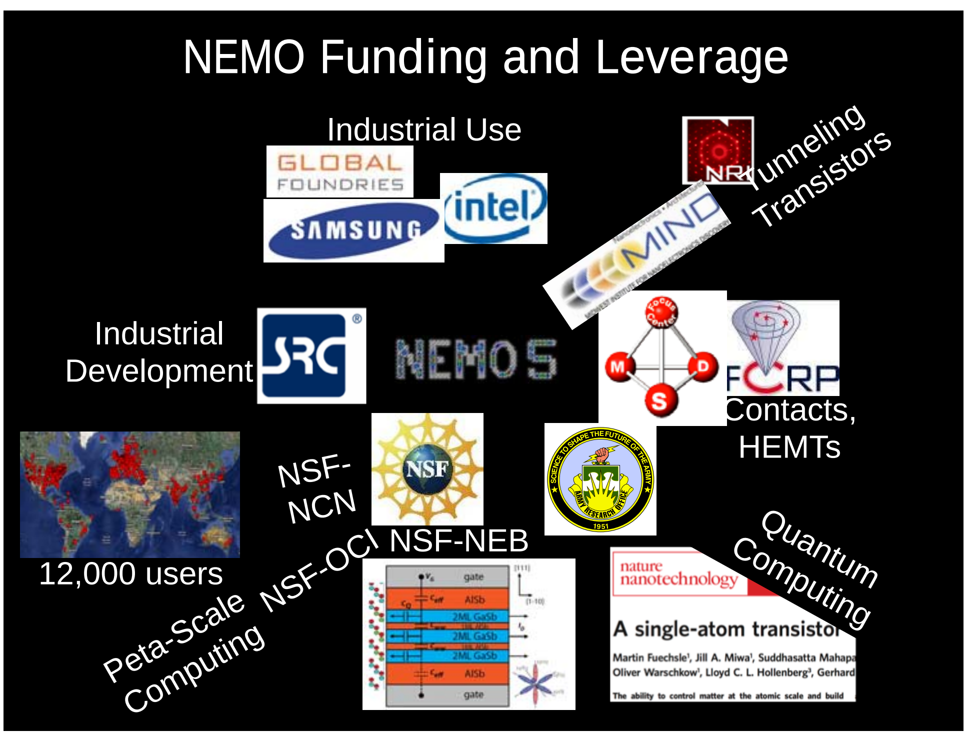
Network for Computational Nanotechnology
nanoHUB.org
Compute Intensive: NEMO/OMEN
(a)
(b)
(c)
(d)
(e)
(f)
Double Precision
Mixed Precision
1.44 PFlop/s
1.27 PFlop/s
Slope of Ideal Scaling
Walltime (s)
Performance (TFlop/s)
4 parallel levels
Voltage
20x
18 years development
•Texas Instruments
•NASA JPL
•Purdue
•Peta-scale Engineering
•Gordon Bell
SC11
ACM Gordon Bell Prize
Honorable Mention
Mathieu Luisier, Timothy B. Boykin,
Gerhard Klimeck, Wolfgang Fichtner
Atomistic Nanoelectronic Device Engineering with
Sustained Performances up to 1.44 PFlop/s
Scott Lathrop
SC11 Conference Chair
Thom H. Dunning, Jr.
Gordon Bell Chair



Network for Computational Nanotechnology
nanoHUB.org
Compute Intensive: NEMO/OMEN
(a)
(b)
(c)
(d)
(f)
SC11
ACM Gordon Bell Prize
Honorable Mention
Mathieu Luisier, Timothy B. Boykin,
Gerhard Klimeck, Wolfgang Fichtner
Double Precision
Mixed Precision
1.44 PFlop/s
1.27 PFlop/s
Slope of Ideal Scaling
Walltime (s)
Performance (TFlop/s)
4 parallel levels
Voltage 20x
Momentum 30x
Energy 420x-1470x
Space 9x
~1 hour
2700
11,070
44,280
221,400
Number of Cores
Ohm's Law Survives to the
Atomic Scale
Science
AAAS
nature nanotechnology
A single-atom transistor
•Science, Nature Nano



Network for Computational Nanotechnology
nanoHUB.org
Compute Intensive: NEMO/OMEN
ACM Gordon Bell Prize
Mathieu Luisier, Timothy B. Boykin, Gerhard Klimeck, Wolfgang Fichtner
1.44 PFlop/s
1.27 PFlop/s
Double Precision
Mixed Precision
Slope of Ideal Scaling
224 classes w/ 2044 students
62 citations
18 years development
•Texas Instruments
•NASA JPL
•Purdue
•Peta-scale Engineering
•Gordon Bell
•Science, Nature Nano
Powers 8 Tools:
>12,300 Users
>187,000 Simulation Runs

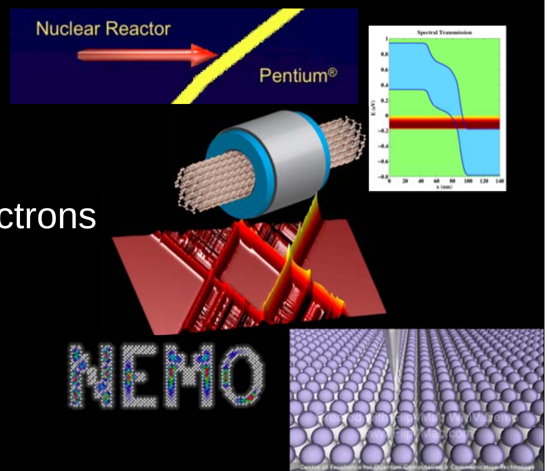


NEMO Funding and Leverage
Industrial Use
GLOBAL FOUNDRIES
SAMSUNG
intel
NRI
MIND
Tunneling Transistors
Industrial Development
SRC
NEMO 5
FCRP
Contacts, HEMTs
NSF-NCN
NSF
NSF-NEB
12,000 users
Peta-Scale Computing
NSF-OCI
nature nanotechnology
A single-atom transistor
Quantum Computing

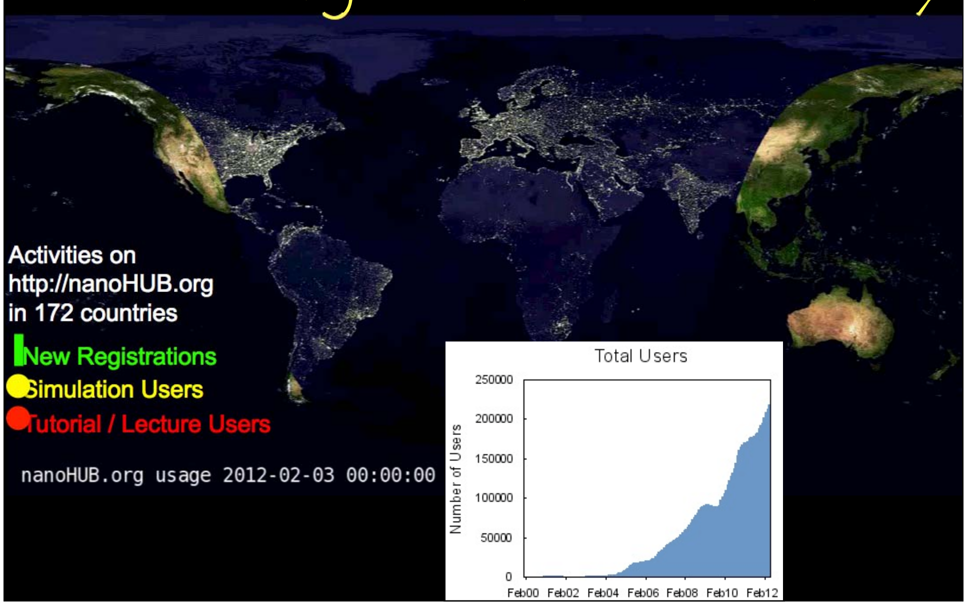
The single-atom transistor

Presentation Outline

- Why?
  - A power problem
  - Near term solution
  - Continuum invalid
    => finite atoms/electrons
- What is it?
  - Coulomb diamond
  - How is it built?
- How to model this?
  - NEMO
- Where to study this?
  - nanoHUB.org



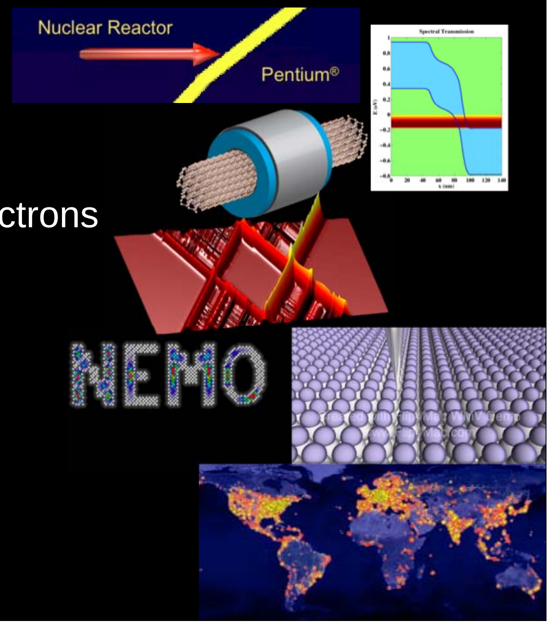
nanoHUB
World's Largest Nano User Facility



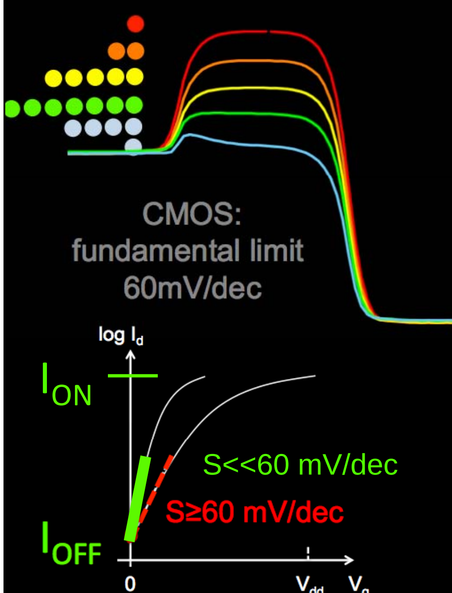
The single-atom transistor

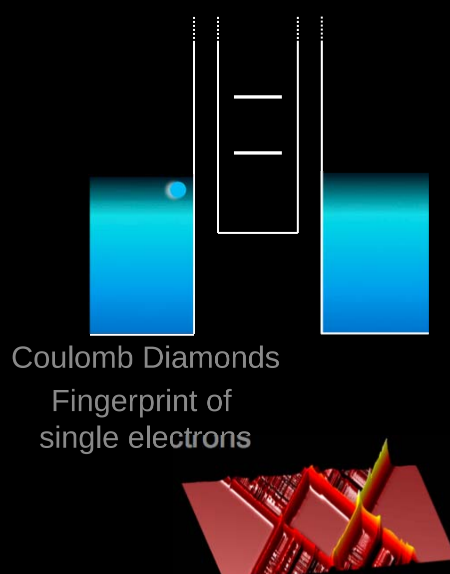
Presentation Outline

- Why?
  - A power problem
  - Near term solution
  - Continuum invalid
    => finite atoms/electrons
- What is it?
  - Coulomb diamond
  - How is it built?
- How to model this?
  - NEMO
- Where to study this?
  - nanoHUB.org

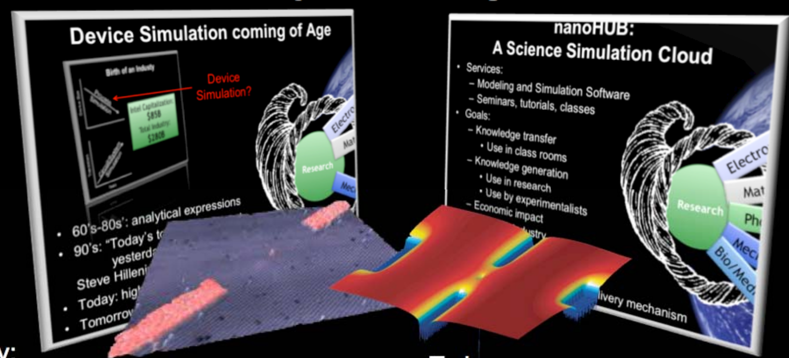


Teaching Moments





Key Messages



Today:
- Drift Diffusion fit to atomistic model

Tomorrow:
- Quantum at the core
- 5nm transistors with metals by design

Future:
- Wires: 1 atom tall, 4 atoms wide
- Transistor made of one P atom
- Quantum computing

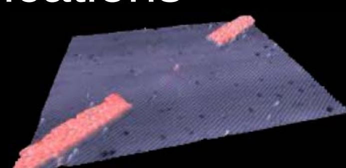
Today:
- Software as a service delivered to thousands in an open science gateway
- No code rewrite needed

Tomorrow:
- Vendors embrace software as a service

What are the implications?....

Single Atom Transistor: Future Implications

Other limits to Moore's Law (real world issues)
- Mass production
  - Not today
  - Zyvex maybe "tomorrow"
- Room temperature operation
  - Not today
  - Need other impurity
- Single Electron circuit architectures
  - Research available
  - Stray charges



Research Today:
- Atomic physical limit of Moore's law (not accidental)
- Wires: 1 atom tall, 4 atoms wide
- Transistor made of one P atom
- Goal / funding: Quantum computing
- NEMO5 calibration
  - Atomistic, discrete
  - Realistically extended

Thank You!

Research Group
@Purdue
@NASA JPL 1998-2003
@Texas Instruments 1994-1998

Collaborators:
Michelle Simmons, Sydney
Lloyd Hollenberg, Melbourne
Alan Seabaugh, Notre Dame

Thank You!