Chapter 13
Small-Signal Modeling and Linear Amplification

Microelectronic Circuit Design

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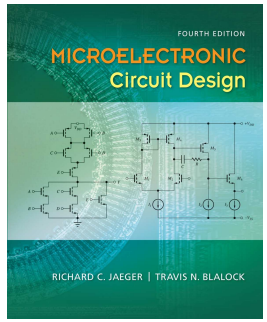


Chapter Goals

Understanding of concepts related to:

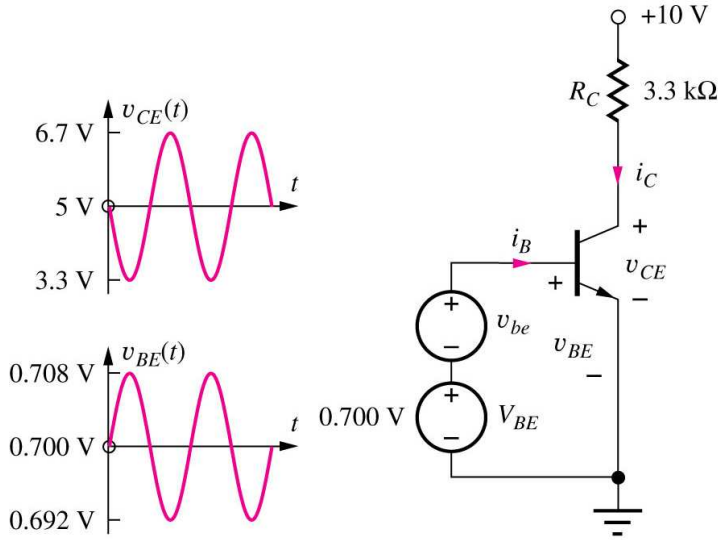
- Transistors as linear amplifiers
- dc and ac equivalent circuits
- Use of coupling and bypass capacitors and inductors to modify dc and ac equivalent circuits
- Concept of small-signal voltages and currents
- Small-signal models for diodes and transistors
- Identification of common-source and common-emitter amplifiers
- Amplifier characteristics such as voltage gain, input and output resistances, and linear signal range
- Rule-of-thumb estimates for the voltage gain of common-emitter and common-source amplifiers.

Introduction to Amplifiers

- Amplifiers usually use electronic devices operating in the Active Region
  - A BJT is used as an amplifier when biased in the forward-active region
  - The FET can be used as amplifier if operated in the pinch-off or saturation region
- In these regions, transistors can provide high voltage, current and power gains
- Bias is provided to stabilize the operating point (the Q-Point) in the desired region of operation
- Q-point also determines
  - Small-signal parameters of transistor
  - Voltage gain, input resistance, output resistance
  - Maximum input and output signal amplitudes
  - Power consumption

Transistor Amplifiers

BJT Amplifier Concept



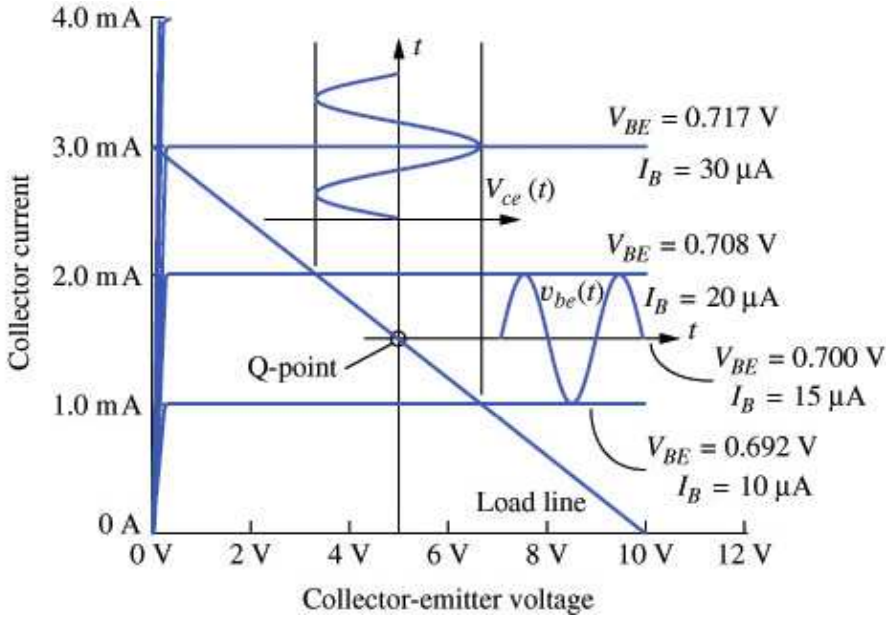
The BJT is biased in the active region by dc voltage source V_{BE}. Q-point is set at $(I_C, V_{CE}) = (1.5\text{ mA}, 5\text{ V})$ with $I_B = 15\ \mu\text{A}$ $(\beta_F = 100)$

Total base-emitter voltage is: $v_{BE} = V_{BE} + v_{be}$

Collector-emitter voltage is: $v_{CE} = 10 - i_C R_C$ This is the load line equation.

Transistor Amplifiers

BJT Amplifier (cont.)



8 mV peak change in v_{BE} gives 5 μA change in i_B and 0.5 mA change in i_C.

0.5 mA change in i_C produces a 1.65 V change in v_{CE} .

If changes in operating currents and voltages are small enough, then i_C and v_{CE} waveforms are undistorted replicas of the input signal.

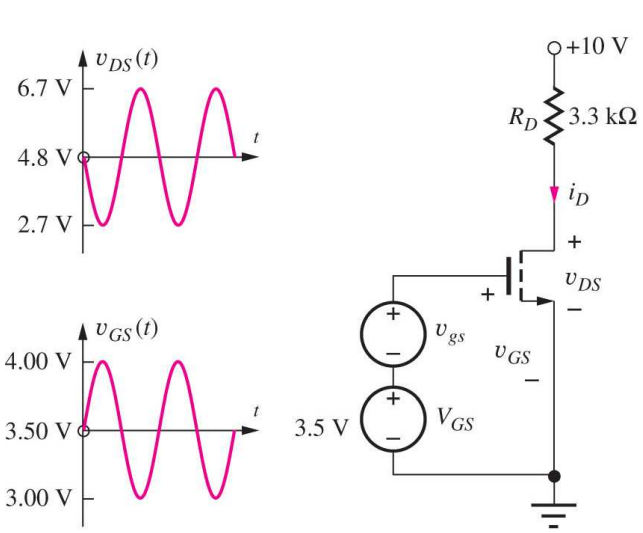
A small voltage change at the base causes a large voltage change at collector. Voltage gain is given by:

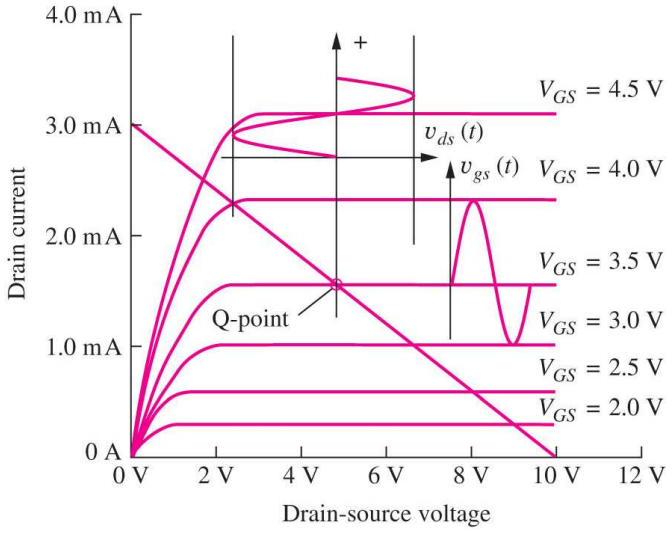
$$A_v = \frac{V_{ce}}{V_{be}} = \frac{1.65\angle 180^o}{0.008\angle 0^o} = 206\angle 180^o = -206$$

Minus sign indicates 180º phase shift between th einput and output signals.

Transistor Amplifiers

MOSFET Amplifier Concept





$$A_v = \frac{V_{ds}}{V_{gs}}$$

$$A_v = \frac{4\angle 180^o}{1\angle 0^o}$$

$$A_v = -4.00$$

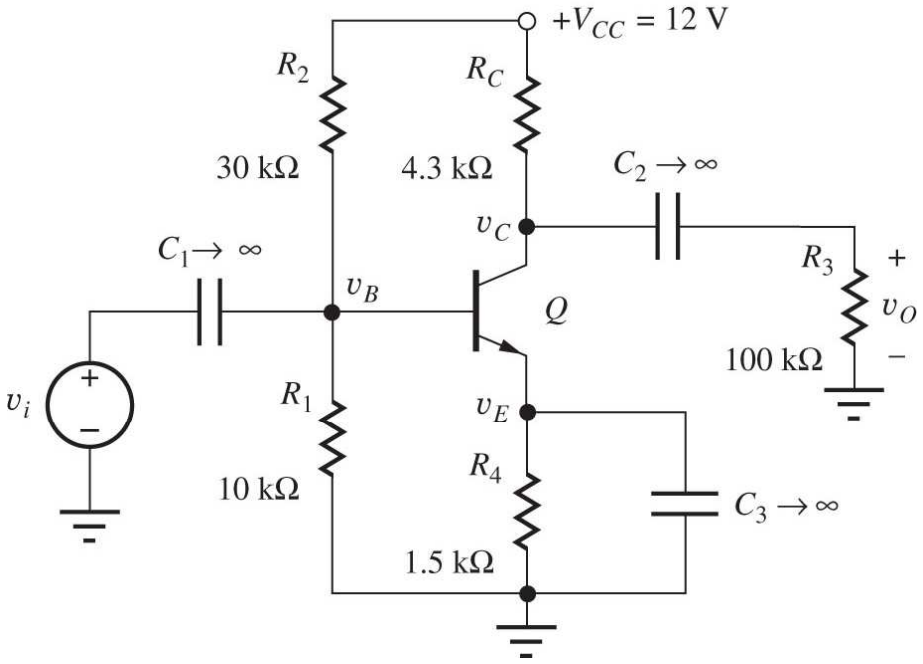
MOSFET is biased in active region by dc voltage source V_{GS}. Q-point is set at (I_D, V_{DS}) = (1.56 mA, 4.8 V) with V_{GS} = 3.5 V

Total gate-source voltage is: $v_{GS} = V_{GS} + v_{gs}$

1 $V_{p\text{-}p}$ change in v_{GS} yields 1.25 $mA_{p\text{-}p}$ change in i_D and a 4 $V_{p\text{-}p}$ change in v_{DS}

Transistor Amplifiers

Coupling and Bypass Capacitors



ac coupling through capacitors is used to inject ac input signal and extract output signal without disturbing Q-point

Capacitors are designed to provide negligible impedance at frequencies of interest and provide open circuits at dc.

C_1 and C_2 are low impedance coupling capacitors or dc blocking capacitors whose reactance at the signal frequency is designed to be negligible.

C_3 is a bypass capacitor that provides a low impedance path for ac current from emitter to ground, thereby removing R_E (required for good Q-point stability) from the circuit when ac signals are considered.

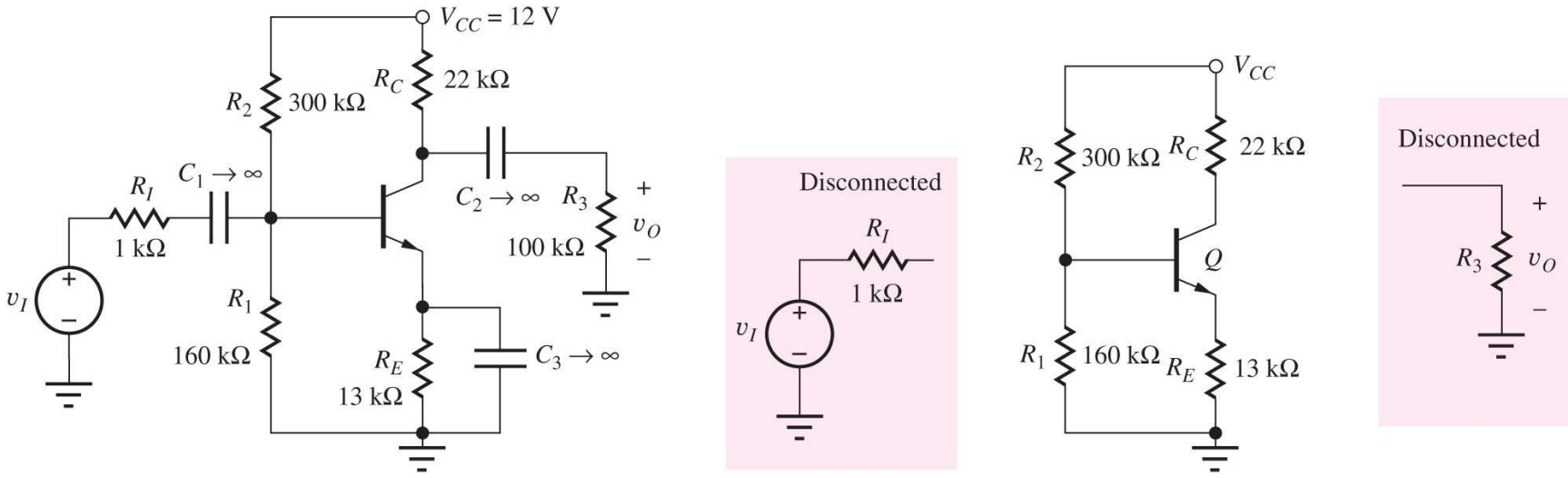
Transistor Amplifiers

dc and ac Analysis – Two Step Analysis

- dc analysis:
  - Find dc equivalent circuit by replacing all capacitors by open circuits and inductors by short circuits.
  - Find Q-point from dc equivalent circuit by using appropriate large-signal transistor model.
- ac analysis:
  - Find ac equivalent circuit by replacing all capacitors by short circuits, inductors by open circuits, dc voltage sources by ground connections and dc current sources by open circuits.
  - Replace transistor by its small-signal model
  - Use small-signal ac equivalent to analyze ac characteristics of amplifier.
  - Combine end results of dc and ac analysis to yield total voltages and currents in the network.

Transistor Amplifiers

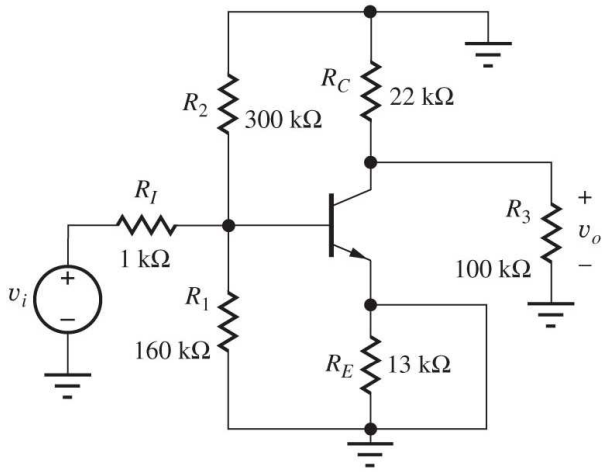
dc Equivalent Circuit for BJT Amplifier



- All capacitors in the original amplifier circuit are replaced by open circuits, disconnecting v_I, R_I, and R_3 from circuit.

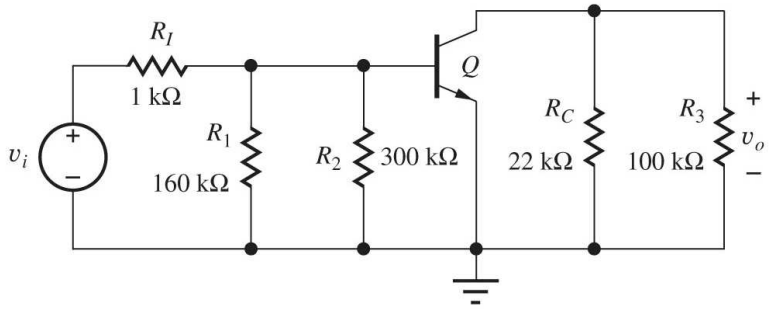
Transistor Amplifiers

ac Equivalent Circuit for BJT Amplifier

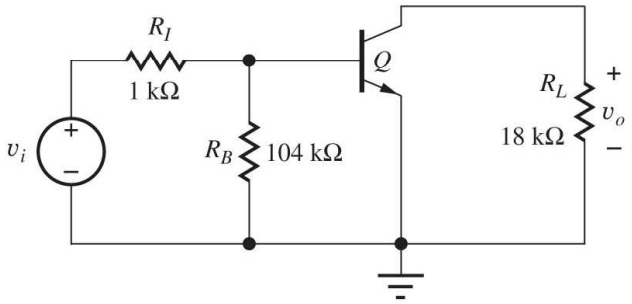


(c)

Capacitors are replaced by short circuits



(d)



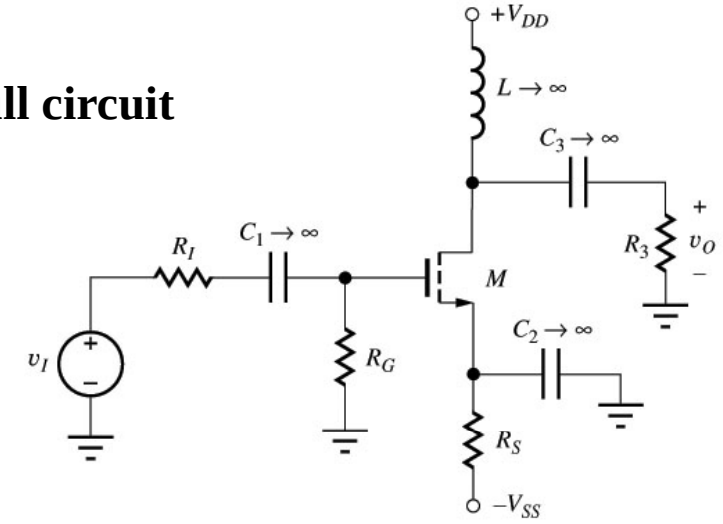
$$R_B = R_1 \| R_2 = 100\text{k}\Omega \| 300\text{k}\Omega$$

$$R = R_C \| R_3 = 22\text{k}\Omega \| 100\text{k}\Omega$$

Transistor Amplifiers

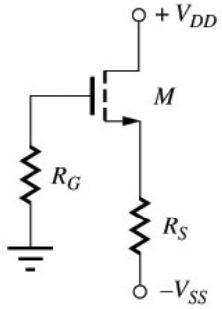
dc and ac Equivalents for a MOSFET Amplifier

Full circuit



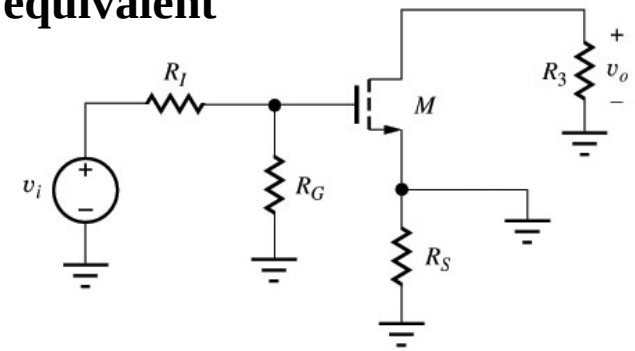
(a)

dc equivalent

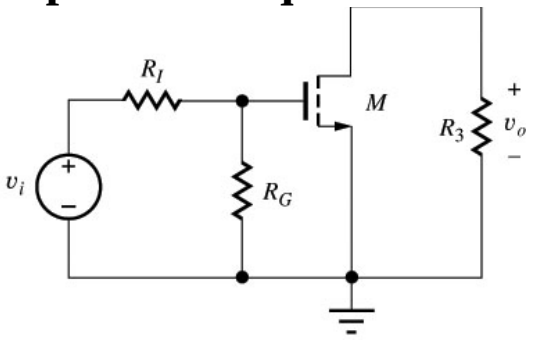


(b)

ac equivalent

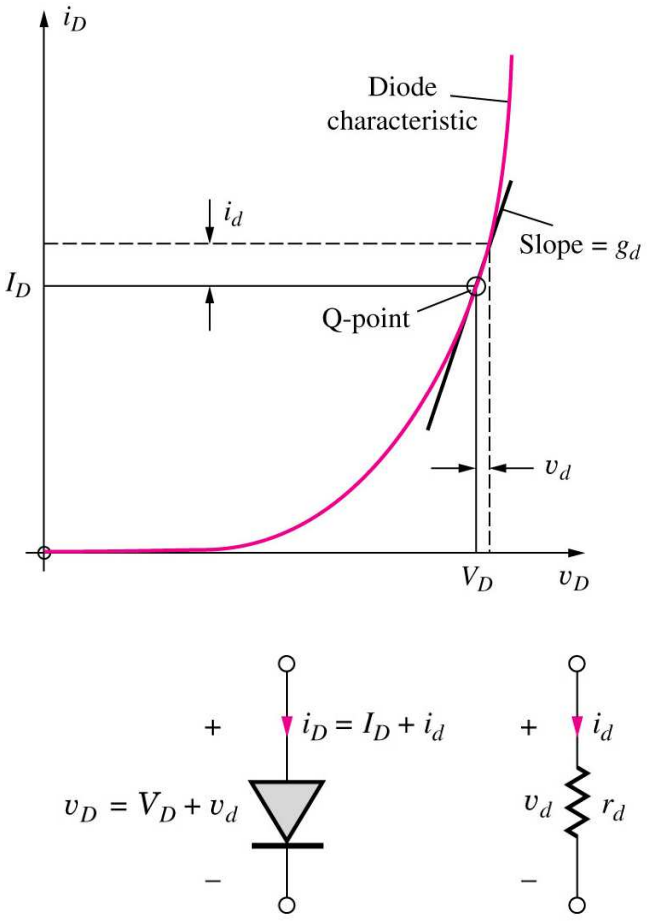


Simplified ac equivalent



Small-Signal Operation

Diode Small-Signal Model



- The slope of the diode characteristic at the Q-point is called the **diode conductance** and is given by:

$$g_d = \left.\frac{\partial i_D}{\partial v_D}\right|_{Q-point} = \frac{I_S}{V_T}\exp\left(\frac{V_D}{V_T}\right) = \frac{I_D + I_S}{V_T}$$

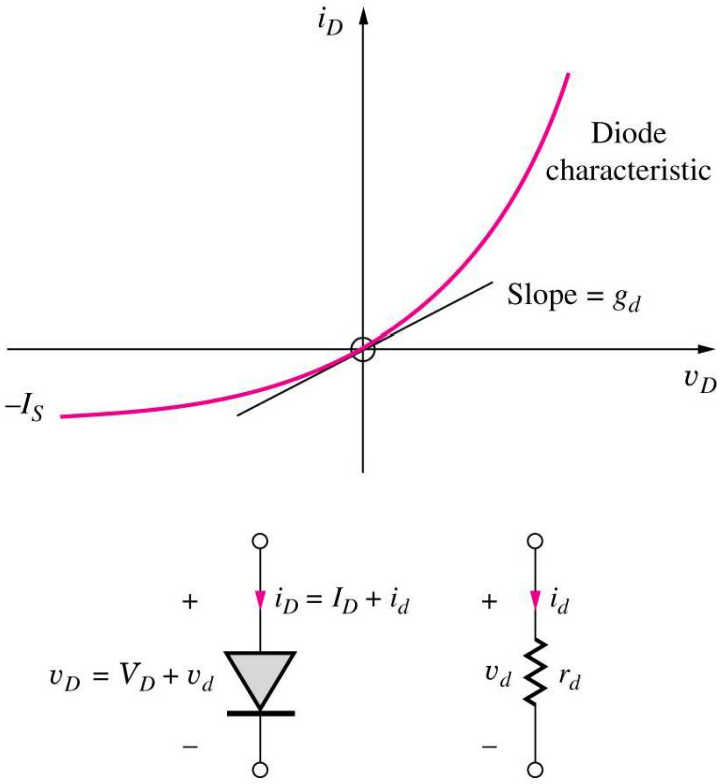
$$g_d \cong \frac{I_D}{V_T} \cong \frac{I_D}{0.025\text{V}} = 40 I_D \quad \text{for} \quad I_D >> I_S$$

- **Diode resistance** is given by:

$$r_d = \frac{1}{g_d}$$

Small-Signal Operation

Diode Small-Signal Model (cont.)



- g_d is small but non-zero for $I_D = 0$ because slope of diode equation is nonzero at the origin.
- At the origin, the diode conductance and resistance are given by:

$$g_d = \frac{I_S}{V_T} \quad \text{and} \quad r_d = \frac{V_T}{I_S}$$

Small-Signal Operation

Definition of a Small-Signal

Now let's determine the largest magnitude of v_d that represents a small signal.

$$i_D = I_S\left[\exp\left(\frac{v_D}{V_T}\right)-1\right] \qquad \therefore I_D + i_d = I_S\left[\exp\left(\frac{V_D+v_d}{V_T}\right)-1\right]$$

$$I_D + i_d = I_S\left[\exp\left(\frac{V_D}{V_T}\right)-1\right] + I_S\exp\left(\frac{v_D}{V_T}\right)\left[\frac{v_d}{V_T}+\frac{1}{2}\left(\frac{v_d}{V_T}\right)^2+\frac{1}{6}\left(\frac{v_d}{V_T}\right)^3+\ldots\right]$$

Subtracting I_D from both sides of the equation,

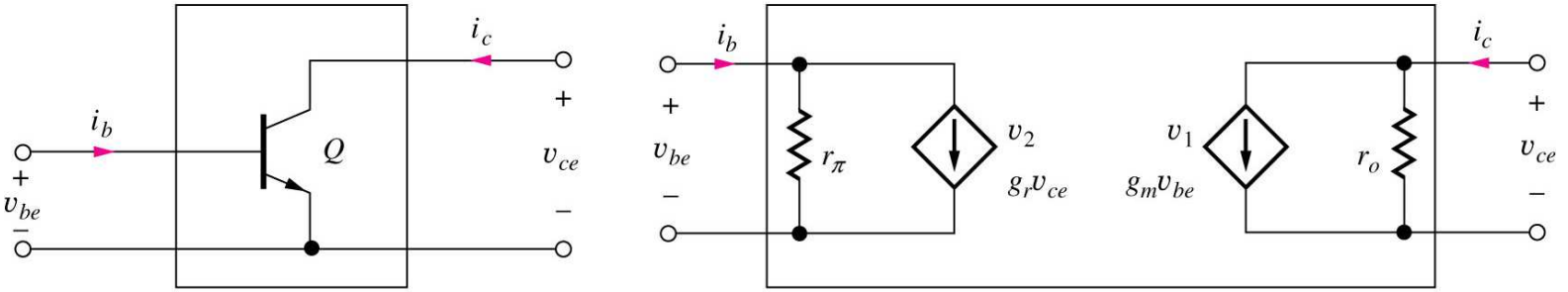
$$i_d = (I_D+I_S)\left[\frac{v_d}{V_T}+\frac{1}{2}\left(\frac{v_d}{V_T}\right)^2+\frac{1}{6}\left(\frac{v_d}{V_T}\right)^3+\ldots\right]$$

For i_d to be a linear function of signal voltage v_d, $v_d << 2V_T = 0.05$ V or $v_d \leq 5$ mV. Thus $v_d \leq 5$ mV represents the requirement for small-signal (linear) operation of the diode.

$$\therefore i_d = (I_D+I_S)\left(\frac{v_d}{V_T}\right) = g_d v_d \quad \Rightarrow \quad i_D = I_D + g_d v_d$$

Small-Signal Operation

BJT Small-Signal Model (The Hybrid-Pi Model)



The bipolar transistor is assumed to be operating in the Forward-Active Region:

$$i_C \cong I_S \exp\left(\frac{v_{BE}}{V_T}\right)\left(1+\frac{v_{CE}}{V_A}\right) \qquad \text{and} \qquad i_B \cong \frac{i_C}{\beta_F} \qquad \left(V_{CE} \geq V_{BE}\right)$$

Using a two-port *y*-parameter network:

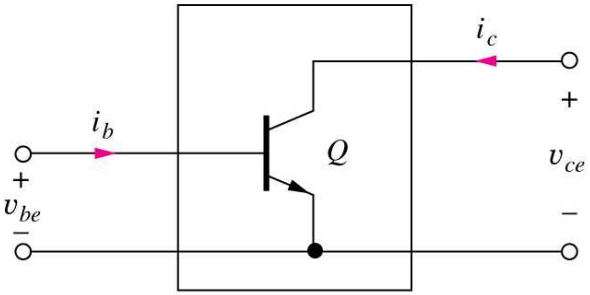
$$i_c = g_m v_{be} + g_o v_{ce}$$

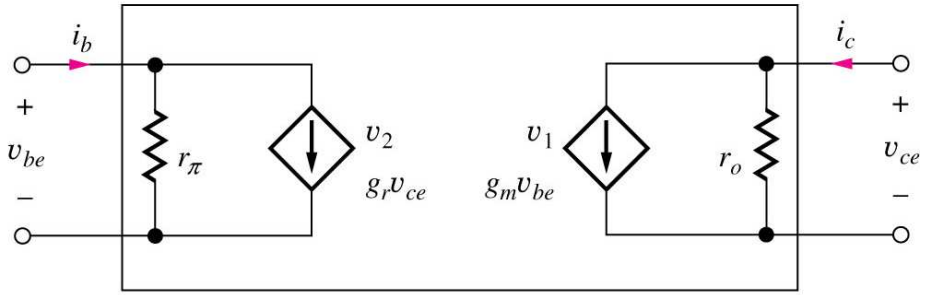
$$i_b = g_\pi v_{be} + g_r v_{ce}$$

The port variables can represent either time-varying part of total voltages and currents or small changes in them away from Q-point values.

Small-Signal Operation

BJT Small-Signal Model (The Hybrid-Pi Model)





$$i_c = g_m v_{be} + g_o v_{ce}$$

$$i_b = g_\pi v_{be} + g_r v_{ce}$$

$$i_C \cong I_S \exp\left(\frac{v_{BE}}{V_T}\right)\left(1+\frac{v_{CE}}{V_A}\right)$$

$$i_B \cong \frac{i_C}{\beta_F}$$

β_o is called the **small-signal common-emitter current gain** of the BJT.

$$g_m = \left.\frac{i_c}{v_{be}}\right|_{v_{ce}=0} = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{\text{Q-point}} = \frac{I_C}{V_T}$$

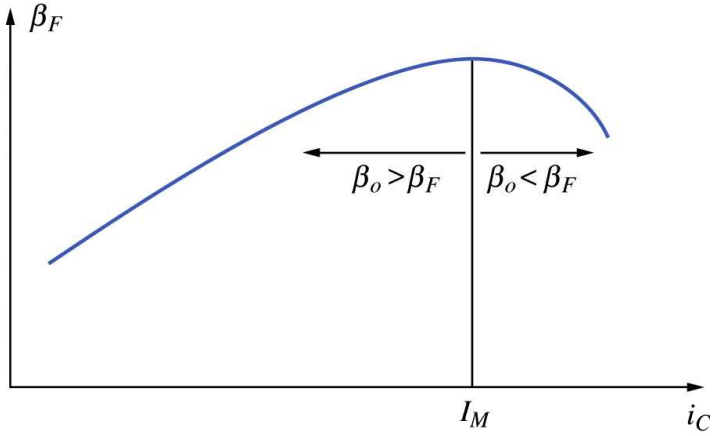
$$g_o = \left.\frac{i_c}{v_{ce}}\right|_{v_{be}=0} = \left.\frac{\partial i_C}{\partial v_{CE}}\right|_{\text{Q-point}} = \frac{I_C}{V_A + V_T}$$

$$g_\pi = \left.\frac{i_b}{v_{be}}\right|_{v_{ce}=0} = \left.\frac{\partial i_B}{\partial v_{BE}}\right|_{\text{Q-point}} = \frac{I_C}{\beta_o V_T}$$

$$g_r = \left.\frac{i_b}{v_{ce}}\right|_{v_{be}=0} = \left.\frac{\partial i_B}{\partial v_{CE}}\right|_{\text{Q-point}} = 0$$

BJT Small-Signal Operation

Current Gain & Intrinsic Voltage Gain



$$\beta_o = g_m r_\pi = \frac{\beta_F}{\left[1 - I_C\left(\frac{1}{\beta_F}\frac{\partial \beta_F}{\partial i_C}\right)_{Q-point}\right]}$$

$\beta_o > \beta_F$ for $i_C < I_M$, and $\beta_o < \beta_F$ for $i_C > I_M$. However, for simplicity β_F and β_o will be assumed to be equal

Intrinsic voltage gain is defined by:

$$\mu_f = g_m r_o = \frac{I_C}{V_T}\left(\frac{V_A + V_{CE}}{I_C}\right) = \frac{V_A + V_{CE}}{V_T}$$

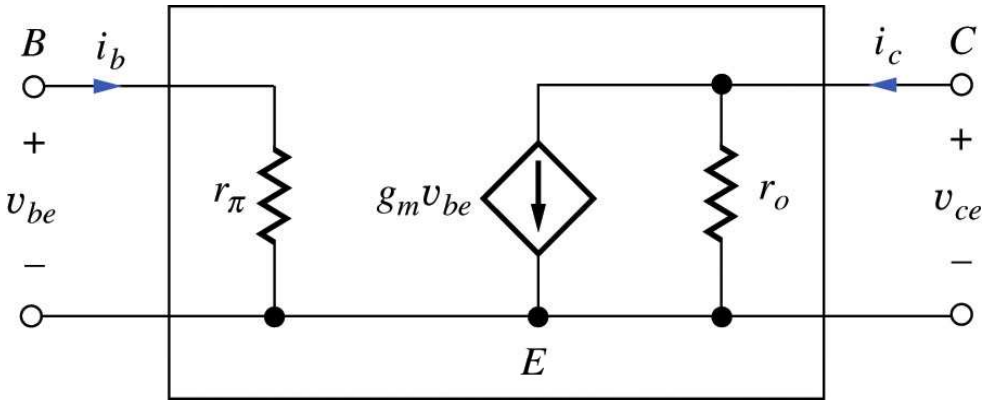
For $V_{CE} << V_A$

$$\mu_f \cong \frac{V_A}{V_T} \cong 40 V_A$$

μ_f represents the maximum voltage gain an individual BJT can provide and does not change with operating point.

Small-Signal Operation

BJT Hybrid-Pi Model - Summary



- The hybrid-pi small-signal model is the intrinsic representation of the BJT.
- Small-signal parameters are controlled by the Q-point and are independent of geometry of the BJT

Transconductance:

$$g_m = \frac{I_C}{V_T} \cong 40 I_C$$

Input resistance:

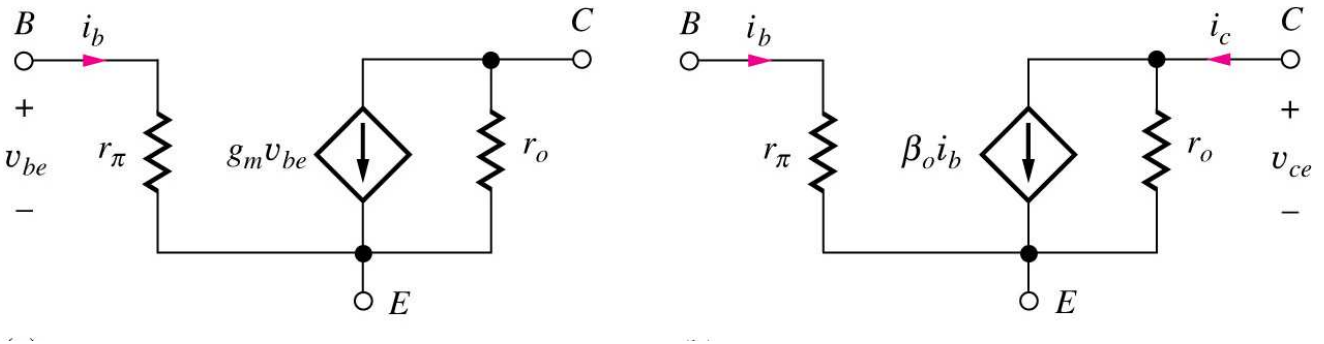
$$r_\pi = \frac{\beta_o V_T}{I_C} = \frac{\beta_o}{g_m} \quad \text{or} \quad \beta_o = g_m r_\pi$$

Output resistance:

$$r_o = \frac{V_A + V_{CE}}{I_C} \cong \frac{V_A}{I_C}$$

BJT Small-Signal Operation

Equivalent Forms of Small-Signal Model



- Voltage-controlled current source $g_m v_{be}$ can be transformed into current-controlled current source,

$$v_{be} = i_b r_\pi$$

$$g_m v_{be} = g_m i_b r_\pi = \beta_o i_b$$

$$i_c = \beta_o i_b + \frac{v_{ce}}{r_o} \cong \beta_o i_b$$

- Basic relationship $i_c = \beta i_b$ is useful in both dc and ac analysis when the BJT is in the forward-active region.

BJT Small-Signal Operation

Small-Signal Definition

$$i_C = I_S \exp\left(\frac{v_{BE}}{V_T}\right) = I_S \exp\left(\frac{V_{BE} + v_{be}}{V_T}\right) \qquad \therefore i_C = I_C + i_c = I_S \exp\left(\frac{V_{BE}}{V_T}\right)\exp\left(\frac{v_{be}}{V_T}\right) = I_C \exp\left(\frac{v_{be}}{V_T}\right)$$

$$I_C + i_c = I_C\left[1 + \left(\frac{v_{be}}{V_T}\right) + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^3 + \cdots\right]$$

$$\therefore i_c = I_C\left[\left(\frac{v_{be}}{V_T}\right) + \frac{1}{2}\left(\frac{v_{be}}{V_T}\right)^2 + \frac{1}{6}\left(\frac{v_{be}}{V_T}\right)^3 + \cdots\right]$$

For linearity, i_c should be proportional to v_{be} with $v_{be} << 2V_T$ or $v_{be} \leq 0.005$ V.

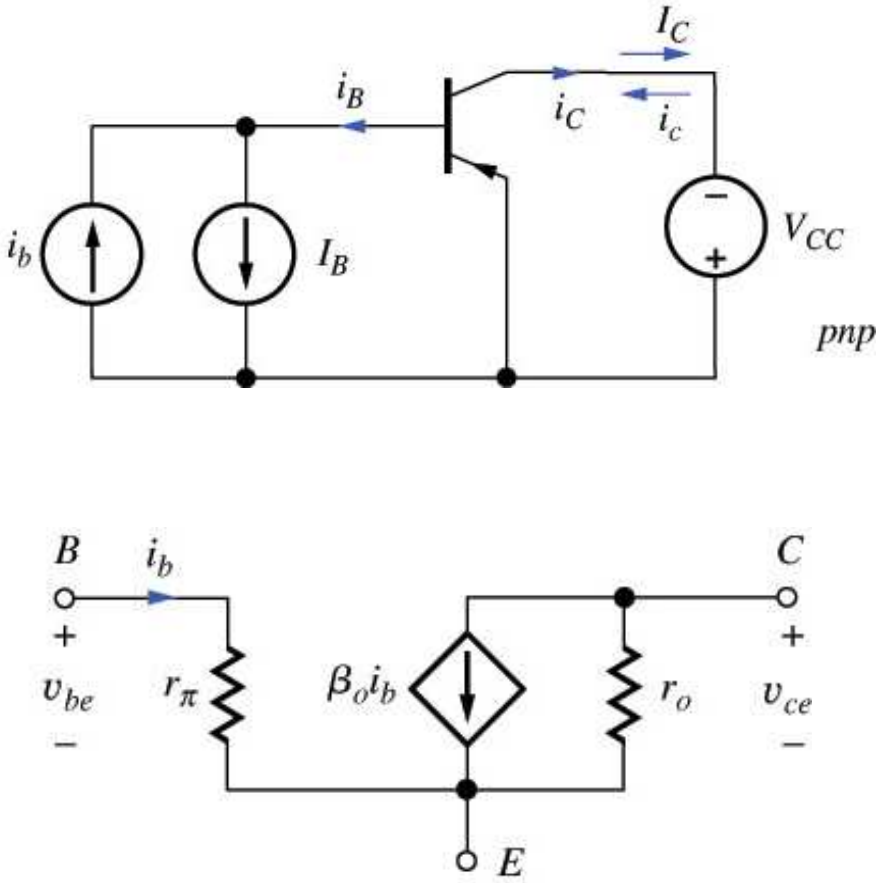
$$i_C \cong I_C\left(1 + \frac{v_{be}}{V_T}\right) = I_C + I_C\frac{v_{be}}{V_T} = I_C + g_m v_{be}$$

The change in i_c that corresponds to small-signal operation is:

$$\frac{i_c}{I_C} = \frac{v_{be}}{V_T} \leq \frac{0.005V}{0.025V} = 0.200$$

BJT Small-Signal Operation

Small-Signal Model for *pnp* Transistor



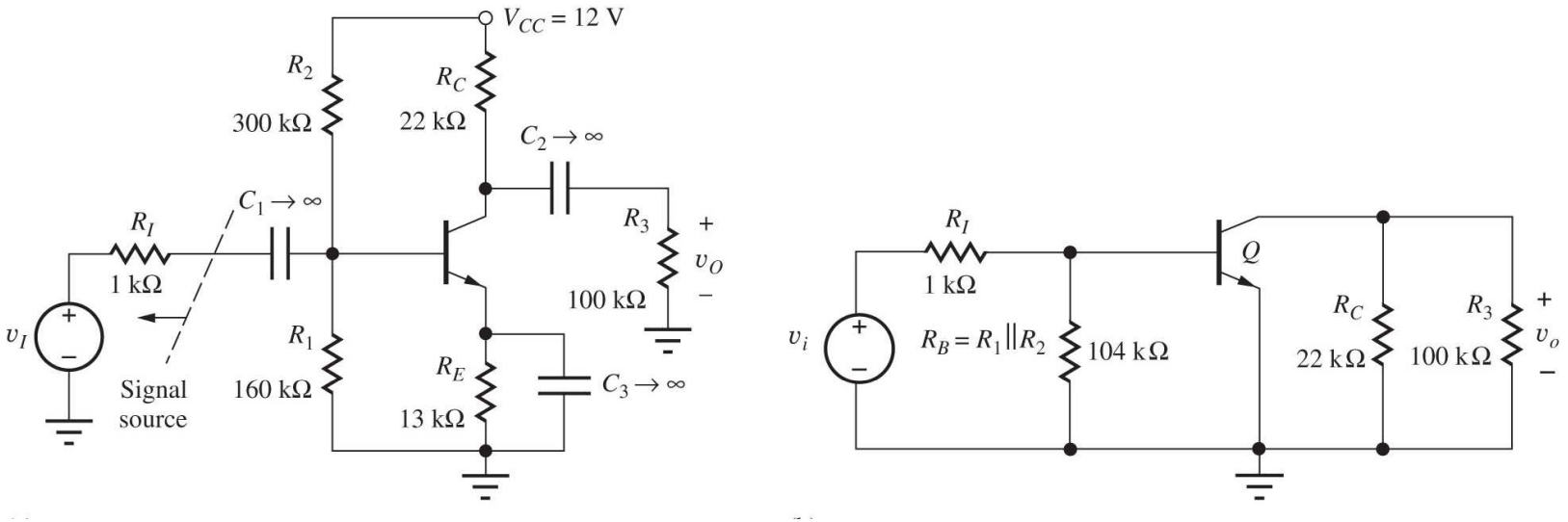
- For the *pnp* transistor

$$i_B = I_B - i_b$$
$$i_C = I_C - i_c = \beta_F I_B - \beta_F i_b$$

- Signal current injected into base causes decrease in total collector current which is equivalent to increase in signal current entering collector.
- So the small-signal models for the npn and pnp devices are identical!

Common-Emitter Amplifiers

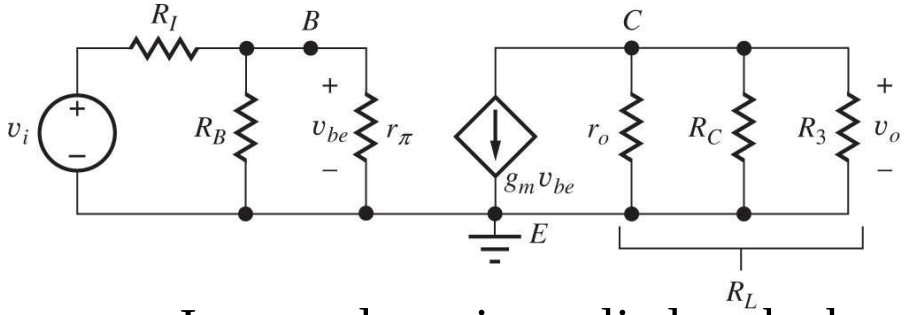
Small-Signal Analysis - ac Equivalent Circuit

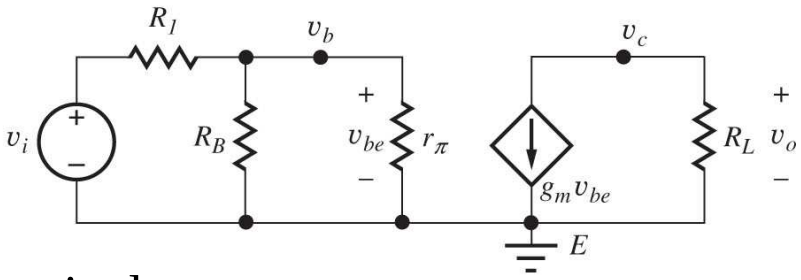


- ac equivalent circuit is constructed by assuming that all capacitances have zero impedance at signal frequency and dc voltage sources are ac ground.
- Assume that Q-point is already known.

Common-Emitter Amplifiers

Small-Signal Equivalent Circuit



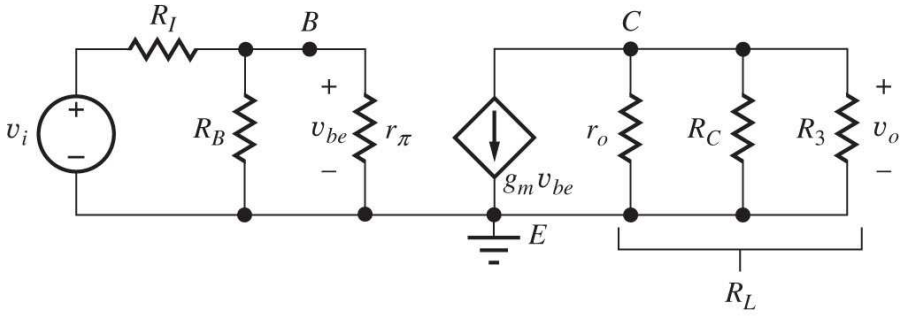


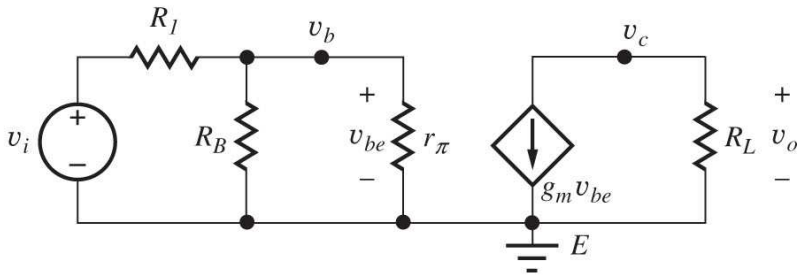
- Input voltage is applied to the base terminal
- Output signal appears at collector terminal
- Emitter is *common* to both input and output signals
  Thus circuit is termed a Common-Emitter (C-E) Amplifier.
- The terminal gain of the C-E amplifier is the gain from the base terminal to the collector terminal

$$A_{vt}^{CE} = \frac{v_c}{v_b} = -g_m R_L \qquad R_L = r_o \| R_C \| R_3$$

Common-Emitter Amplifiers

Input Resistance and Signal Source Gain





Define R_{iB} as the input resistance looking into the base of the transistor:

$$R_{iB} = \frac{v_b}{i_b} = r_\pi$$

The input resistance presented to v_i is:

$$R_{in} = R_I + R_B \| R_{iB} = R_I + R_B \| r_\pi$$

The signal source voltage gain is:

$$A_v^{CE} = \frac{v_o}{v_i} = \frac{v_o}{v_b}\frac{v_b}{v_i} = A_{vt}^{CE}\frac{R_B \| r_\pi}{R_I + R_B \| r_\pi}$$

Common-Emitter Amplifiers

"Rule of Thumb" Design Estimate

$$A_v^{CE} = A_{vt}^{CE}\frac{R_B \| r_\pi}{R_I + R_B \| r_\pi} \cong A_{vt}^{CE} \qquad A_{vt}^{CE} = -g_m R_L \qquad R_L = r_o \| R_C \| R_3$$

Typically: $r_o >> R_C$ and $R_3 >> R_C$ $\qquad A_v^{CE} \cong -g_m R_C = -40 I_C R_C$

$I_C R_C$ represents the voltage dropped across collector resistor R_C

A typical design point is $\qquad I_C R_C = \frac{V_{CC}}{3}$

$$\therefore A_v^{CE} \cong -40\frac{V_{CC}}{3} = 13.3 V_{CC}$$

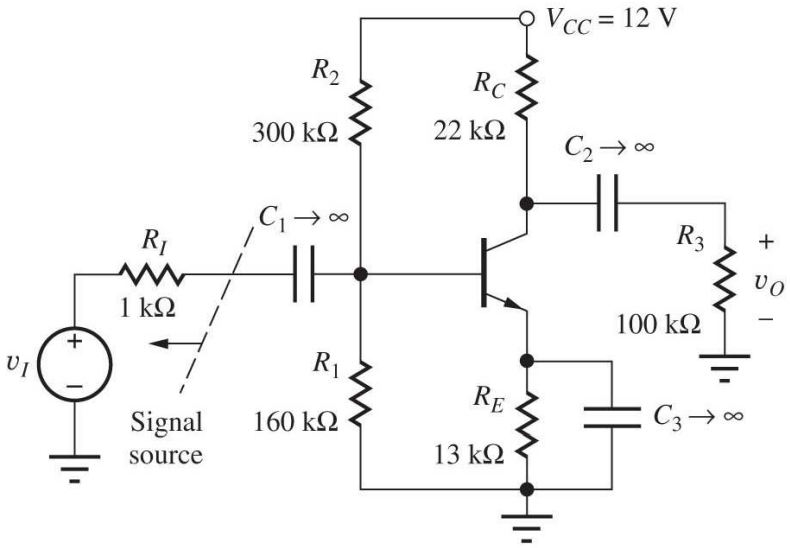
To help account for all the approximations and have a number that is easy to remember, our "rule-of-thumb" estimate for the voltage gain becomes

$$A_v^{CE} \cong -10 V_{CC}$$

Common-Emitter Amplifiers

Voltage Gain Example

- **Problem:** Calculate voltage gain, input resistance and maximum input signal level for a common-emitter amplifier with a specified Q-point
- **Given data:** β_F = 100, V_A = 75 V, Q-point is (0.245 mA, 3.39 V)
- **Assumptions:** Transistor is in active region, $\beta_O = \beta_F$. Signals are low enough to be considered small signals. Room temperature.
- **Analysis:**



$$g_m = 40 I_C = 40(0.245mA) = 9.80\ mS \qquad r_\pi = \frac{\beta_o}{g_m} = \frac{100}{9.8mS} = 10.2\ k\Omega$$

$$r_o = \frac{V_A + V_{CE}}{I_C} = \frac{75V + 3.39V}{0.245mA} = 320\ k\Omega \qquad R_B = R_1 \| R_2 = 160k\Omega \| 300k\Omega = 104\ k\Omega$$

$$R_L = r_o \| R_C \| R_L = 320k\Omega \| 22k\Omega \| 100k\Omega = 17.1\ k\Omega \qquad R_B \| r_\pi = 104k\Omega \| 10.2k\Omega = 9.29\ k\Omega$$

Common-Emitter Amplifiers

Voltage Gain Example (cont.)

Analysis (cont):

$$A_v = -g_m R_L \left(\frac{R_B \| r_\pi}{R_I + R_B \| r_\pi} \right) = -9.8mS\left(17.1k\Omega\right)\left(\frac{9.29k\Omega}{1k\Omega + 9.29k\Omega} \right) = -168\left(0.903\right) = -151$$

$$R_{in} = R_I + R_B \| r_\pi = 10.3\ k\Omega$$

$$v_{be} = v_i \left(\frac{R_B \| r_\pi}{R_I + R_B \| r_\pi} \right) \qquad \therefore v_{be} \le 0.005V \rightarrow v_i \le 5mV \left(\frac{10.3k\Omega}{9.29k\Omega} \right) = 5.54\ mV$$

Check the rule-of-thumb estimate: $A_v^{CE} \cong -10\left(12\right) = -120$ (ballpark estimate)

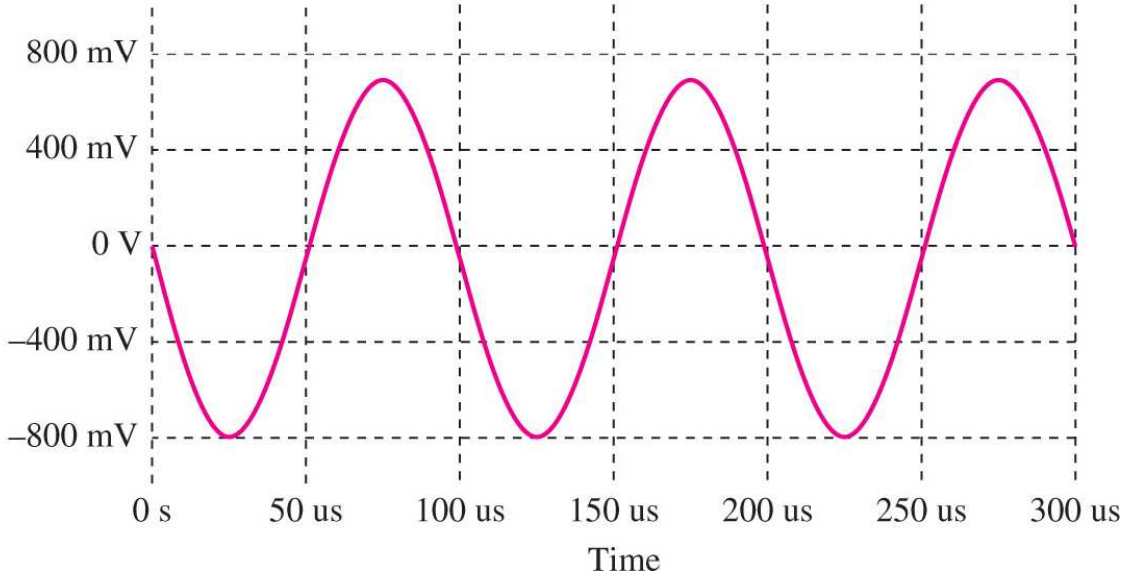
What is the maximum amplitude of the output signal: $v_o \le 5.54mV\left(-151\right) = 0.837\ V$

Common-Emitter Amplifiers

Voltage Gain Example (cont.)

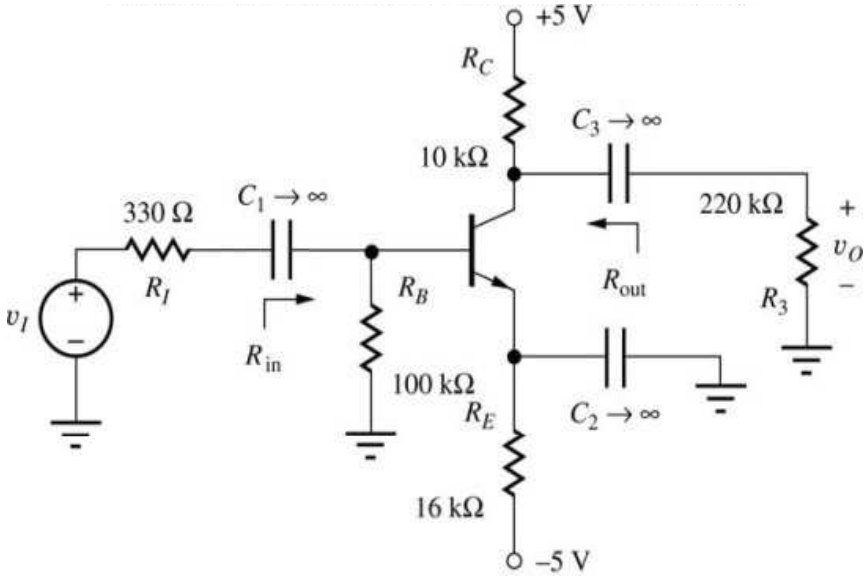
Simulation Results: The graph below presents the output voltage for an input voltage that is a 5-mV, 10-kHz sine wave.

Note that although the sine wave at first looks good, the positive and negative peak amplitudes are different indicating the presence of distortion. The input is near our small-signal limit for linear operation.



Common-Emitter Amplifiers

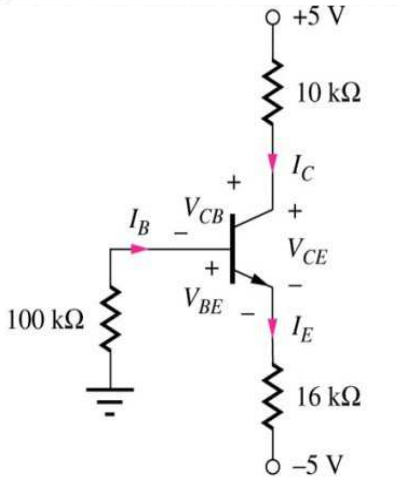
Dual Supply Operation - Example



- **Problem:** Find voltage gain, input and output resistances for the circuit above
- **Given data:** $\beta_F = 65$, $V_A = 50$ V
- **Assumptions:** Active-region operation, $V_{BE} = 0.7$ V, small signal operating conditions.

Analysis: To find the Q-point, the dc equivalent circuit is constructed.

$$10^5 I_B + V_{BE} + (\beta_F + 1) I_B (1.6 \times 10^4) = 5$$



$$\therefore I_B = 3.71\ \mu A$$

$$I_C = 65 I_B = 241\ \mu A$$

$$I_E = 66 I_B = 245\ \mu A$$

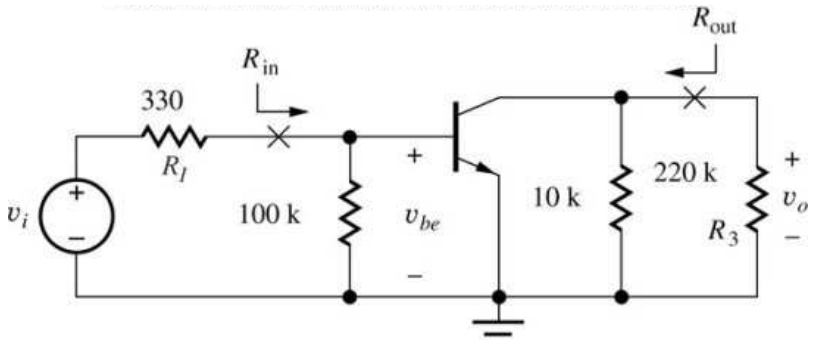
$$5 - 10^4 I_C - V_{CE} - (1.6 \times 10^4) I_E - (-5) = 0$$

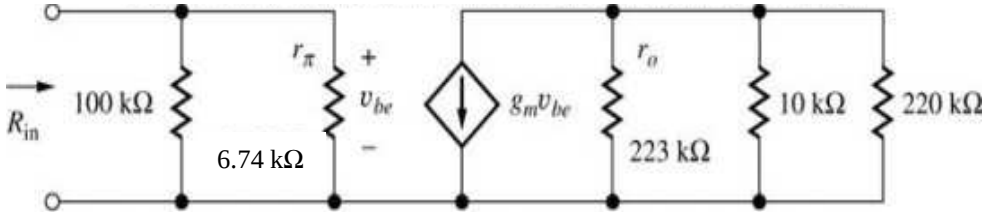
$$\therefore V_{CE} = 3.67\ V$$

Common-Emitter Amplifiers

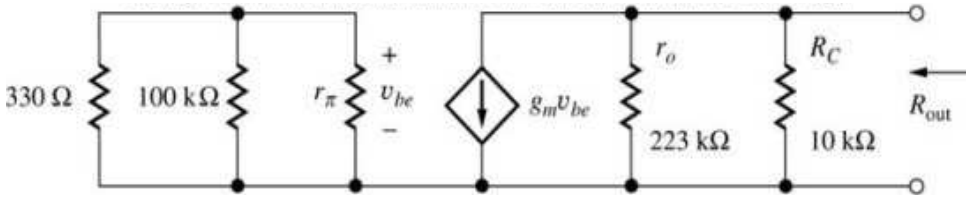
Dual Supply Operation - Example (cont.)

Next we construct the ac equivalent and simplify it.





$$R_{in} = R_B \| r_\pi = 6.31\ k\Omega$$



$$g_m = 40 I_C = 9.64 \times 10^{-3}\ S$$

$$r_\pi = \frac{\beta_o}{40 I_C} = 6.74\ k\Omega$$

$$r_o = \frac{V_A + V_{CE}}{I_C} = 223\ k\Omega$$

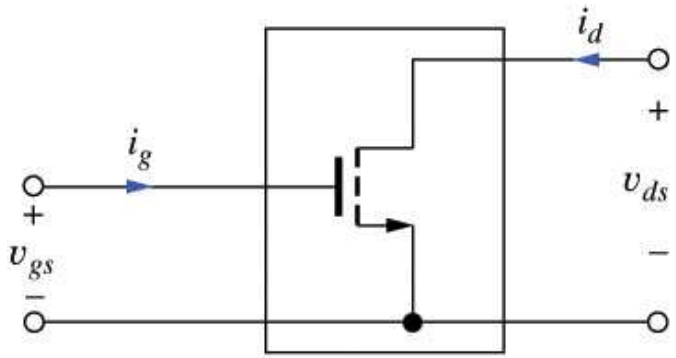
$$R_{out} = R_C \| r_o = 9.57\ k\Omega$$

$$A_v^{CE} = \frac{v_o}{v_i} = -g_m \left(R_{out} \| R_3\right)\left(\frac{R_{in}}{R_I + R_{in}}\right) = -84.0$$

Gain Estimate: $A_v^{CE} \cong -10\left(V_{CC} + V_{EE}\right) = -100$

Small-Signal Operation

MOSFET Small-Signal Model



Using a two-port *y*-parameter network,

$$i_g = g_\pi v_{gs} + g_r v_{ds}$$

$$i_d = g_m v_{gs} + g_o v_{ds}$$

The port variables can represent either time-varying part of total voltages and currents or small changes in them away from Q-point values.

$$g_\pi = \left.\frac{i_g}{v_{gs}}\right|_{v_{ds}=0} = \left.\frac{\partial i_G}{\partial v_{GS}}\right|_{\text{Q-point}}$$

$$g_r = \left.\frac{i_g}{v_{ds}}\right|_{v_{ds}=0} = \left.\frac{\partial i_G}{\partial v_{DS}}\right|_{\text{Q-point}}$$

$$g_m = \left.\frac{i_d}{v_{gs}}\right|_{v_{ds}=0} = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{\text{Q-point}}$$

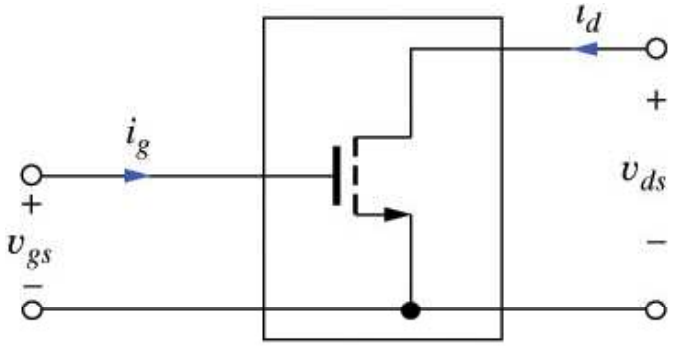
$$g_o = \left.\frac{i_d}{v_{ds}}\right|_{v_{ds}=0} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{\text{Q-point}}$$

$$I_G = 0$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)$$

Small-Signal Operation

MOSFET Small-Signal Model (cont.)



$$I_G = 0$$

$$I_D = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2\left(1 + \lambda V_{DS}\right)$$

$$g_\pi = \left.\frac{\partial i_G}{\partial v_{GS}}\right|_{\text{Q-point}} = 0$$

$$g_r = \left.\frac{\partial i_G}{\partial v_{DS}}\right|_{\text{Q-point}} = 0$$

$$i_g = g_\pi v_{gs} + g_r v_{ds}$$

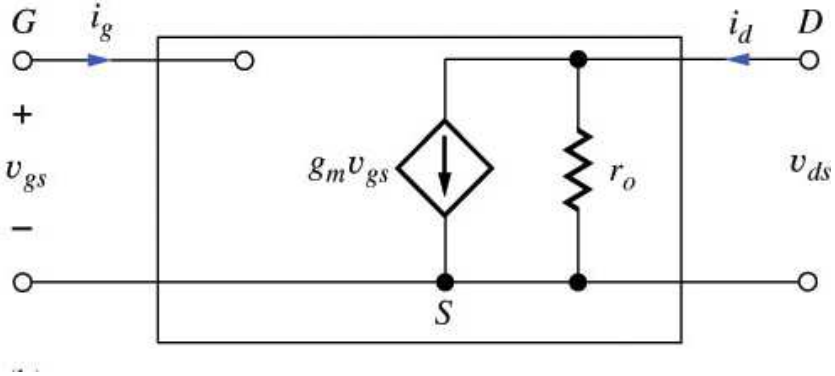
$$i_d = g_m v_{gs} + g_o v_{ds}$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{\text{Q-point}} = \frac{K_n}{2}\left(V_{GS} - V_{TN}\right)\left(1 + \lambda V_{DS}\right) = \frac{2I_D}{V_{GS} - V_{TN}}$$

$$g_o = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{\text{Q-point}} = \lambda\frac{K_n}{2}\left(V_{GS} - V_{TN}\right)^2 = \frac{\lambda I_D}{1 + \lambda V_{DS}} = \frac{I_D}{\frac{1}{\lambda} + V_{DS}}$$

Small-Signal Operation

MOSFET Small-Signal Model - Summary



- Since gate is insulated from channel by gate-oxide input resistance of transistor is infinite.
- Small-signal parameters are controlled by the Q-point.
- For the same operating point, MOSFET has lower transconductance and an output resistance that is similar to the BJT.

Transconductance:

$$g_m = \frac{2I_D}{V_{GS} - V_{TN}} = \sqrt{2K_n I_D}$$

Output resistance:

$$r_o = \frac{1}{g_o} = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda I_D}$$

Amplification factor for $\lambda V_{DS} << 1$:

$$\mu_f = g_m r_o = \frac{1 + \lambda V_{DS}}{\lambda I_D} \cong \frac{1}{\lambda}\sqrt{\frac{2K_n}{I_D}}$$

MOSFET Small-Signal Operation

Small-Signal Definition

Assume $\lambda v_{DS} << 1$. Then $i_D \cong \frac{K_n}{2}\left(v_{GS} - V_{TN}\right)^2$ for $v_{DS} \geq v_{GS} - V_{TN}$

For $v_{GS} = V_{GS} + v_{gs}$, $i_D = I_D + i_d = \frac{K_n}{2}\left[\left(v_{GS} - V_{TN}\right)^2 + 2v_{gs}\left(V_{GS} - V_{TN}\right) + v_{gs}^2\right]$

$\therefore i_d = \frac{K_n}{2}\left[2v_{gs}\left(V_{GS} - V_{TN}\right) + v_{gs}^2\right]$

For linearity, i_d should be proportional to v_{gs} and we require $v_{gs}^2 << 2v_{gs}\left(V_{GS} - V_{TN}\right)$

or $v_{gs} << 2\left(V_{GS} - V_{TN}\right) \quad \rightarrow \quad v_{gs} \leq 0.2\left(V_{GS} - V_{TN}\right)$

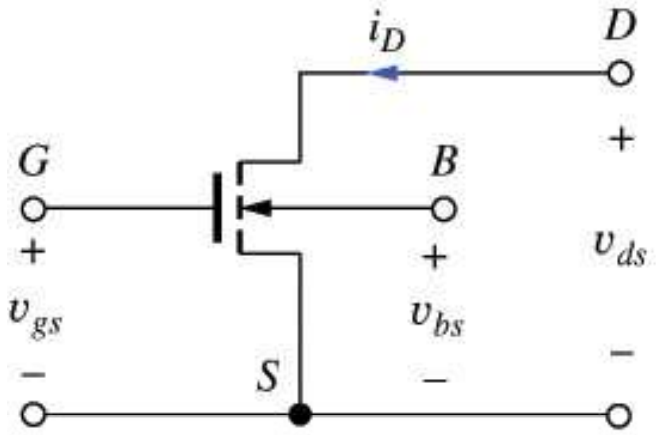
Since the MOSFET can be biased with (V_{GS} - V_{TN}) equal to several volts, it can handle much larger values of v_{gs} than corresponding the values of v_{be} for the BJT.

The change in drain current that corresponds to small-signal operation is:

$$\frac{i_d}{I_D} = \left(\frac{g_m}{I_D}\right)v_{gs} \leq \frac{2}{V_{GS} - V_{TN}}\left[0.2\left(V_{GS} - V_{TN}\right)\right] \quad \rightarrow \quad \frac{i_d}{I_D} \leq 0.4$$

MOSFET Small-Signal Operation

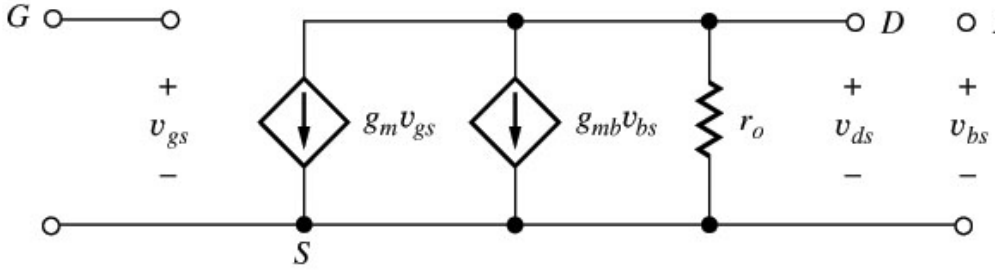
Body Effect in Four-terminal MOSFETs



Drain current depends on threshold voltage which in turn depends on v_{SB}. **Back-gate transconductance** is:

$$g_{mb} = \left.\frac{\partial i_D}{\partial v_{BS}}\right|_{\text{Q-point}} = -\left.\frac{\partial i_D}{\partial v_{SB}}\right|_{\text{Q-point}}$$

$$g_{mb} = -\left(\frac{\partial i_D}{\partial V_{TN}}\right)\left.\left(\frac{\partial V_{TN}}{\partial v_{SB}}\right)\right|_{\text{Q-point}} = -(-g_m\eta) = g_m\eta$$

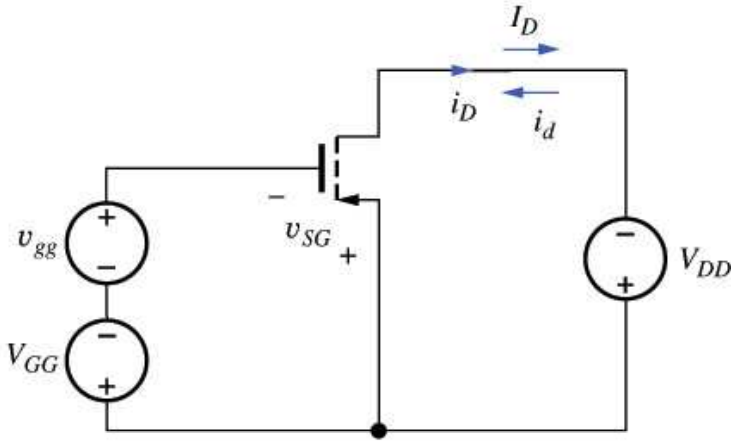


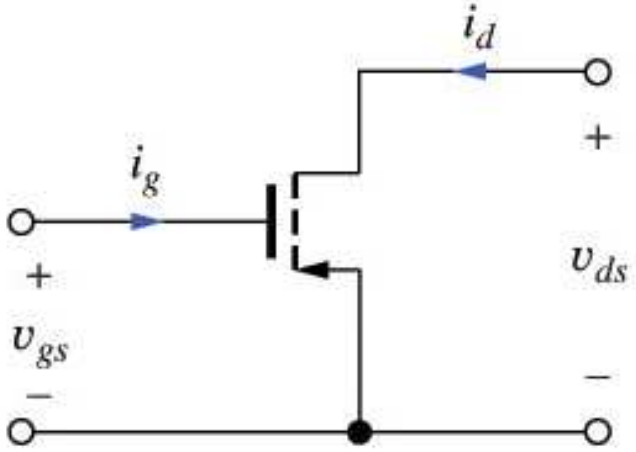
$0 < \eta < 3$ is called the back-gate transconductance parameter.

The bulk terminal is a reverse-biased diode. Hence, no conductance from the bulk terminal to other terminals.

MOSFET Small-Signal Operation

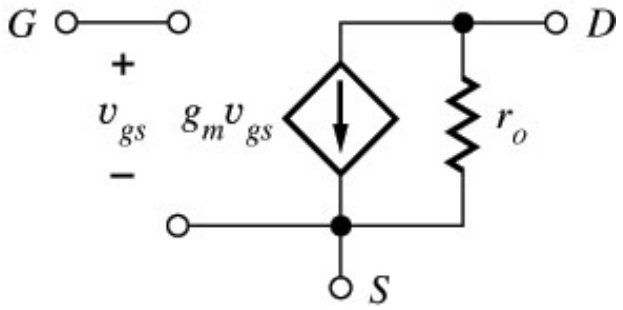
Small-Signal Model for PMOS Transistor





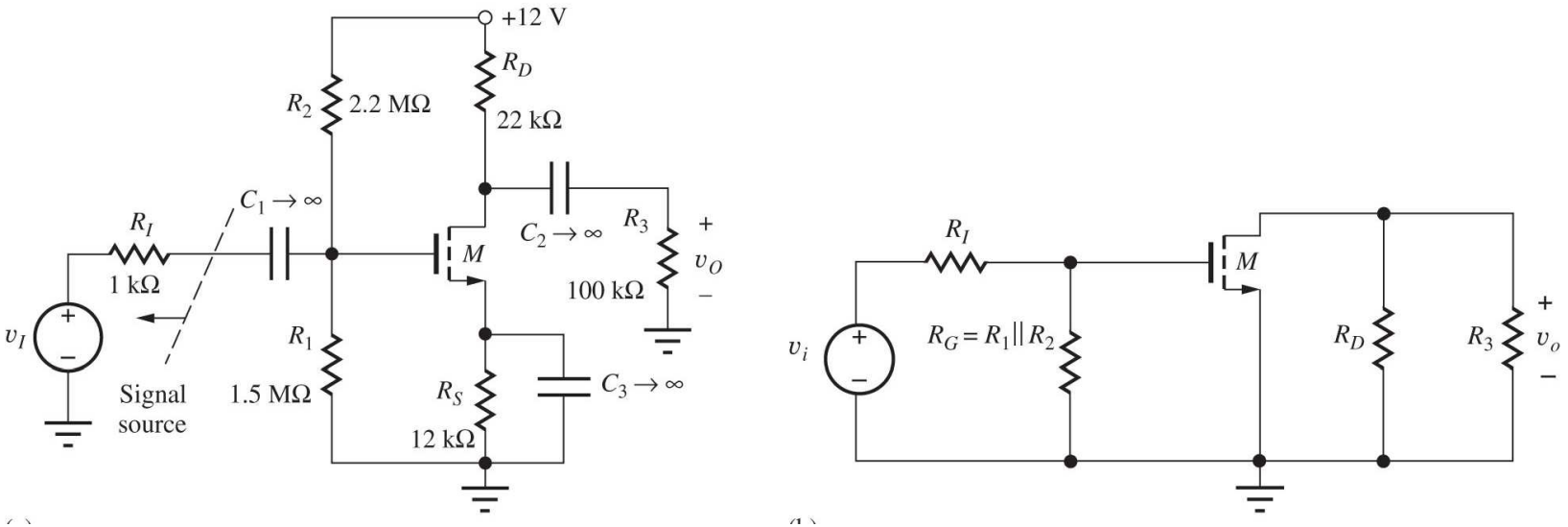
- For a *PMOS* transistor $v_{SG} = V_{GG} - v_{gg}$

  $i_D = I_D - i_d$
- Positive signal voltage v_{gg} reduces source-gate voltage of the PMOS transistor causing decrease in total current exiting the drain, equivalent to an increase in the signal current entering the drain.
- The NMOS and PMOS small-signal models are the same!



Common-Source Amplifiers

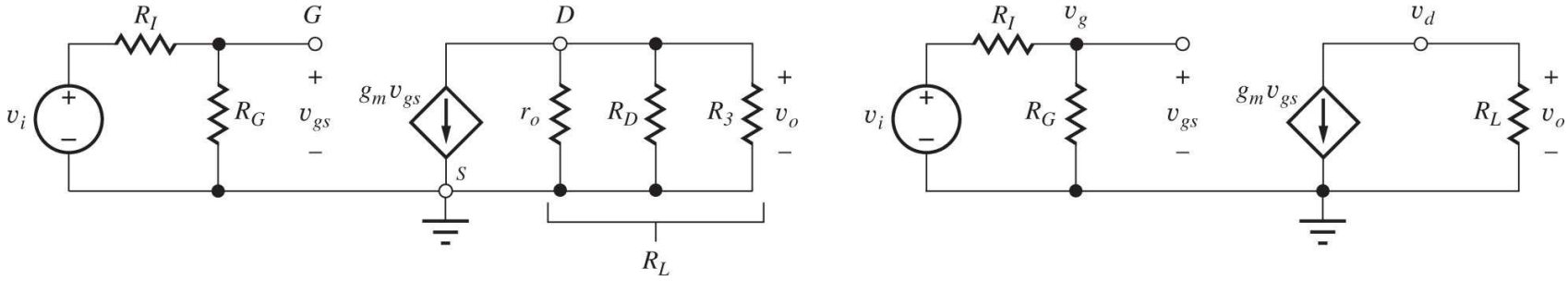
Small-Signal Analysis - ac Equivalent Circuit



- ac equivalent circuit is constructed by assuming that all capacitances have zero impedance at signal frequency and dc voltage sources are ac ground.

Common-Source Amplifiers

Small-Signal Equivalent Circuit

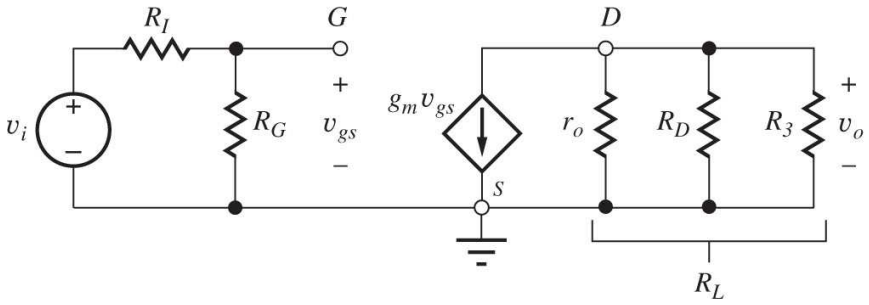


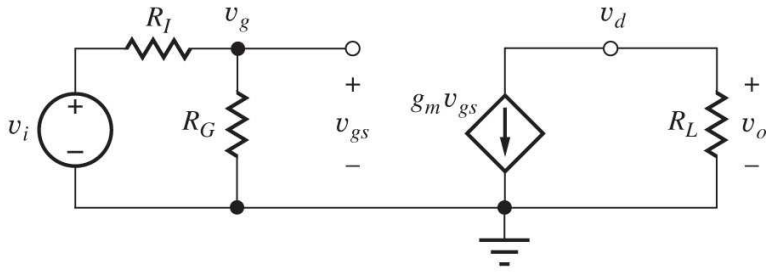
- Input voltage is applied to the gate terminal
- Output signal appears at the drain terminal
- Source is *common* to both input and output signals
  Thus circuit is termed a Common-Source (C-S) Amplifier.
- The terminal gain of the C-S amplifier is the gain from the gate terminal to the drain terminal

$$A_{vt}^{CE} = \frac{v_d}{v_g} = -g_m R_L \qquad R_L = r_o \| R_D \| R_3$$

Common-Source Amplifiers

Input Resistance and Signal-Source Gain





Define R_{iG} as the input resistance looking into the base of the transistor. R_{in} is the resistance presented to v_i.

$$R_{iG} = \frac{v_g}{i_i} = R_G$$

$$R_{in} = R_I + R_G$$

The signal source voltage gain is:

$$A_v^{CS} = \frac{v_o}{v_i} = \frac{v_o}{v_g}\frac{v_g}{v_i} = A_{vt}^{CS}\frac{R_G}{R_I + R_G}$$

$$A_v^{CS} = -g_m R_L\left(\frac{R_G}{R_I + R_G}\right)$$

Common-Source Amplifiers

"Rule of Thumb" Design Estimate

$$A_v^{CS} = -g_m R_L \left(\frac{R_G}{R_I + R_G} \right) \cong A_{vt}^{CS} \qquad A_{vt}^{CS} = -g_m R_L \qquad R_L = r_o \| R_D \| R_3$$

Typically: $r_o >> R_D$ and $R_3 >> R_D$ $\qquad A_v^{CS} \cong -g_m R_D = -\dfrac{I_D R_D}{\left(\dfrac{V_{GS} - V_{TN}}{2} \right)}$

$I_D R_D$ represents the voltage dropped across drain resistor R_D

A typical design point is $\qquad I_D R_D = \dfrac{V_{DD}}{2} \qquad$ with $\qquad V_{GS} - V_{TN} = 1\,V$

$$\therefore A_v^{CS} \cong -V_{DD}$$

Our rule-of-thumb estimate for the C-S amplifier:

the voltage gain equals the power supply voltage.

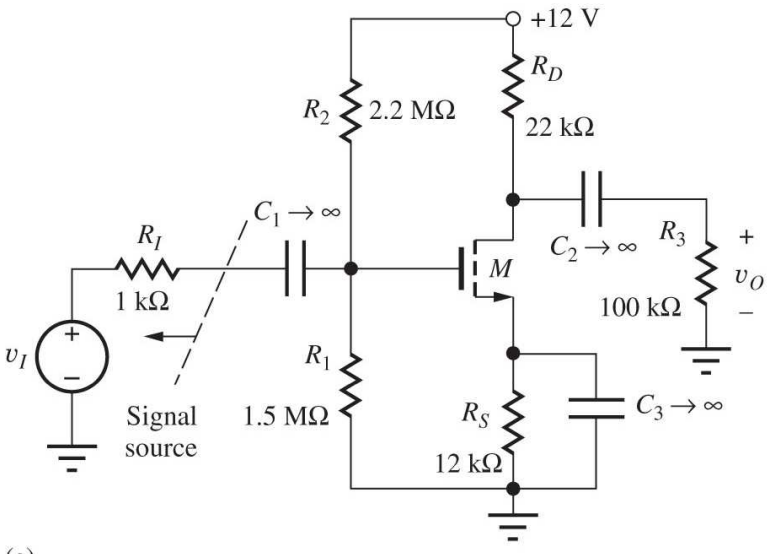
Note that this is 10 times smaller than that for the BJT!

Common-Source Amplifiers

Voltage Gain Example

- **Problem:** Calculate voltage gain, input resistance and maximum input signal level for a common-source amplifier with a specified Q-point
- **Given data:** K_n = 0.50 mA/V^2, V_{TN} = 1 V, $\lambda = 0.0133\text{V}^{-1}$,

  Q-point is (0.241 mA, 3.81 V)
- **Assumptions:** Transistor is in the active region. Signals are low enough to be considered small signals.
- **Analysis:**

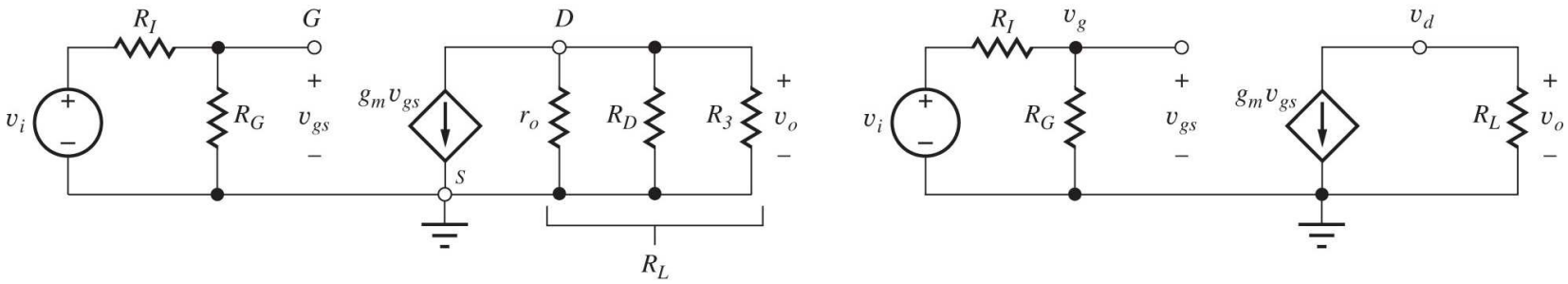


$$g_m = \sqrt{2K_n I_D\left(1+\lambda V_{DS}\right)} = 0.503\ mS \qquad r_o = \frac{\lambda^{-1}+V_{DS}}{I_D} = 328\ k\Omega$$

$$R_G = R_1 \| R_2 = 892\ k\Omega \qquad R_L = r_o \| R_D \| R_3 = 17.1\ k\Omega$$

Common-Source Amplifiers

Voltage Gain Example (cont.)



$g_m = 0.503\ mS \qquad r_o = 328\ k\Omega \qquad R_G = 892\ k\Omega \qquad R_L = 17.1\ k\Omega$

$$A_v^{CS} = -g_m R_L \left(\frac{R_G}{R_I + R_G} \right) = -0.503mS\,(17.1k\Omega)\left(\frac{892k\Omega}{1k\Omega + 892k\Omega} \right) = -8.60\,(0.999) = -8.59$$

$$R_{in} = R_I + R_G = 893\ k\Omega \qquad v_{gs} = v_i \left(\frac{R_G}{R_I + R_G} \right) \rightarrow |v_i| \left(\frac{R_G}{R_I + R_G} \right) \leq 0.2\,(V_{GS} - V_{TN})$$

$$V_{GS} - V_{TN} \cong \sqrt{\frac{2I_D}{K_n}} = 0.982\ V \qquad \therefore |v_i| \leq 0.2\,(0.982V)\left(\frac{893k\Omega}{892k\Omega} \right) = 0.197\ V$$

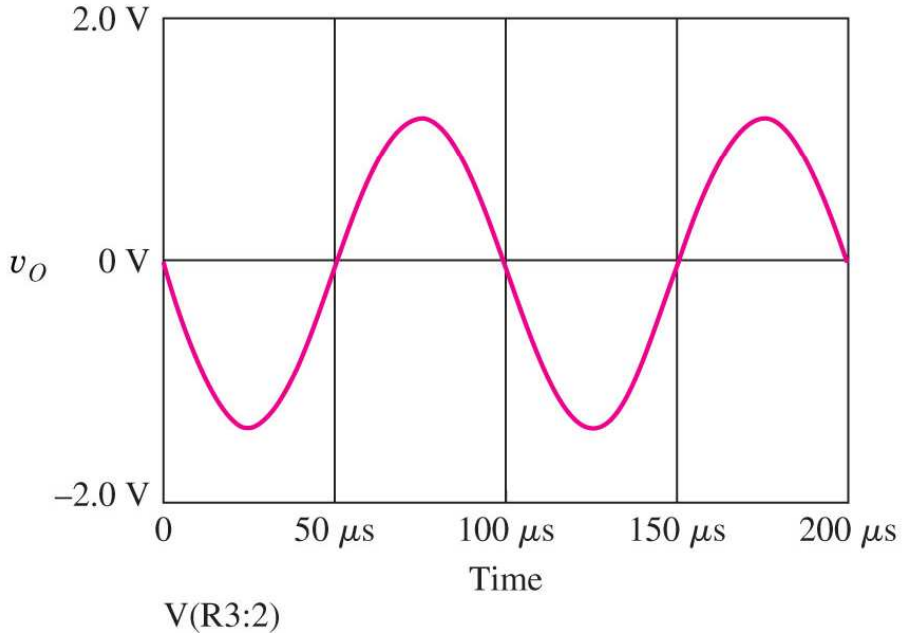
Check the rule-of-thumb estimate: $A_v^{CS} \cong -V_{DD} = -12\ V$ (ballpark estimate)

Common-Source Amplifiers

Voltage Gain Example (cont.)

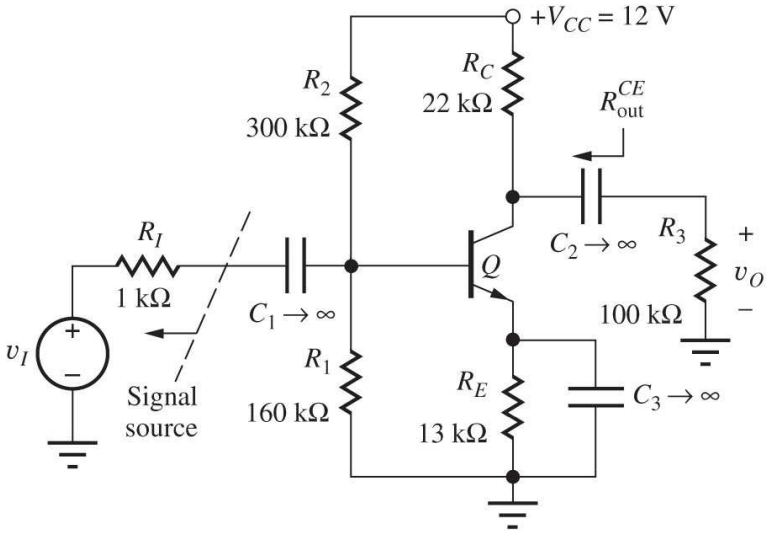
Simulation Results: The graph below presents the output voltage for an input voltage that is a 0.15-V, 10-kHz sine wave. The expected output voltage amplitude is |vo| = 8.59(0.15) = 1.29 V.

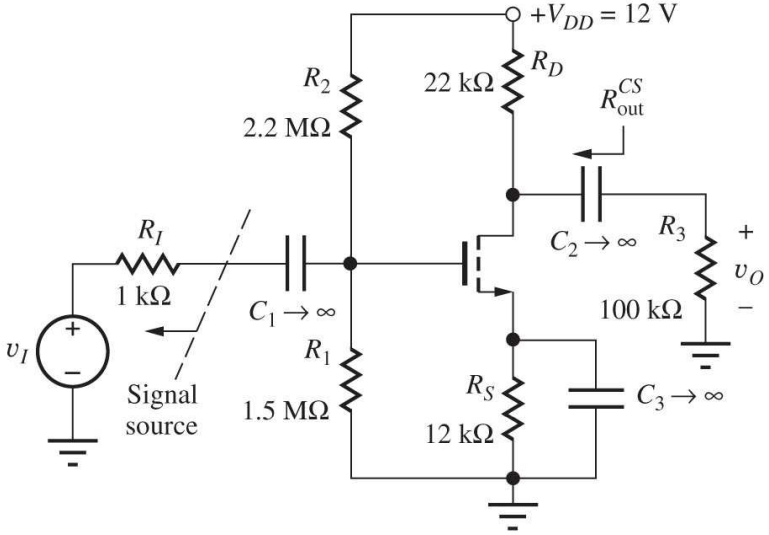
Note that although the sine wave at first looks good, the positive and negative peak amplitudes are different indicating the presence of distortion, and the amplitude is actually larger than expected. The input is near our small-signal limit for linear operation.

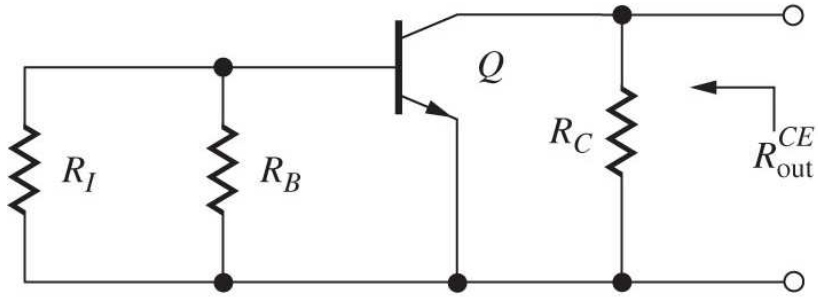


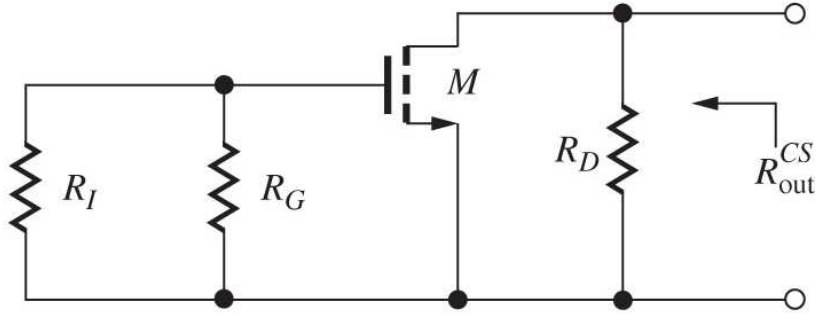
C-E and C-S Amplifiers

Output Resistance



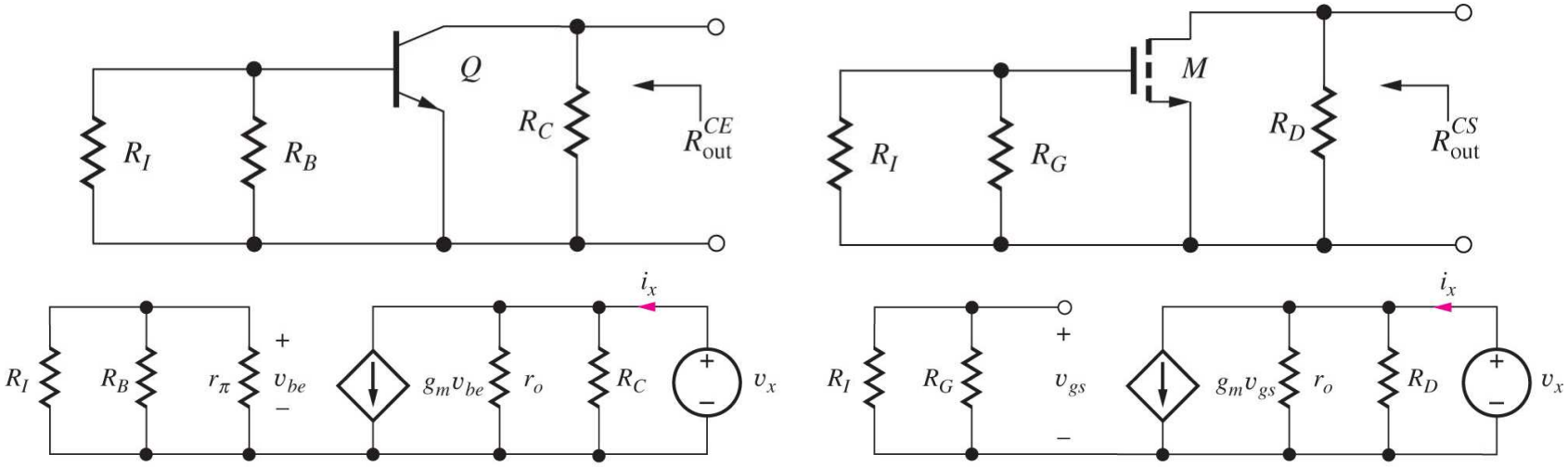






C-E and C-S Amplifiers

Output Resistance (cont.)



Apply test source v_x and find i_x (with $v_i = 0$)

$v_{be} = 0 \rightarrow g_m v_{be} = 0$

$$\therefore R_{out} = \frac{v_x}{i_x} = R_C \| r_o$$

$R_{out} \cong R_C$ for $r_o >> R_C$

$v_{gs} = 0 \rightarrow g_m v_{gs} = 0$

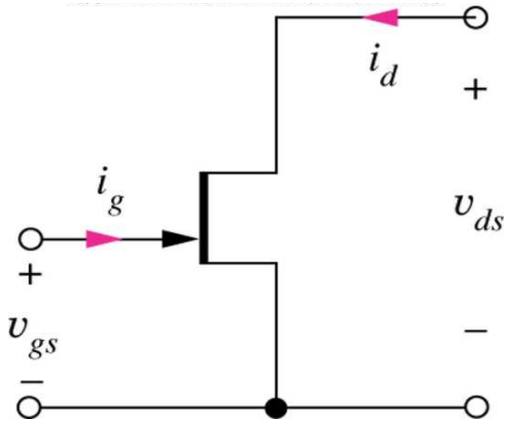
$$\therefore R_{out} = \frac{v_x}{i_x} = R_D \| r_o$$

$R_{out} \cong R_D$ for $r_o >> R_D$

For comparable bias points, output resistances of C-S and C-E amplifiers are similar.

JFET Small-Signal Operation

Small-Signal Model



$$i_D = I_{DSS}\left(1-\frac{v_{GS}}{V_P}\right)^2\left(1+\lambda v_{DS}\right)$$

for $\quad v_{DS} \geq v_{GS} - V_P$

$$i_G = I_{SG}\left[\exp\left(\frac{v_{GS}}{V_T}\right)-1\right]$$

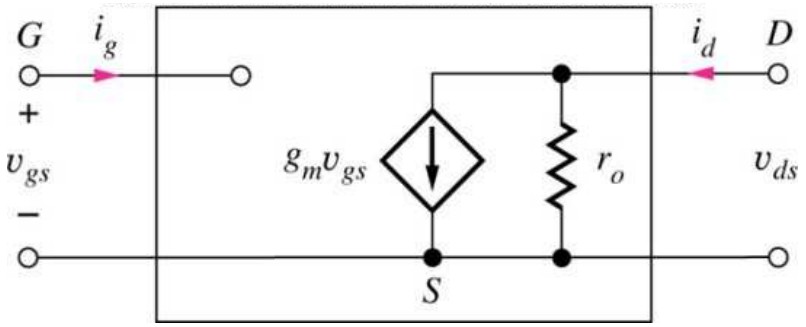
$$g_g = \frac{1}{r_g} = \left.\frac{\partial i_G}{\partial v_{GS}}\right|_{\text{Q-point}} = \frac{I_G + I_{SG}}{V_T} \cong 0 \quad \text{for} \quad I_G = 0$$

$$g_m = \left.\frac{\partial i_D}{\partial v_{GS}}\right|_{\text{Q-point}} = \frac{2I_D}{V_{GS}-V_P} \cong 2\frac{I_{DSS}}{V_P^2}\left(V_{GS}-V_P\right)$$

$$g_o = \frac{1}{r_o} = \left.\frac{\partial i_D}{\partial v_{DS}}\right|_{\text{Q-point}} = \frac{I_D}{\frac{1}{\lambda}+V_{DS}}$$

JFET Small-Signal Operation

Small-Signal Model (cont.)



Since JFET is normally operated with gate junction reverse-biased,

$$I_G = -I_{SG}$$
$$r_g = \infty$$

For small-signal operation, the input signal limit is:

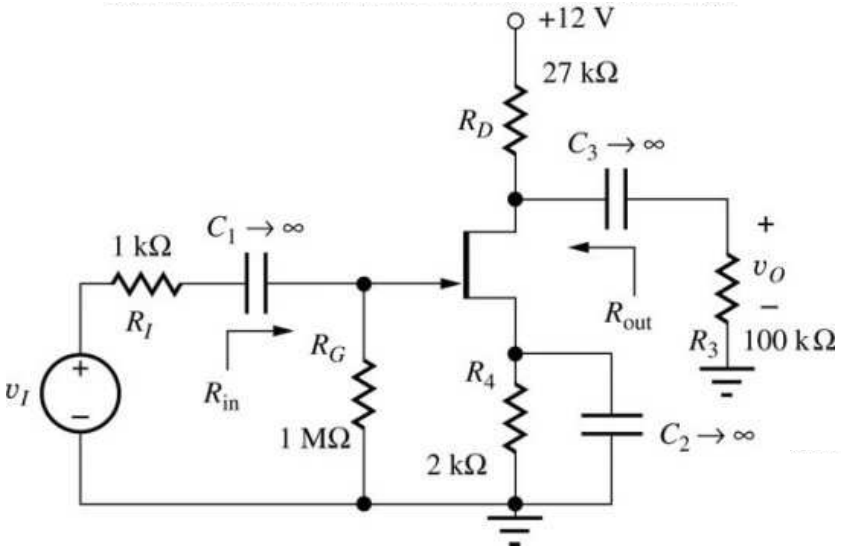
$$v_{gs} < 0.2\left(V_{GS} - V_P\right)$$

The amplification factor is given by:

$$\mu_f = g_m r_o = 2\frac{\frac{1}{\lambda} + V_{DS}}{V_{GS} - V_P} \cong \frac{2}{\lambda |V_P|}\sqrt{\frac{I_{DSS}}{I_D}}$$

Common-Source Amplifiers

JFET Example



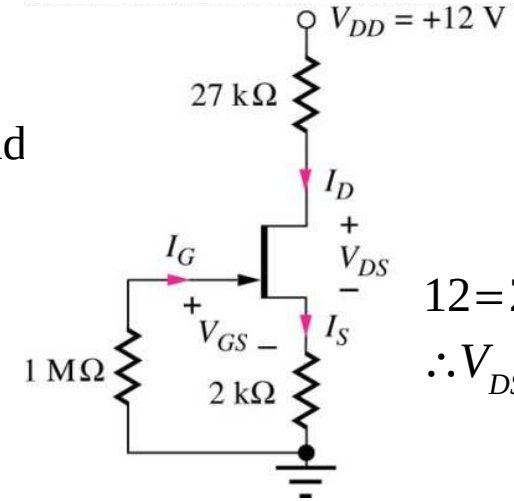
- **Problem:** Find voltage gain, input and output resistances.
- **Given data:** I_{DSS} = 1 mA, V_P = -1V, λ = 0.02 V^{-1}
- **Assumptions:** Pinch-off region of operation.

Analysis: Dc equivalent circuit is constructed. $I_G = 0$, $I_S = I_D$.

$$V_{GS} = -2000 I_D$$

$$V_{GS} = -(2\times10^{3})(1\times10^{-3})\left(1-\frac{V_{GS}}{(-1)}\right)^2$$

Choose V_{GS} less negative than V_P.



$$\therefore V_{GS} = -0.5\ V$$

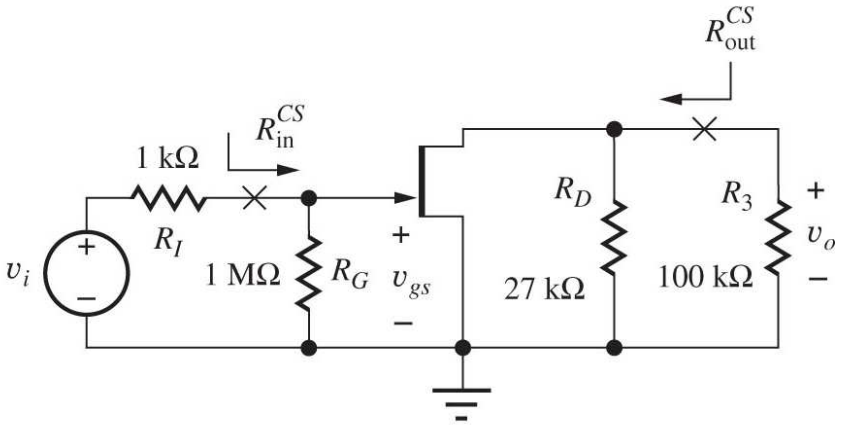
$$I_D = 0.250\ mA$$

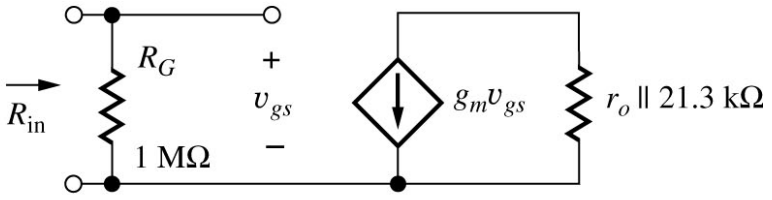
$$12 = 27{,}000 I_D + V_{DS} + 2000 I_S$$

$$\therefore V_{DS} = 4.75 V$$

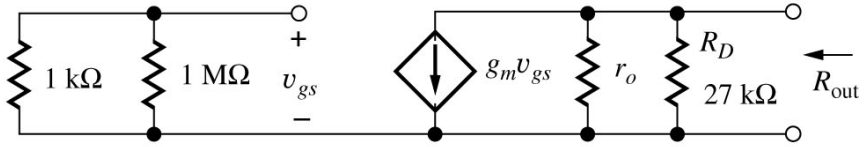
Common-Source Amplifier
JFET Example (cont.)

Next we construct the ac equivalent and simplify it.





$$R_{in} = R_G = 1\ M\Omega$$



$$g_m = \frac{2}{|V_P|}\sqrt{I_{DSS} I_{DS}(1+\lambda V_{DS})} = 1.05\ mS$$

$$r_o = \frac{1+\lambda V_{DS}}{\lambda I_{DS}} = 219\ k\Omega$$

$$R_{out} = r_o \| R_D = 24.0\ k\Omega$$

$$A_v = \frac{v_o}{v_i} = -g_m (R_{out} \| R_3)\left[\frac{R_{in}}{R_I + R_{in}}\right] = -20.3$$

BJT and FET Small-Signal Model Summary

TABLE 13.3
Small-Signal Parameter Comparison

PARAMETER	BIPOLAR TRANSISTOR	MOSFET	JFET
Transconductance g_m	$\frac{I_C}{V_T}$	$\frac{2I_D}{V_{GS}-V_{TN}} \cong \sqrt{2K_n I_D}$	$\frac{2I_D}{V_{GS}-V_P} \cong \frac{2}{\lvert V_P\rvert}$
Input resistance	$r_\pi = \frac{\beta_o}{g_m} = \frac{\beta_o V_T}{I_C}$	∞	∞
Output resistance r_o	$\frac{V_A + V_{CE}}{I_C} \cong \frac{V_A}{I_C}$	$\frac{\frac{1}{\lambda} + V_{DS}}{I_D} \cong \frac{1}{\lambda I_D}$	$\frac{\frac{1}{\lambda} + V_{DS}}{I_D} \cong \frac{1}{\lambda I_D}$
Intrinsic voltage gain μ_f	$\frac{V_A + V_{CE}}{V_T} \cong \frac{V_A}{V_T}$	$\frac{2\left(\frac{1}{\lambda} + V_{DS}\right)}{V_{GS}-V_{TN}} \cong \frac{1}{\lambda}\sqrt{\frac{2K_n}{I_D}}$	$\frac{2\left(\frac{1}{\lambda} + V_{DS}\right)}{V_{GS}-V_P} \cong \frac{2}{\lambda\lvert V_P\rvert}\sqrt{\frac{I_{DSS}}{I_D}}$
Small-signal requirement	$v_{be} \le 0.005$ V	$v_{gs} \le 0.2(V_{GS}-V_{TN})$	$v_{gs} \le 0.2(V_{GS}-V_P)$

dc i-v active region expressions for use with Table 13.3:

BJT: $I_C = I_S\left[\exp\left(\frac{V_{BE}}{V_T}\right) - 1\right]\left[1 + \frac{V_{CE}}{V_A}\right] \qquad V_T = \frac{kT}{q}$

MOSFET: $I_D = \frac{K_n}{2}(V_{GS}-V_{TN})^2(1+\lambda V_{DS}) \qquad K_n = \mu_n C_{ox}\frac{W}{L}$

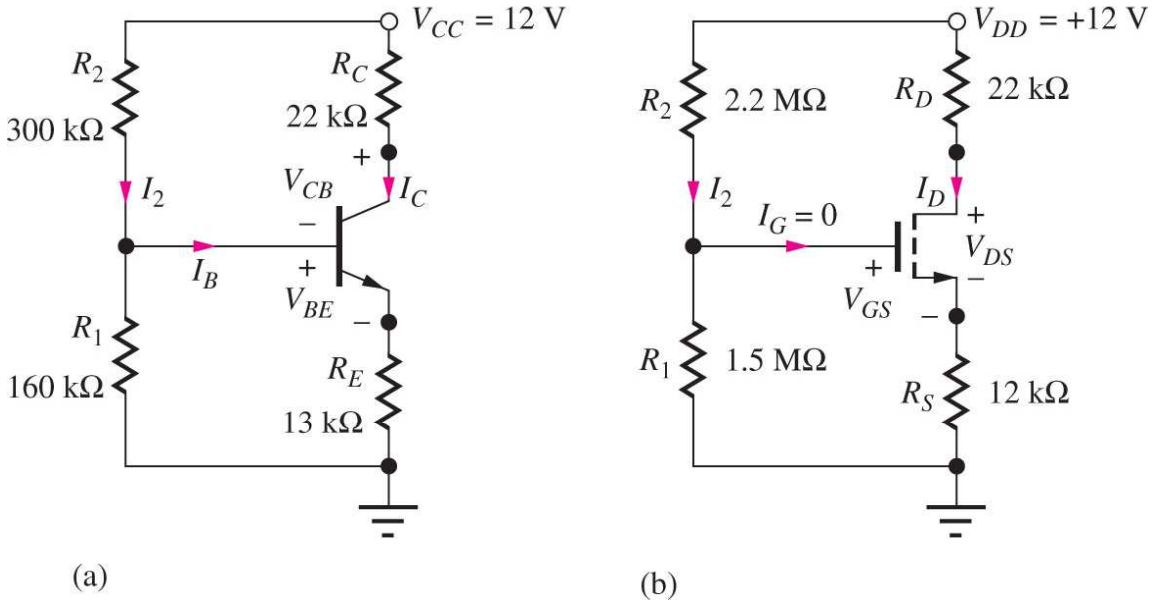
JFET: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2(1+\lambda V_{DS})$

Common-Emitter/Common-Source Amplifiers Summary

	COMMON-EMITTER AMPLIFIER	COMMON-SOURCE AMPLIFIERS
Terminal gain A_{vt}	$-g_m R_L$	$-g_m R_L$
Rule-of-thumb estimate for $g_m R_L$	$-10V_{CC}$	$-V_{DD}$
Voltage gain A_v	$A_v = \frac{\mathbf{v}_o}{\mathbf{v}_i} = -g_m(R_{\text{out}} \| R_3)\left(\frac{R_{\text{in}}}{R_I + R_{\text{in}}}\right)$	
Input resistance R_{in}	$R_B \| r_\pi$	R_G
Output resistance R_{out}	$R_C \| r_o \cong R_C$	$R_D \| r_o \cong R_D$
Input signal phase	0.005 V	$0.2(V_{GS} - V_{TN})$ or $0.2(V_{GS} - V_P)$

Amplifier Power Dissipation

Static power dissipation in amplifiers is found from their dc equivalent circuits.



(a) Total power dissipated in the C-B and E-B junctions is:

$$P_D = V_{CE} I_C + V_{BE} I_B \quad \text{where} \quad V_{CE} = V_{CB} + V_{BE}$$

Total power supplied is:

$$P_S = V_{CC} I_C + V_{EE} I_E$$

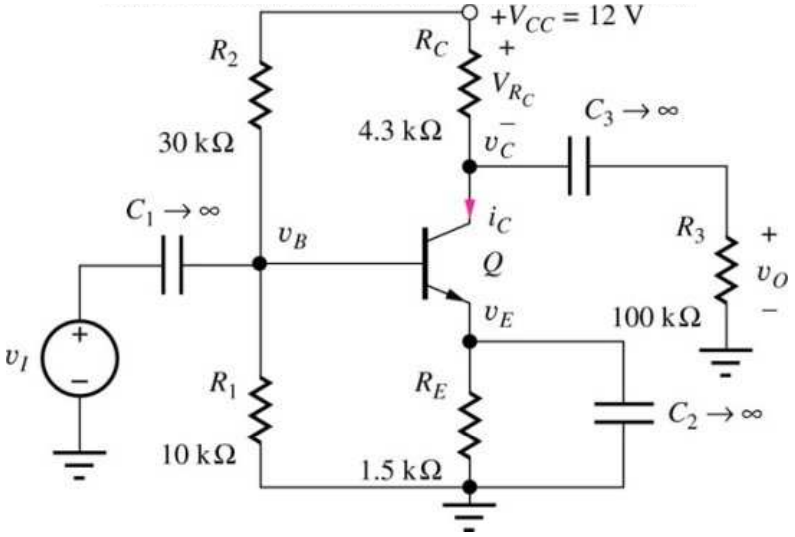
(b) Total power dissipated in the transistor is:

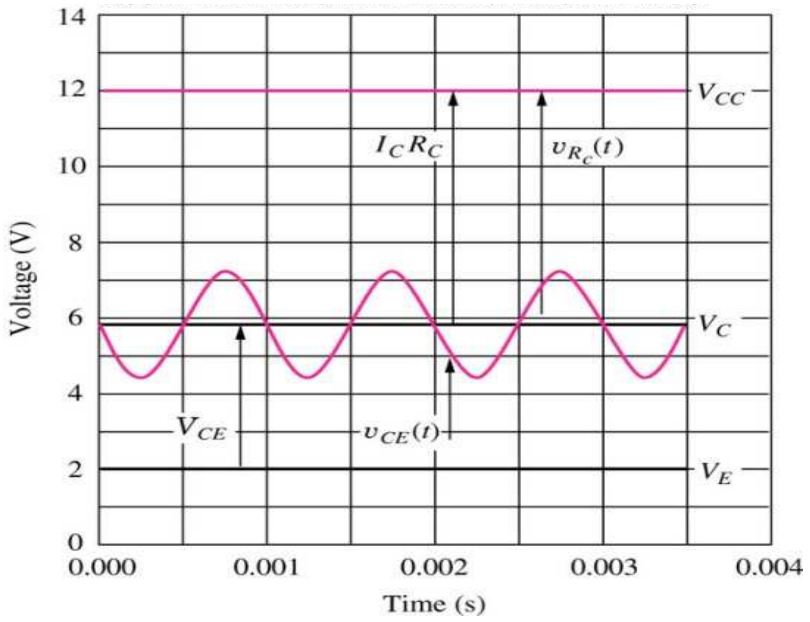
$$P_D = V_{DS} I_D + V_{GS} I_G = V_{DS} I_D$$

Total power supplied is:

$$P_S = V_{DD} I_D + V_{DD}^2/(R_1+R_2)$$

Amplifier Signal Range





$v_{CE} = V_{CE} - V_m \sin \omega t$ where V_m is the output signal. Active region operation requires $v_{CE} \geq v_{BE}$ So: $V_m \leq V_{CE} - V_{BE}$

Also: $v_{R_c}(t) = I_C R_C - V_m \sin \omega t \geq 0$

$\therefore V_m \leq \min\left[I_C R_C, (V_{CE} - V_{BE}) \right]$

Similarly for MOSFETs and JFETs:

$$V_M \leq \min\left[I_D R_D, (V_{DS} - (V_{GS} - V_{TN})) \right]$$

$$V_M \leq \min\left[I_D R_D, (V_{DS} - (V_{GS} - V_P)) \right]$$

End of Chapter 13