Chapter 5
Bipolar Junction Transistors

Microelectronic Circuit Design
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Chapter Goals

• Explore physical structure of bipolar transistor
• Understand bipolar transistor action and importance of carrier transport across base region
• Study terminal characteristics of BJT.
• Explore differences between npn and pnp transistors.
• Develop the Transport Model for the bipolar device.
• Define four operation regions of BJT.
• Explore model simplifications for each operation region.
• Understand origin and modeling of the Early effect.
• Present SPICE model for bipolar transistor.
• Provide examples of worst-case and Monte Carlo analysis of bias circuits.
Bipolar Transistor
Physical Structure

- Consists of 3 alternating layers of $n$- and $p$-type semiconductor called **emitter** ($E$), **base** ($B$) and **collector** ($C$).
- Majority of current enters the collector, crosses the base region and exits through the emitter. A small current also enters the base terminal, crosses the base-emitter junction and exits through the emitter.
- Carrier transport in the the active base region directly beneath the heavily doped ($n^+$) emitter dominates the $i-v$ characteristics of BJT.
Transport Model for the \textit{n}pn Transistor

- Base-emitter voltage $v_{BE}$ and base-collector voltage $v_{BC}$ determine currents in transistor and are said to be positive when they forward-bias their respective \textit{pn} junctions.
- The terminal currents are collector current ($i_C$), base current ($i_B$) and emitter current ($i_E$).
- Primary difference between BJT and FET is that $i_B$ is significant while $i_G = 0$.

- Narrow width of the base region causes coupling between the two back-to-back \textit{pn} junctions.
- Emitter injects electrons into base region, almost all travel across narrow base and are removed by collector.
**nnp Transistor**

**Forward Characteristics**

Base current $i_B$ is given by

$$i_B = \frac{i_F}{\beta_F} = \frac{I_S}{\beta_F} \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \quad 20 \leq \beta_F \leq 500$$

$\beta_F$ is the forward common-emitter current gain

Emitter current $i_E$ is

$$i_E = i_C + i_B = \frac{I_S}{\alpha_F} \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] \quad \alpha_F = \frac{\beta_F}{\beta_F + 1}$$

$0.95 \leq \alpha_F \leq 1$

$\alpha_F$ is the forward common-base current gain

In this forward-active region of operation

$$\beta_F = \frac{i_C}{i_B} \quad \alpha_F = \frac{i_C}{i_E}$$

Forward transport current is

$$i_C = i_F = I_S \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right]$$

$I_S$ is the BJT saturation current

$$10^{-18} \ A \leq I_S \leq 10^{-9} \ A$$

$V_T = kT/q$ =0.025 V at room temperature

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**nnp Transistor**  
**Reverse Characteristics**

$\beta_R$ is the reverse common-emitter current gain  

$$0 \leq \beta_R \leq 0.95$$

Base currents in forward and reverse modes are different due to asymmetric doping levels in emitter and collector regions.

Collector current $i_C$ is given by

$$i_C = i_B - i_E = \frac{I_S}{\alpha_R} \left[ \exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right]$$

$\alpha_R$ is the reverse common-base current gain

$$\alpha_R = \frac{\beta_R}{\beta_R + 1} \quad 0 \leq \alpha_R \leq 0.95$$

Emitter current $i_E$ is

$$i_E = -i_R = I_S \left[ \exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right]$$

Base current $i_B$ is given by

$$i_B = \frac{i_R}{\beta_R} = \frac{I_S}{\beta_R} \left[ \exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right]$$
npn Transistor
Complete Transport Model - Valid for Any Bias

\[ i_C = I_S \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - \exp \left( \frac{v_{BC}}{V_T} \right) \right] - \frac{I_S}{\beta_R} \left[ \exp \left( \frac{v_{BC}}{V_T} \right) - 1 \right] \]

\[ i_E = I_S \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - \exp \left( \frac{v_{BC}}{V_T} \right) \right] + \frac{I_S}{\beta_F} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \]

\[ i_B = \frac{I_S}{\beta_F} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] - \frac{I_S}{\beta_R} \left[ \exp \left( \frac{v_{BC}}{V_T} \right) - 1 \right] \]

First term in both emitter and collector current expressions gives current transported completely across base region.

Symmetry exists between base-emitter and base-collector voltages in establishing dominant current in bipolar transistor.
Transport Model Calculations

Example

- **Problem:** Find terminal voltages and currents.
- **Given data:** $V_{BB} = 0.75 \text{ V}$, $V_{CC} = 5.0 \text{ V}$, $I_S = 10^{-16} \text{ A}$, $\beta_F = 50$, $\beta_R = 1$
- **Assumptions:** Room temperature operation, $V_T = 25.0 \text{ mV}$.
- **Analysis:** $V_{BE} = 0.75 \text{ V}$, $V_{BC} = V_{BB} - V_{CC} = 0.75 \text{ V} - 5.00 \text{ V} = -4.25 \text{ V}$

\[
I_C = 10^{-16} \left[ \exp \left( \frac{0.75}{0.025} \right) - \exp \left( \frac{-4.25}{0.025} \right) \right] - 10^{-16} \left[ \exp \left( \frac{-4.25}{0.025} \right) - 1 \right] = 1.07 \text{ mA}
\]

\[
I_E = 10^{-16} \left[ \exp \left( \frac{0.75}{0.025} \right) - \exp \left( \frac{-4.25}{0.025} \right) \right] + \frac{10^{-16}}{50} \left[ \exp \left( \frac{0.75}{0.025} \right) - 1 \right] = 1.09 \text{ mA}
\]

\[
I_B = \frac{10^{-16}}{50} \left[ \exp \left( \frac{0.75}{0.025} \right) - 1 \right] - \frac{10^{-16}}{1} \left[ \exp \left( \frac{-4.25}{0.025} \right) - 1 \right] = 21.4 \text{ µA}
\]

$\beta_F = \frac{I_C}{I_B} = 50.0$

$\alpha_F = \frac{I_C}{I_E} = 0.982$
**pnp Transistor Structure**

- Voltages $v_{EB}$ and $v_{CB}$ are positive when they forward bias their respective $pn$ junctions.
- Collector current and base current exit transistor terminals and emitter current enters the device.
**pnp Transistor**

**Forward Characteristics**

Base current $i_B$ is given by

$$i_B = \frac{i_F}{\beta_F} = \frac{I_S}{\beta_F} \left[ \exp \left( \frac{v_{EB}}{V_T} \right) - 1 \right]$$

Emitter current $i_E$ is given by

$$i_E = i_C + i_B = I_S \left[ 1 + \frac{1}{\beta_F} \right] \left[ \exp \left( \frac{v_{EB}}{V_T} \right) - 1 \right]$$

Collector current $i_C$ equals the forward transport current is

$$i_C = i_F = I_S \left[ \exp \left( \frac{v_{EB}}{V_T} \right) - 1 \right]$$
**pnp Transistor**

**Reverse Characteristics**

Base current $i_B$ is given by

$$i_B = \frac{i_E}{\beta_R} = \frac{I_S}{\beta_R} \exp\left(\frac{v_{CB}}{V_T}\right) - 1$$

Collector current $i_C$ is given by

$$i_C = i_B - i_E = I_S \left(\frac{1}{\beta_R} + 1\right) \exp\left(\frac{v_{CB}}{V_T}\right) - 1$$

$$(i_C = \frac{I_S}{\alpha_R} \exp\left(\frac{v_{CB}}{V_T}\right) - 1) = \frac{i_E}{\alpha_R}$$

Emitter current $i_E$ is the negative of the reverse transport current is

$$i_E = -i_R = -I_S \left[\exp\left(\frac{v_{CB}}{V_T}\right) - 1\right]$$
**pnp Transistor**

Complete Transport Model Equations for Any Bias

\[
i_C = I_S \left[ \exp\left(\frac{v_{EB}}{V_T}\right) - \exp\left(\frac{v_{CB}}{V_T}\right) \right] - \frac{I_S}{\beta_R} \left[ \exp\left(\frac{v_{CB}}{V_T}\right) - 1 \right]
\]

\[
i_E = I_S \left[ \exp\left(\frac{v_{EB}}{V_T}\right) - \exp\left(\frac{v_{CB}}{V_T}\right) \right] + \frac{I_S}{\beta_F} \left[ \exp\left(\frac{v_{EB}}{V_T}\right) - 1 \right]
\]

\[
i_B = \frac{I_S}{\beta_F} \left[ \exp\left(\frac{v_{EB}}{V_T}\right) - 1 \right] - \frac{I_S}{\beta_R} \left[ \exp\left(\frac{v_{CB}}{V_T}\right) - 1 \right]
\]

First term in both emitter and collector current expressions gives current transported completely across base region.

Symmetry exists between base-emitter and base-collector voltages in establishing dominant current in bipolar transistor.
In npn transistor (expressions are analogous for pnp transistors), the total current traversing base is modeled by a current source given by:

\[ i_T = i_F - I_R = I_S \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - \exp\left(\frac{v_{BC}}{V_T}\right) \right] \]

Diode currents correspond directly to the two components of base current.

\[ i_B = \frac{I_S}{\beta_F} \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right] - \frac{I_S}{\beta_R} \left[ \exp\left(\frac{v_{BC}}{V_T}\right) - 1 \right] \]
## Operation Regions of Bipolar Transistors

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Binary Logic States
Characteristics of Bipolar Transistors
Common-Emitter Output Characteristics

For $i_B = 0$, the transistor is cutoff. If $i_B > 0$, $i_C$ also increases.

For $v_{CE} > v_{BE}$, npn transistor is in forward-active region, $i_C = \beta_F i_B$ is nearly independent of $v_{CE}$.
For $v_{CE} < v_{BE}$, transistor is in saturation.

For $v_{CE} < 0$, roles of collector and emitter reverse.
For $v_{CB} > 0$, npn transistor is in the forward-active region. $i_C \approx i_E$ is nearly independent of and $v_{CE}$.

For $v_{CB} < 0$, base-collector diode becomes forward-biased and $i_C$ grows exponentially (in negative direction) as base-collector diode begins to conduct.
i-ν Characteristics of Bipolar Transistors

Common-Emitter Transfer Characteristic

Defines relation between collector current and base-emitter voltage of transistor.

Almost identical to transfer characteristic of a \(pn\) junction diode

Setting \(v_{BC} = 0\) in the collector-current expression yields

\[
i_C = I_S \left[ \exp\left(\frac{v_{BE}}{V_T}\right) - 1 \right]
\]

Collector current expression has the same form as that of the diode equation.
Simplified Cutoff Region Model

If we assume that

\[ v_{BE} \leq -4 \frac{kT}{q} \quad \text{and} \quad v_{BC} \leq -4 \frac{kT}{q} \]

where \(-4kT/q = -0.1 \text{ V}\), then the transport model terminal current equations simplify to

\[ i_C = \frac{I_S}{\beta_R} \quad \text{and} \quad i_E = -\frac{I_S}{\beta_F} \]

\[ i_B = -\frac{I_S}{\beta_F} - \frac{I_S}{\beta_F} \]

In the cutoff region, both junctions are reverse-biased; the transistor is said to be in off state

\[ v_{BE} < 0, \; v_{BC} < 0 \]
Simplified Cutoff Region Model

Example

- **Problem:** Estimate terminal currents using the transport model
- **Given data:** $I_S = 10^{-16}$ A, $\alpha_F = 0.95$, $\alpha_R = 0.25$, $V_{BE} = 0$ V, $V_{BC} = -5$ V
- **Assumptions:** Simplified transport model assumptions
- **Analysis:** From given voltages, we know that transistor is in cutoff.

\[
I_C = I_S \left(1 + \frac{1}{\beta_R}\right) = \frac{I_S}{\alpha_R} = 4 \times 10^{-16} \text{ A}
\]

\[
I_E = I_S = 10^{-16} \text{ A}
\]

\[
I_B = -\frac{I_S}{\beta_R} = -3 \times 10^{-16} \text{ A}
\]

For practical purposes, all three currents are essentially zero.
Simplified Forward-Active Region Model

In forward-active region, the emitter-base junction is forward-biased and the collector-base junction is reverse-biased. $v_{BE} > 0$, $v_{BC} < 0$. If we assume

$$v_{BE} \geq -\frac{4kT}{q} \quad \text{and} \quad v_{BC} \leq -\frac{4kT}{q}$$

then the transport model terminal current equations simplify to

$$i_C \equiv I_S \exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_R}$$

$$i_E \equiv I_S \exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_F} = \frac{I_S}{\alpha_F} \exp\left(\frac{v_{BE}}{V_T}\right)$$

$$i_B \equiv \frac{I_S}{\beta_F} \exp\left(\frac{v_{BE}}{V_T}\right) + \frac{I_S}{\beta_R} \equiv \frac{I_S}{\beta_F} \exp\left(\frac{v_{BE}}{V_T}\right)$$

$$i_C = \alpha_F I_E$$

$$i_C = \beta_F I_B$$

BJT is often considered a current-controlled device, though fundamental forward-active behavior suggests a voltage-controlled current source.
Simplified Forward-Active Region Model

Example 1

• **Problem:** Estimate transistor terminal currents and base-emitter voltage
• **Given data:** $I_S = 10^{-16}$ A, $\alpha_F = 0.95$, $V_{BC} = V_B - V_C = -5$ V, $I_E = 100$ $\mu$A
• **Assumptions:** Simplified transport model assumptions, room temperature operation, $V_T = 25.0$ mV
• **Analysis:** Current source forward-biases base-emitter diode, $V_{BE} > 0$, $V_{BC} < 0$, we know that transistor is in forward-active operation region.

\[
I_C = \alpha_F I_E = 0.95(100\mu A) = 95\ \mu A
\]
\[
\beta_F = \frac{\alpha_F}{1 - \alpha_F} = \frac{0.95}{1 - 0.95} = 19
\]
\[
I_B = \frac{I_E}{\beta_F + 1} = \frac{100\mu A}{20} = 5\ \mu A
\]
\[
V_{BE} = V_T \ln \left( \frac{\alpha_F I_E}{I_S} \right) = 0.689\ V
\]
**Simplified Forward-Active Region Model**

**Example 2**

- **Problem:** Estimate terminal currents, base-emitter and base-collector voltages for the transistor in the given circuit.
- **Given data:** $I_S = 10^{-16}$ A, $\alpha_F = 0.95$, $V_C = +5$ V, $I_B = 100$ $\mu$A
- **Assumptions:** Simplified transport model assumptions, room temperature operation, $V_T = 25.0$ mV
- **Analysis:** Current source causes base current to forward-bias base-emitter diode, $V_{BE} > 0$, $V_{BC} < 0$, we know that transistor is in forward-active operation region.

\[
\beta_F = \frac{\alpha_F}{1 - \alpha_F} = \frac{0.95}{1 - 0.95} = 19
\]

\[
I_C = \beta_F I_B = 19(100\mu A) = 1.90 \text{ mA}
\]

\[
I_E = (\beta_F + 1) I_B = 20(100\mu A) = 2.00 \text{ mA}
\]

\[
V_{BE} = V_T \ln \left(1 + \frac{I_C}{I_S}\right) = 0.025V \ln \left(1 + \frac{1.9mA}{0.1fA}\right) = 0.764 \text{ V}
\]

\[
V_{BC} = V_B - V_C = V_{BE} - V_C = 0.764 - 5 = -4.24 \text{ V}
\]
Simplified Circuit Model
Forward-Active Region

- Current in base-emitter diode is amplified by common-emitter current gain $\beta_F$ and appears at collector; base and collector currents are exponentially related to base-emitter voltage.
- Base-emitter diode is replaced by constant voltage drop model ($V_{BE} = 0.7$ V) since it is forward-biased in forward-active region.
- dc base and emitter voltages differ by 0.7-V diode voltage drop in forward-active region.
Example 3

- **Problem:** Find transistor Q-point
- **Given data:** \( \beta_F = 50, \beta_R = 1 \)
- **Assumptions:** Forward-active region of operation, \( V_{BE} = 0.7 \text{ V} \)
- **Analysis:**

\[
V_{BE} + 8200I_E - V_{EE} = 0
\]

\[
\therefore I_E = \frac{9 - 0.7}{8200} = 1.01 \text{ mA}
\]

\[
I_B = \frac{I_E}{\beta_F + 1} = \frac{1.01\text{mA}}{51} = 19.8 \mu\text{A}
\]

\[
I_C = \beta_F I_B = 50(19.8\mu\text{A}) = 0.990 \text{ mA}
\]

\[
V_{CE} = V_{CC} - I_C R_C - ( -V_{BE} )
\]

\[
V_{CE} = 9 - 0.99\text{mA}(4.3K) + 0.7 = 5.44 \text{ V}
\]

Forward-active region is correct.
In reverse-active region, base-collector diode is forward-biased and base-emitter diode is reverse-biased.

Simplified equations are:

\[ i_E = -I_S \exp \left( \frac{v_{BC}}{V_T} \right) \]
\[ i_C = -\frac{I_S}{\alpha_R} \exp \left( \frac{v_{BC}}{V_T} \right) \]
\[ i_B = \frac{I_S}{B_R} \exp \left( \frac{v_{BC}}{V_T} \right) \]

\[ i_E = \alpha_R i_C \]
\[ i_E = -\beta_R i_B \]

\[ -i_C = (\beta_R + 1) i_B \]
Simplified Reverse-Active Region Model

Example

• **Problem:** Find transistor Q-point
• **Given data:** $\beta_F = 50$, $\beta_R = 1$ $V_{BE} = V_B - V_E = -9$ V. Combination of $R$ and the voltage source forward biases base-collector junction.
• **Assumptions:** Reverse-active region of operation, $V_{BC} = 0.7$ V
• **Analysis:**

\[ -I_C = \frac{-0.7V - (-9V)}{8200\Omega} = 1.01 \text{ mA} \]

\[ I_B = \frac{-I_C}{\beta_R + 1} = \frac{1.01mA}{2} = 0.505 \text{ mA} \]

\[ -I_E = \beta_R I_B = 0.505 \text{ mA} \]

Current directions are consistent with reverse-active region operation.
Simplified Circuit Model

Saturation Region

- In the saturation region, both junctions are forward-biased, and the transistor operates with a small voltage between collector and emitter. $v_{CESAT}$ is the saturation voltage for the npn BJT.

$$I_C = I_s \exp\left(\frac{V_{BE}}{V_T}\right) - I_s \frac{V_{BC}}{\alpha_R} \exp\left(\frac{V_{BC}}{V_T}\right) \quad I_B = I_s \frac{V_{BE}}{\beta_F} \exp\left(\frac{V_{BE}}{V_T}\right) + I_s \frac{V_{BC}}{\beta_R} \exp\left(\frac{V_{BC}}{V_T}\right)$$

$$V_{CESAT} = V_{BE} - V_{BC} = V_T \ln \left[ \frac{1 + I_C}{\alpha_R} \right] \left[ 1 + \frac{I_C}{(\beta_R + 1)I_B} \right] \quad \text{for} \quad I_B \geq \frac{I_C}{\beta_F}$$

No simplified expressions exist for terminal currents other than $i_C + i_B = i_E$. 
Non Ideal BJT Behavior

Junction Breakdown Voltages

- If reverse voltage across either of the two $pn$ junctions in the transistor is too large, the corresponding diode will break down.
- The emitter is the most heavily-doped region, and the collector is the most lightly doped region.
- Due to doping differences, the base-emitter diode has a relatively low breakdown voltage (3 to 10 V). The collector-base diode can be designed to break down at much larger voltages.
- Transistors must be selected in accordance with possible reverse voltages in circuit.
Non Ideal BJT Behavior

Minority Carrier Transport in the Base Region

• BJT current dominated by diffusion of minority carriers (electrons in npn and holes in pnp transistors) across base region.

• Base current consists of hole injection back into emitter and collector and a small additional current to replenish holes lost to recombination with electrons in base.

• Minority carrier concentrations at the two ends of the base region are:

\[ n(0) = n_{bo} \exp\left(\frac{V_{BE}}{V_T}\right) \]  
\[ n(W_B) = n_{bo} \exp\left(\frac{V_{BC}}{V_T}\right) \]

\( n_{bo} \) is equilibrium electron density in the p-type base region.

\[ n_{bo} \] is equilibrium electron density in the p-type base region.
Minority Carrier Transport in the Base Region (cont.)

- For narrow base devices, minority carrier density decreases linearly across the base, and the diffusion current in the base is:

\[ I_S = qAD_n \frac{n_{bo}}{W_B} = \frac{qAD_n}{W_B} \frac{n_i^2}{N_{AB}} \]

\( N_{AB} \) = doping concentration in base
\( n_i^2 \) = intrinsic carrier concentration (10\(^{10}\)/cm\(^3\))
\( n_{bo} = n_i^2 / N_{AB} \)

- Saturation current for the \( pnp \) transistor is

\[ I_S = qAD_p \frac{p_{bo}}{W_B} = \frac{qAD_p}{W_B} \frac{n_i^2}{N_{DB}} \]

- Due to higher mobility of electrons than holes, the \( npn \) transistor conducts higher current than the \( pnp \) for a given set of applied voltages.
Non Ideal BJT Behavior

Base Transit Time

Forward transit time $\tau_F$ is the time constant associated with storing minority-carrier charge $Q$ required to establish career gradient in base region.

$$Q = qA n_{bo} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right] \frac{W_B}{2}$$

$$i_T = \frac{qAD_n}{W_B} n_{bo} \left[ \exp \left( \frac{v_{BE}}{V_T} \right) - 1 \right]$$

$$\tau_F = \frac{Q}{i_T} = \frac{W_B^2}{2D_n} = \frac{W_B^2}{2\mu_n V_T}$$

Transit time places upper limit on useful operating frequency of transistor.
Non Ideal BJT Behavior

**Diffusion Capacitance**

- For $v_{BE}$ and hence $i_C$ to change, charge stored in base region must also change.
- Diffusion capacitance in parallel with forward-biased base-emitter diode models the change in charge with $v_{BE}$.

\[
C_D = \left. \frac{dQ}{dv_{BE}} \right|_{Q_{-pt}} = \frac{1}{V_T} q A n_{bo} W_B \exp \left( \frac{V_{BE}}{V_T} \right) = \frac{I_T}{V_T} \tau_F
\]

- Since transport current normally represents collector current in forward-active region,

\[
C_D = \frac{I_C}{V_T} \tau_F
\]
\( \beta \) Cutoff-Frequency, Transconductance and Transit Time

- Forward-biased diffusion and reverse-biased \( pn \) junction capacitances of the BJT cause current gain to be frequency-dependent.
- Unity gain frequency \( f_T \) is frequency at which the current gain is unity

\[
\beta(f) = \frac{\beta_F}{\sqrt{1 + \left(\frac{f}{f_B}\right)^2}} \quad \text{where} \quad f_B = \frac{f_T}{\beta_F} \quad \text{is the } \beta \text{ cutoff-frequency}
\]

- Transconductance is defined by:

\[
g_m = \left. \frac{di_C}{dv_{BE}} \right|_{Q-P_t} = \frac{d}{dv_{BE}} \left[ I_S \exp\left(\frac{v_{BE}}{V_T}\right) \right]_{Q-P_t} = \frac{I_C}{V_T}
\]

- Transit time is given by:

\[
\tau_F = C_D \frac{g_m}{g_m} \quad \text{with} \quad g_m = \frac{I_C}{V_T}
\]
Early Effect and Early Voltage

- As reverse-bias across the collector-base junction increases, width of the collector-base depletion layer increases and width of the base decreases (termed “base-width modulation”).
- In a practical BJT, the output characteristics have a positive slope in forward-active region; collector current is not independent of \( v_{CE} \).
- Early effect: When the output characteristics are extrapolated back to point of zero \( i_C \), the curves intersect (approximately) at a common point \( v_{CE} = -V_A \) which lies between 15 V and 150 V. (\( V_A \) is named the Early voltage)
- Simplified equations (including Early effect):

\[
\begin{align*}
  i_C &= I_s \exp\left(\frac{v_{BE}}{V_T}\right) \left[1 + \frac{v_{CE}}{V_A}\right] \\
  \beta_F &= \beta_{FO} \left[1 + \frac{v_{CE}}{V_A}\right] \\
  i_B &= \frac{I_s}{\beta_{FO}} \exp\left(\frac{v_{BE}}{V_T}\right)
\end{align*}
\]
BJT SPICE Model

- Besides capacitances associated with the physical structure, additional components are: diode current $i_S$ and substrate capacitance $C_{JS}$ related to the large area $pn$ junction that isolates the collector from the substrate and one transistor from the next.

- $R_B$ is resistance between the external base contact and the intrinsic base region.

- Collector current must pass through $R_C$ on its way to the active region of the collector-base junction.

- $R_E$ models any extrinsic emitter resistance in device.
BJT SPICE Model Parameters

Typical Values

Saturation Current  $I_S = 3 \times 10^{-17}$ A
Forward current gain  $B_F = 100$
Reverse current gain  $B_R = 0.5$
Forward Early voltage  $V_{AF} = 75$ V
Base resistance  $R_B = 250$ Ω
Collector Resistance  $R_C = 50$ Ω
Emitter Resistance  $R_E = 1$ Ω
Forward transit time  $T_T = 0.15$ ns
Reverse transit time  $T_R = 15$ ns
High Performance BJTs

- Modern BJTs use a combination of shallow and deep trench isolation processes to reduce device capacitances and transit times.
- Devices have polysilicon emitters, narrow bases, and/or SiGe base regions.
- SiGe transistors exhibit cutoff frequencies > 100 GHz.
Biasing for the BJT

Overview

• The goal of biasing is to establish known Q-point which in turn establishes initial operating region of the transistor.
• For a BJT, the Q-point is represented by \((I_C, V_{CE})\) for an \(n\!p\!n\) transistor or \((I_C, V_{EC})\) for a \(p\!n\!p\) transistor.
• The Q-point controls values of diffusion capacitance, transconductance, input and output resistances.
• In general, during circuit analysis, we use simplified mathematical relationships derived for a specified operation region, and the Early voltage is assumed to be infinite.
• Two practical biasing circuits used for a BJT are:
  – Four-Resistor Bias Network
  – Two-Resistor Bias Network
BJT Biasing
Four-Resistor Bias Network

Thevenin Equivalent of Base Bias Network

\[ V_{EQ} = V_{CC} \frac{R_1}{R_1 + R_2} = 4 \text{ V} \]

\[ R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = 12 \text{ kΩ} \]

\[ V_{EQ} = I_B R_{EQ} + V_{BE} + I_E R_E \]

\[ I_B = \frac{V_{EQ} - V_{BE}}{R_{EQ} + (\beta_F + 1) R_E} \]

\[ I_B = \frac{4V - 0.7V}{12kΩ + (76)16kΩ} = 2.69 \text{ μA} \]

\[ I_C = \beta_F I_B = 202 \text{ μA} \]

\[ I_E = (\beta_F + 1) I_B = 204 \text{ μA} \]

\[ V_{CE} = V_{CC} - I_C R_C - I_E R_E = 4.29 \text{ V} \]

Forward active region is correct

Q-point is (202 μA, 4.29 V)
BJT Biasing
Four-Resistor Bias Network (cont.)

- All calculated currents > 0, $V_{BC} = V_{BE} - V_{CE} = 0.7 - 4.32 = -3.62 \text{ V}$
- Hence, base-collector junction is reverse-biased, and assumption of forward-active region operation is correct.
- Load-line for the circuit is:

$$V_{CE} = V_{CC} - \left( R_C + \frac{R_E}{\alpha_F} \right) I_C = 12 - 38200I_C$$

The two points needed to plot the load line are (0, 12 V) and (314 μA, 0). The resulting load line is plotted on the common-emitter output characteristics.

$I_B = 2.7 \text{ μA}$ - the intersection of the corresponding characteristic with load line gives the Q-point: (200 μA, 4.3 V)
BJT Biasing

Four-Resistor Bias Design Objectives

- We know that

\[ I_C \cong I_E = \frac{V_{EQ} - V_{BE} - I_B R_{EQ}}{R_E} \cong \frac{V_{EQ} - V_{BE}}{R_E} \quad \text{for} \quad I_B R_{EQ} \ll \left( V_{EQ} - V_{BE} \right) \]

- We desire \( I_B \ll I_{R2} \) that \( I_{R1} = I_{R2} \). In this case, base current doesn’t disturb the voltage divider action of \( R_1 \) and \( R_2 \). Thus, the Q-point is independent of base current as well as current gain!

- Also, \( V_{EQ} \) is designed to be large enough that small variations in the assumed value of \( V_{BE} \) won’t affect \( I_E \) and \( I_C \).

- Current in the base voltage divider network is set by choosing \( I_2 \leq I_C/5 \). This ensures that power dissipation in bias resistors is < 17% of the total quiescent power consumed by circuit, and \( I_2 \gg I_B \) for \( \beta > 50 \).
BJT Biasing

Four-Resistor Bias Design Guidelines

- Choose Thévenin equivalent base voltage
  \[
  \frac{V_{CC}}{4} \leq V_{EQ} \leq \frac{V_{CC}}{2}
  \]

- Select \( R_1 \) to set \( I_1 = 9I_B \).
  \[
  R_1 = \frac{V_{EQ}}{9I_B}
  \]

- Select \( R_2 \) to set \( I_2 = 10I_B \).
  \[
  R_2 = \frac{V_{CC} - V_{EQ}}{10I_B}
  \]

- \( R_E \) is determined by \( V_{EQ} \) and the desired \( I_C \).
  \[
  R_E \approx \frac{V_{EQ} - V_{BE}}{I_C}
  \]

- \( R_C \) is determined by desired \( V_{CE} \).
  \[
  R_C \approx \frac{V_{EQ} - V_{BE}}{I_C} - R_E
  \]
Four-Resistor Bias for BJT

Design Example

- **Problem:** Design 4-resistor bias circuit with given parameters.
- **Given data:** $I_C = 750 \ \mu\text{A}$, $\beta_F = 100$, $V_{CC} = 15 \ \text{V}$, $V_{CE} = 5 \ \text{V}$
- **Assumptions:** Forward-active operation region, $V_{BE} = 0.7 \ \text{V}$
- **Analysis:** Divide $(V_{CC} - V_{CE})$ equally between $R_E$ and $R_C$. Thus, $V_E = 5 \ \text{V}$ and $V_C = 10 \ \text{V}$; Choose nearest 5% resistor values.

\[
R_C = \frac{V_{CC} - V_C}{I_C} = 6.67 \ \text{k}\Omega \rightarrow 6.8 \ \text{k}\Omega \quad I_2 = 10I_B = 75.0 \ \mu\text{A}
\]

\[
R_E = \frac{V_E}{I_E} = 6.60 \ \text{k}\Omega \rightarrow 6.8 \ \text{k}\Omega \quad I_2 = 9I_B = 67.5 \ \mu\text{A}
\]

\[
V_B = V_E + V_{BE} = 5.7 \ \text{V}
\]

\[
I_B = \frac{I_C}{\beta_F} = 7.5 \ \mu\text{A}
\]

\[
R_1 = \frac{V_B}{9I_B} = 84.4 \ \text{k}\Omega \rightarrow 82 \ \text{k}\Omega
\]

\[
R_2 = \frac{V_{CC} - V_B}{10I_B} = 124 \ \text{k}\Omega \rightarrow 120 \ \text{k}\Omega
\]
BJT Biasing

Two-Resistor Bias Example

- **Problem:** Find the Q-point for a pnp transistor in a 2-resistor bias circuit with given parameters.
- **Given data:** $\beta_T = 50$, $V_{CC} = 9$ V
- **Assumptions:** Forward-active operation region, $V_{EB} = 0.7$ V
- **Analysis:**

\[
9 = V_{EB} + 18000I_B + 1000(I_C + I_B)
\]

\[
9 = V_{EB} + 18000I_B + 1000(51I_B)
\]

\[
I_B = \frac{9 - 0.7}{69000} = 120 \mu A \quad I_C = 50I_B = 6.01 \text{ mA}
\]

\[
V_{EC} = 9 - 1000(I_C + I_B) = 2.88 \text{ V} \quad V_{EC} > V_{BE}
\]

Forward-active region operation is correct Q-point is : (6.01 mA, 2.88 V)
Tolerances & Worst-Case Analysis

Example

- **Problem:** Find worst-case values of $I_C$ and $V_{CE}$ in the circuit below.
- **Given data:** $\beta_{FO} = 75$ with 50% tolerance, $V_A = 50$ V, 5% tolerance on $V_{CC}$, 10% tolerance for each resistor. $R_1 = 18 \, \Omega$, $R_2 = 36 \, \Omega$.
- **Simplified Analysis:**

$$ I_C \equiv I_E \equiv \frac{V_{EQ} - V_{BE}}{R_E} $$

To maximize $I_C$, $V_{EQ}$ should be maximized, $R_E$ should be minimized and the opposite for minimizing $I_C$. Extremes of $R_E$ are: 14.4 $\Omega$ and 17.6 $\Omega$.

$$ V_{EQ} = V_{CC} \frac{R_1}{R_1 + R_2} = \frac{V_{CC}}{1 + \left(\frac{R_2}{R_1}\right)} $$

To maximize $V_{EQ}$, $V_{CC}$ and $R_1$ should be maximized, $R_2$ should be minimized and opposite for minimizing $V_{EQ}$. 
Tolerances & Worst-Case Analysis

Example (cont.)

\[ V_{CC} = 12V \pm 5\% \]
\[ R_1 = 18k\Omega \pm 10\% \]
\[ R_2 = 36k\Omega \pm 10\% \]

\[ V_{EQ} = V_{CC} \frac{R_1}{R_1 + R_2} = \frac{V_{CC}}{1 + \left( \frac{R_2}{R_1} \right)} \]

\[ R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} = R_1 \parallel R_2 \]

\[ V_{EQ}^{\max} = \frac{12V(1.05)}{1 + \left[ \frac{36k\Omega(0.9)}{18k\Omega(1.1)} \right]} = 4.78 \text{ V} \]

\[ I_C^{\max} \approx \frac{4.78V - 0.7V}{16k\Omega(0.90)} = 283 \ \mu\text{A} \]

\[ V_{EQ}^{\min} = \frac{12V(0.95)}{1 + \left[ \frac{36k\Omega(1.1)}{18k\Omega(0.9)} \right]} = 3.31 \text{ V} \]

\[ I_C^{\min} \approx \frac{3.31V - 0.7V}{16k\Omega(1.1)} = 148 \ \mu\text{A} \]
Extremes of $V_{EQ}$ are: 4.78 V and 3.31 V.
Extremes for $I_C$ are: 283 $\mu$A and 148 $\mu$A.

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \equiv V_{CC} - I_C R_C - \frac{V_{EQ} - V_{BE}}{R_E} R_E$$

$$V_{CE} \equiv V_{CC} - I_C R_C - V_{EQ} + V_{BE}$$

$$V_{CE}^{\text{max}} = 12V \left(1.05\right) - 0.148mA \left(22k\Omega\right) \left(0.9\right) - 3.31 + 0.7 = 6.73 \text{ V}$$

$$V_{CE}^{\text{min}} = 12V \left(0.95\right) - 0.283mA \left(22k\Omega\right) \left(1.1\right) - 4.78 + 0.7 = 0.471 \text{ V} \times$$

To maximize $V_{CE}$, $I_C$ and $R_C$ should be minimized, and opposite for minimizing $V_{EQ}$.
Extremes of $V_{CE}$ are: 7.06 V (forward-active region) and 0.471 V (saturated, hence calculated values for $V_{CE}$ and $I_C$ actually not correct).
Tolerances - Monte Carlo Analysis

- In real circuits, it is unlikely that various components will reach their extremes at the same time, instead they will have some statistical distribution. Hence worst-case analysis over-estimates extremes of circuit behavior.
- In Monte Carlo analysis, values of each circuit parameter are randomly selected from possible distributions of parameters and used to analyze the circuit.
- Random parameter sets are generated, and the statistical behavior of circuit is built up from the analysis of many test cases.
**Tolerances - Monte Carlo Analysis**

**Example**

For each Case: Assign random values to all circuit elements

\[ V_{CC} = 12 \left[ 1 + 0.1 (Rand(\ ) - 0.5) \right] \]

\[ R_1 = 18000 \left[ 1 + 0.2 (Rand(\ ) - 0.5) \right] \]

\[ R_2 = 36000 \left[ 1 + 0.2 (Rand(\ ) - 0.5) \right] \]

\[ R_E = 16000 \left[ 1 + 0.2 (Rand(\ ) - 0.5) \right] \]

\[ R_C = 22000 \left[ 1 + 0.2 (Rand(\ ) - 0.5) \right] \]

\[ \beta_F = 75 \left[ 1 + (Rand(\ ) - 0.5) \right] \]

Then calculate resulting currents and voltages

\[ V_{EQ} = V_{CC} \frac{R_1}{R_1 + R_2} \]

\[ R_{EQ} = \frac{R_1 R_2}{R_1 + R_2} \]

\[ I_B = \frac{V_{EQ} - V_{BE}}{R_{EQ} + (\beta_F + 1) R_E} \]

\[ I_C = \beta_F I_B \]

\[ I_E = (\beta_F + 1) I_B \]

\[ V_{CE} = V_{CC} - I_C R_C - I_E R_E \]

Note: Assume constant \( V_{BE} = 0.7 \) for simplicity.
• Full results of Monte Carlo analysis of 500 cases of the 4-resistor bias circuit yields mean values of 207 \( \mu \)A and 4.06 V for \( I_C \) and \( V_{CE} \) respectively which are close to values originally estimated from nominal circuit elements. Standard deviations are 19.6 \( \mu \)A and 0.64 V respectively.

• The worst-case calculations lie well beyond the extremes of the distributions
  – Note that circuit never saturates in the Monte Carlo Analyses
End of Chapter 5