## Chapter 3Solid-State Diodes and Diode Circuits

#### **Microelectronic Circuit Design**

Richard C. JaegerTravis N. Blalock



**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Chapter Goals

- •Understand diode structure and basic layout
- •Develop electrostatics of the *pn* junction
- $\bullet$  Explore various diode models including the mathematical model, the ideal diode model, and the constant voltage drop model
- • Understand the SPICE representation and model parameters for the diode
- $\bullet$  Define regions of operation of the diode (forward bias, reverse bias, and reverse breakdown)
- •Apply the various types of models in circuit analysis
- •Explore different types of diodes
- $\bullet$ Discuss the dynamic switching behavior of the *pn* junction diode
- •Explore diode applications
- •Practice simulating diode circuits using SPICE

#### Diode Introduction





Diode symbol

- $\bullet$  A diode is formed by joining an *n*-type semiconductor with a *p*-type semiconductor.
- $\bullet$  <sup>A</sup>*pn* **junction** is the interface between *n* and *p*regions.

**Jaeger/Blalock 4/28/11**

#### *pn*n Junction Electrostatics



**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Drift Currents

- • Diffusion currents lead to localized charge density variations near the *pn* junction.
- $\bullet$ Gauss' law predicts an electric field due to the charge distribution:

$$
\nabla \cdot E = \frac{\rho_c}{\varepsilon_s}
$$

•Assuming constant permittivity,

$$
E(x) = \frac{1}{\varepsilon_s} \int \rho(x) dx
$$

 $\bullet$  Resulting electric field gives rise to a drift current. With no external circuit connections, drift and diffusion currents cancel. There is no actual current, since this would imply power dissipation, rather the electric field cancels the diffusion current 'tendency.'

**Jaeger/Blalock 4/28/11**

# Space-Charge Region Formation at the *pn* Junction



**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Potential Across the Junction



**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Width of Depletion Region

Combining the previous expressions, we can form an expression for the width of the space-charge region, or depletion region. The region is referred to as the depletion region since the excess holes and electrons are depleted from the dopant atoms on either side of the junction.

$$
w_{d0} = (x_n + x_p) = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \phi_j
$$

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLEWidth of Depletion Region

**Problem:** Find built-in potential and depletion-region width for a given diode**Given data:** On *p*-type side:  $N_A = 10^{17}/\text{cm}^3$ ; On *n*-type side:  $N_D = 10^{20}/\text{cm}^3$ **Assumptions:** Room-temperature operation with  $V_T = 0.025$  V **Analysis:**

$$
\phi_j = V_T \ln \left( \frac{N_A N_D}{n_i^2} \right) = (0.025 \text{ V}) \ln \left[ \frac{\left( 10^{17} / \text{cm}^3 \right) \left( 10^{20} / \text{cm}^3 \right)}{\left( 10^{20} / \text{cm}^6 \right)} \right] = 0.979 \text{ V}
$$

$$
w_{d0} = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D}\right) \phi_j} = 0.113 \ \mu \text{m}
$$

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLEDiode Electric Field

- **Problem:** Find the electric field and size of the individual depletion layers on either side of a *pn* junction for a given diode
- Given data: On the *p*-type side:  $N_A = 10^{17} / \text{cm}^3$  on the *n*-type side:  $N_D =$  $10^{20}$ /cm<sup>3</sup> from earlier example,  $\phi_j = 0.979V$  *w*<sub>*d*0</sub> = 0.113  $\mu$ m
- **Assumptions**: Room-temperature operation
- **Analysis:**

$$
w_{d0} = x_n + x_p = x_n \left( 1 + \frac{N_D}{N_A} \right) = x_p \left( 1 + \frac{N_A}{N_D} \right)
$$
  

$$
x_n = \frac{w_{d0}}{\left( 1 + \frac{N_D}{N_A} \right)} = 1.13 \times 10^{-4} \ \mu m \qquad x_p = \frac{w_{d0}}{\left( 1 + \frac{N_A}{N_D} \right)} = 0.113 \ \mu m
$$
  

$$
E_{MAX} = \frac{2\phi_j}{w_{d0}} = \frac{2(0.979V)}{0.113 \mu m} = 173 \ \ kV/cm
$$

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Internal Diode Currents

Mathematically, for a diode with no external connections, the total current expressions developed in Chapter 2 are equal to zero. The equations only dictate that the total currents are zero. However, as mentioned earlier, since there is no power dissipation, we must assume that the drift and diffusion current tendencies cancel and the individual hole and electron currents are both zero.

$$
j_n^T = q\mu_n nE + qD_n \frac{\partial n}{\partial x} = 0
$$
  

$$
j_p^T = q\mu_p pE - qD_p \frac{\partial p}{\partial x} = 0
$$

When external bias voltage is applied to the diode, the above equations are no longer equal to zero.

**Jaeger/Blalock 4/28/11**

## Diode Junction Potential for Different Applied Voltages



Applied voltage v<sub>D</sub> There is negligible voltage drop in the ohmic regions<sub>D</sub> appears across the space-charge region

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

# Diode *i-v* Characteristics



The turn-on voltage marks the point of significant current flow.*IS* is called the reverse saturation current.

## Diode Equation

$$
i_D = I_S \left[ \exp\left(\frac{qv_D}{nkT}\right) - 1 \right] = I_S \left[ \exp\left(\frac{v_D}{nV_T}\right) - 1 \right]
$$



 $I<sub>S</sub>$  is typically between 10<sup>-18</sup> and 10<sup>-9</sup> A, and is strongly temperature dependent due to its dependence on  $n_i^2$ . The non-ideality factor is typically close to 1, but approaches 2 for devices with high current densities. It is assumed to be 1 in this text.

 $+ v_D -$ 

 $i_D$ 

#### EXAMPLEDiode Voltage and Current Calculations

**Problem:** Find diode voltage for diode with given specificationsGiven data:  $(I_S, I_D) = (0.1 \text{ fA}, 300 \mu\text{A}), (10 \text{ fA}, 300 \mu\text{A}), (0.1 \text{ fA}, 1 \text{ mA})$ **Assumptions:** Room-temperature dc operation with  $V_T = 0.025$  V **Analysis:**

With 
$$
I_s = 0.1
$$
 fA:  $V_D = nV_T \ln \left( 1 + \frac{I_D}{I_S} \right) = 1(0.025V) \ln \left( 1 + \frac{3x10^{-4} A}{10^{-16} A} \right) = 0.718 V$   
\nWith  $I_s = 10$  fA:  $V_D = (0.025V) \ln \left( 1 + \frac{3x10^{-4} A}{10^{-14} A} \right) = 0.603 V$   
\nWith  $I_s = 0.1$  fA,  $I_D = 1$  mA:  $V_D = (0.025V) \ln \left( 1 + \frac{10^{-3} A}{10^{-16} A} \right) = 0.748 V$ 

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Diode Current for Reverse, Zero, and Forward Bias

- $\bullet$  Reverse bias: *i D*=*I* $I_{S}$  exp *v* $\underline{P}$  $nV^T$  $\bigg($  $\setminus$  $\bigg)$  $\int$ 1 $\overline{\phantom{a}}$  $\overline{\phantom{a}}$  $\overline{\phantom{0}}$  <sup>≅</sup> *I* $I_{S} \left[ 0-1 \right] \equiv$ − $1 \equiv -1$ *IS*
- • Zero bias: *v* $\overline{\phantom{a}}$   $\bigg)$  $\overline{\phantom{0}}$  $i_{\rm b} = I_{\rm s}$  exp $\frac{D}{2}$  - 1 *D*=*I* $I_{S}$  exp  $\frac{P}{nV}$  $\left\langle nV_{T}\right\rangle$  $\int$ 1 $\overline{\mathsf{L}}$  $\overline{\phantom{a}}$  <sup>≅</sup> *I* $I_{S}[1-1]$   $\cong$ 1≅0
- •Forward bias:

$$
i_D = I_s \left[ \exp\left(\frac{v_D}{nV_T}\right) - 1 \right] \equiv I_s \exp\left(\frac{v_D}{nV_T}\right)
$$

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Semi-log Plot of Forward Diode Current and Current for Three Different Values of  $I_{\rm S}$



**Jaeger/Blalock 4/28/11**

**Chap 3 - 17**

#### Diode Temperature Coefficient

Diode voltage under forward bias:

$$
v_D = V_T \ln \left( \frac{i_D}{I_S} + 1 \right) = \frac{kT}{q} \ln \left( \frac{i_D}{I_S} + 1 \right) \approx \frac{kT}{q} \ln \left( \frac{i_D}{I_S} \right)
$$

Taking the derivative with respect to temperature yields

$$
\frac{dv_D}{dT} = \frac{k}{q} \ln \left( \frac{i_D}{I_S} \right) - \frac{kT}{q} \frac{1}{I_S} \frac{dI_S}{dT} = \frac{v_D}{T} - V_T \frac{1}{I_S} \frac{dI_S}{dT} = \frac{v_D - V_{GO} - 3V_T}{T}
$$
 V/K

Assuming i<sub>D</sub>  $I_D$  >>  $I_S$ ,  $I_S \propto n_i^2$ , and  $V_{GO}$  is the silicon bandgap energy at 0 K. For a typical silicon diode

$$
\frac{dv_D}{dT} = \frac{(0.65 - 1.12 - 0.075)W}{300K} = -1.82 \text{ mV/K} \approx -1.8 \text{ mV}^{\circ}\text{C}
$$

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Reverse Bias

External reverse bias adds to the built-in potential of the pn junction. The shaded regions below illustrate the increase in the characteristics of the space charge region due to an externally applied reverse bias,  $v<sub>D</sub>$ .



**Jaeger/Blalock 4/28/11**

#### Reverse Bias (cont.)

External reverse bias also increases the width of the depletion region since the larger electric field must be supported by additional charge.

$$
w_d = (x_n + x_p) = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \left(\phi_j + v_R\right)
$$
  

$$
w_d = w_{d0} \sqrt{1 + \frac{v_R}{\phi_j}}
$$
  
where  $w_{d0} = (x_n + x_p) = \sqrt{\frac{2\varepsilon_s}{q} \left(\frac{1}{N_A} + \frac{1}{N_D}\right)} \phi_j$ 

**Jaeger/Blalock 4/28/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

### Reverse Bias Saturation Current

We earlier assumed that the reverse saturation current was constant. Since it results from thermal generation of electron-hole pairs in the depletion region, it is dependent on the volume of the space charge region. It can be shown that the reverse saturation gradually increases with increased reverse bias.

$$
I_S = I_{S0} \sqrt{1 + \frac{v_R}{\phi_j}}
$$

 $I_{\scriptscriptstyle S}$  is approximately constant at  $I_{\scriptscriptstyle SO}$  under forward bias.

**Jaeger/Blalock 4/28/11**

#### Reverse Breakdown

Increased reverse bias eventually results in the diode entering the **breakdown region**, resulting in a sharp increase in the diode current. The voltage at which this occurs is the **breakdown** voltage,  $V_z$ .





**Jaeger/Blalock 4/28/11**



## Reverse Breakdown Mechanisms

#### $\bullet$ **Avalanche Breakdown**

 Si diodes with *VZ* greater than about 5.6 volts breakdown according to an avalanche mechanism. As the electric field increases, accelerated carriers begin to collide with fixed atoms. As the reverse bias increases, the energy of the accelerated carriers increases, eventually leading to ionization of the impacted ions. The new carriers also accelerate and ionize other atoms. This process feeds on itself and leads rapidly to avalanche breakdown.



**Jaeger/Blalock 4/29/11**

## Reverse Breakdown Mechanisms (cont.)

#### •**Zener Breakdown**

 Zener breakdown occurs in heavily doped diodes. The heavy doping results in a very narrow depletion region at the diode junction. Reverse bias leads to carriers with sufficient energy to tunnel directly between conduction and valence bands moving across the junction. Once the tunneling threshold is reached, additional reverse bias leads to a rapidly increasing reverse current.

#### $\bullet$ **Breakdown Voltage Temperature Coefficient**

Temperature coefficient is a quick way to distinguish breakdown mechanisms. Avalanche breakdown voltage increases with temperature, whereas Zener breakdown decreases with temperature.

For silicon diodes, zero temperature coefficient is achieved at approximately 5.6 V.

#### Breakdown Region Diode Model



In breakdown, the diode is modeled with a voltage source, *V<sup>Z</sup>*, and a series resistance, *RZ*.  $R_{\rm Z}$  models the slope of the  $\imath$  characteristic. models the slope of the *i-v*

Diodes designed to operate in reverse breakdown are called **Zener diodes** (regardless of the actual mechanism) and use the indicated symbol.

**Jaeger/Blalock 4/30/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Reverse Bias Capacitance

Changes in voltage lead to changes in depletion width and charge. This leads to a capacitance that we can calculate from the chargevoltage dependence.

$$
Q_n = qN_D x_n A = q \left(\frac{N_A N_D}{N_A + N_D}\right) w_d A
$$
 Coulombs

$$
C_j = \frac{dQ_n}{dv_R} = \frac{C_{j0}A}{\sqrt{1 + \frac{v_R}{\phi_j}}} \quad \text{F/cm}^2 \quad \text{where } C_{j0} = \frac{\varepsilon_s}{w_{d0}}
$$

*<sup>C</sup>j0* is the zero bias junction capacitance per unit area.

**Jaeger/Blalock 4/29/11**

## Reverse Bias Capacitance (cont.)

Diodes can be designed with hyper-abrupt doping profiles that optimize the reverse-biased diode as a voltage controlled capacitor.



Circuit symbol for the variable capacitance diode(Varactor diodes)

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Forward Bias Capacitance

In forward bias operation, additional charge is stored in the neutral region near the edges of space charge region.

 $Q_D = i_D \tau_T$  Coulombs

 $\tau$ <sub>*T*</sub> is called diode transit time and depends on the size and type of diode.

Additional diffusion capacitance, associated with forward region operation is proportional to current and becomes quite large at high currents.

$$
C_j = \frac{dQ_D}{dv_D} = \frac{(i_D + I_S)\tau_T}{V_T} \cong \frac{i_D \tau_T}{V_T} \quad F
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Schottky Barrier Diode



non-ohmic rectifying metal contact. A Schottky contact is easily formed on *n*-type silicon. The metal region becomes the anode. An *n+* region is added to ensure that the cathode contact is ohmic.

Schottky diodes turn on at a lower voltage than *pn* junction diodes and have significantly reduced internal charge storage under forward bias. Thus Schottky diodes switch faster.

Diode voltage (V)

**Jaeger/Blalock 4/29/11**

#### Diode Spice Model



*Rs* represents the inevitable series resistance of a real device structure. The current controlled current source models the ideal exponential behavior of the diode. Capacitor C includes depletion-layer capacitance for the reverse-bias region as well as diffusion capacitance associated with the junction under forward bias.

Typical default values: Saturation current IS = 10 fA,  $R_s = 0 \Omega$ , transit time  $TT = 0$  seconds,  $N = 1$ 

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Basic Diode Layout



**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Diode dc Circuit Analysis: Basics



V and R may represent the Thévenin equivalent of a more complex 2terminal network. The objective of diode dc circuit analysis is to find the **quiescent operating point** for the diode.

The loop equation for the diode circuit is:

$$
V = I_D R + V_D
$$

This is also called the **load line** for the diode. The solution to this equation can be found by:

- Graphical analysis using the load-line method.
- Analysis with the diode's mathematical model.
- Simplified analysis with the ideal diode model.
- Simplified analysis using the constant voltage drop (CVD) model.

 $Q\text{-Point} = (I_D, V_D)$ 

**Microelectronic Circuit Design, 4E McGraw-Hill**

**Jaeger/Blalock 4/29/11**

## EXAMPLELoad-Line Analysis



**Problem:** Find diode Q-point  $G$ iven data:  $V = 10$  V,  $R = 10$  kΩ. **Analysis:**

 $10 = I_D 10^4 + V_D$ 

To define the load line we use, $For V_D = 0, I_D = (10V/10k\Omega) = 1 mA$ 

 $For V_D = 5V, I_D = (5V/10k\Omega) = 0.5$  *mA* 

These points and the resulting load line are plotted. Q-point is given by the intersection of the load line and diode characteristic:

**Q-point = (0.95 mA, 0.6 V)**

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLEAnalysis using Diode Mathematical Model

**Problem:** Find the Q-point for a given diode characteristic.

**Given data:**  $I_s = 10^{-13}$ A, n = 1,  $V_T = 0.025$ V **Analysis:**

$$
I_D = I_S \left[ exp\left(\frac{V_D}{nV_T}\right) - 1 \right] = 10^{-13} [exp(40V_D) - 1]
$$
  
.: 10 = 10<sup>4</sup>10<sup>-13</sup> [exp(40V\_D) - 1] + V\_D

The solution is given by a transcendental equation. A numerical answer can be found by using Newton's iterative method.

$$
f = 10 - 10^4 10^{-13} \left[ \exp(40V_D) - 1 \right] - V_D
$$

- •Make initial guess  $V_D^0$ . •Evaluate f and its derivative f' for this value of *V<sup>D</sup>*.
- •Calculate new guess for  $V_D$  using

$$
V_D^1 = V_D^0 - \frac{f(V_D^0)}{f'(V_D^0)}
$$

•Repeat steps 2 and 3 till convergence.

Using a spreadsheet we get :**Q-point = ( 0.9426 mA, 0.5742 V)**

Since, usually we don't have accurate saturation current values and significant tolerances exist for sources and passive components, we need answers precise to  $f = 10 - 10^{4} 10^{-13} \left[ \exp(40V_D) - 1 \right] - V_D$  components, we need answer only 2 or 3 significant digits.

**Jaeger/Blalock 4/29/11**

## Analysis using Ideal Model for Diode



If an ideal diode is forward-biased, the voltage across the diode is zero. If an ideal diode is reverse-biased, the current through the diode is zero.

 $v_D = 0$  for  $i_D > 0$  and  $i_D = 0$  for  $v_D < 0$ 

Thus, the diode is assumed to be either on or off. Analysis is conducted in following steps:

• Select a diode model.

• Identify anode and cathode of the diode and label *vD* $D$  and  $i_D$ .

• Guess diode's region of operation from circuit.

• Analyze circuit using diode model appropriate for assumed region of operation.

• Check results to check consistency with assumptions.

**Jaeger/Blalock 4/29/11**

## EXAMPLEAnalysis using Ideal Model for Diode



Since source appears to force positive current through diode, assume diode is on.

$$
I_D = \frac{(10-0)V}{10k\Omega} = 1 \text{ mA} \qquad I_D \ge 0
$$
  
is correct, and the

Our assumption is correct, and the **Q-Point = (1 mA, 0V)**

Since source is forcing current backward through diode assume, diode is off.

Hence  $I_D = 0$  . Loop equation is:

Our assumption is correct and the**Q-Point = (0, -10 V)** $10 + V_D + 10^4 I_D = 0$  $V_D = -10V$  |  $V_D < 0$ 

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Analysis using Constant Voltage Drop Model for Diode



**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLETwo-Diode Circuit Analysis



**Analysis:** The ideal diode model is chosen. Since the 15-V source appears to force positive current through  $D_1$  and  $D_2$ , and the -10-V source is forcing positive current through  $D_2$ , assume both diodes are on.

Since the voltage at node  $D$  is zero due to the short circuit of ideal diode  $D_1$ ,

$$
I_1 = \frac{(15-0)V}{10k\Omega} = 1.50 mA
$$
  
\n
$$
I_{D2} = \frac{0 - (-10V)}{5k\Omega} = 2.00 mA
$$
  
\n
$$
I_1 = I_{D1} + I_{D2} \mid I_{D1} = 1.50 - 2.00 = -0.500 mA
$$
  
\nThe Q-points are (-0.5 mA, 0 V) and (2.0 mA, 0 V)  
\nBut,  $I_{D1} < 0$  is not allowed by the diode, so try again.

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLETwo-Diode Circuit Analysis (cont.)



Since the current in  $D_1$  is zero,  $I_{D2} = I_1$ ,

$$
15-10,000I_1 - 5,000I_{D2} - (-10) = 0
$$
  
\n
$$
I_1 = \frac{25V}{15,000\Omega} = 1.67 \text{ mA}
$$
  
\n
$$
V_{D1} = 15-10,000I_1 = 15-16.7 = -1.67 \text{ V}
$$

**Analysis:** Since current in  $D_2$  is valid, but that in  $D_1$  is not, the second guess is  $D_1$ off and  $D_2$  on.

**Q-Points are** *D***1 : (0 mA, -1.67 V): off** *D***2 : (1.67 mA, 0 V) : on**

Now, the results are consistent with the assumptions.

**Jaeger/Blalock 4/29/11**

## EXMPLEAnalysis of Diodes in Reverse Breakdown



**Jaeger/Blalock 4/29/11**

## EXAMPLEVoltage Regulator Using the Zener Diode



The Zener diode keeps the voltage across load resistor R<sub>L</sub> constant. For Zener breakdown operation,  $I_Z > 0$ .

$$
I_{S} = \frac{V_{S} - V_{Z}}{R} = \frac{(20 - 5)V}{5k\Omega} = 3 \text{ mA}
$$
  

$$
I_{L} = \frac{V_{Z}}{R_{L}} = \frac{5V}{5k\Omega} = 1 mA \quad | \quad I_{Z} = I_{S} - I_{L} = 2 mA
$$

For proper regulation, Zener current  $I_z$  must be positive. If the Zener current  $< 0$ , the Zener diode no longer controls the voltage across the load resistor and the voltage regulator is said to have "dropped out of regulation".

$$
I_{Z} = \frac{V_{S}}{R} - V_{Z} \left(\frac{1}{R} + \frac{1}{R_{L}}\right) > 0 \quad | \quad R_{L} > \frac{R}{\left(\frac{V_{S}}{V_{Z}} - 1\right)} = R_{\text{min}}
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLEVoltage Regulator Including Zener Resistance

**Problem:** Find the output voltage and Zener diode current for a Zener diode regulator.Given data:  $V_s = 20 \text{ V}, R = 5 \text{ k}\Omega$ ,  $R$ <sub>*Z*</sub> = 0.1 kΩ,  $V$ <sub>*Z*</sub> = 5 V **Analysis:** The output voltage is now a function of the current through the Zener diode.



$$
I_{Z} = \frac{V_{L} - 5V}{100\Omega} = \frac{5.19V - 5V}{100\Omega} = 1.9 \text{ mA} > 0
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Line and Load Regulation

**Line regulation** characterizes how sensitive the output voltage is to input voltage changes.

Line Regulation=
$$
\frac{dV_L}{dV_S}
$$
 mV/V

For a fixed load current, Line Regulation =  $_{\small -}$ *RZ R*+*R*

 **Load regulation** characterizes how sensitive the output voltage is to *Z*changes in load current withdrawn from regulator.

$$
Load Regulation = \frac{dV_L}{dI_L} \ \Omega
$$

 For changes in load current, Load Regulation=−*RZ* $\left(R\underset{Z}{\|}R\right]$ ا  $\begin{pmatrix} 1 \\ 1 \end{pmatrix}$ 

Load regulation is the Thévenin equivalent resistance looking back into the regulator from the load terminals.

**Jaeger/Blalock 4/29/11**

## Rectifier Circuits

- A basic rectifier converts an ac voltage to a pulsating dc voltage.
- A filter then eliminates ac components of the waveform to produce a nearly constant dc voltage output.
- Rectifier circuits are used in virtually all electronic devices to convert the 120-V 60-Hz ac power line source to the dc voltages required for operation of electronic devices.
- In rectifier circuits, the diode state changes with time and a given piecewise linear model is valid only for a certain time interval.

## Half-Wave Rectifier Circuit with Resistive Load



For the positive half-cycle of the input, the source forces positive current through the diode, the diode is on, and  $v_O = v_S$  (for an ideal diode).

During the negative half cycle, negative current can't exist in the diode. The diode is off, current in resistor is zero, and  $v<sub>O</sub> = 0$ .

## Half-Wave Rectifier Circuit with Resistive Load (cont.)



Using the CVD model, during the on-state of the diode  $v_Q = v_S - V_{on} = (V_P \sin \omega t) - V_{on}$ . The output voltage is zero when the diode is off.

Often a step-up or step-down transformer is used to convert the 120-V, 60-Hz voltage available from the power line to the desired ac voltage level as shown.



Time-varying components in the rectifier output are removed using a filter capacitor.

**Jaeger/Blalock 4/29/11**

#### Peak Detector Circuit



As the input voltage rises, the diode is on, and the capacitor (initially discharged) charges up to the input voltage minus the diode voltage drop.

At the peak of the input voltage, the diode current tries to reverse, and the diode cuts off. The capacitor has no discharge path and retains a constant voltage providing a constant output voltage:

$$
V_{dc} = V_P - V_{on}
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Half-Wave Rectifier Circuit with *RC* Load



As the input voltage rises during the first quarter cycle, the diode is on and the capacitor (initially discharged) charges up to the peak value of the  $v<sub>o</sub>$  input voltage.

At the peak of the input, the diode current tries to reverse, the diode cuts off, and the capacitor discharges exponentially through *R*. Discharge continues till the input voltage exceeds the output voltage which occurs near the peak of next cycle. This process then repeats once every cycle.

This circuit can be used to generate negative output voltage if the top plate of capacitor is grounded instead of bottom plate. In this case,  $V_{dc} = -(V_{P} - V_{on})$ 

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Half-Wave Rectifier Circuit with *RC* Load (cont.)

The output voltage is not constant as in an ideal peak detector, but has a **ripple voltage***Vr*.

The diode conducts for a short time ∆*T* called the **conduction interval** during each cycle, and its angular equivalent is called the **conduction**  $\textbf{angle}\ \theta_{\text{c}}$ .

$$
V_r \cong (V_p - V_{on}) \frac{T}{RC} \left(1 - \frac{\Delta T}{T}\right) \cong \frac{(V_p - V_{on})}{R} \frac{T}{C}
$$

$$
\Delta T \cong \frac{1}{\omega} \sqrt{\frac{2T}{RC} \frac{(V_p - V_{on})}{V_p}} = \frac{1}{\omega} \sqrt{\frac{2V_r}{V_p}}
$$

$$
\theta_c = \omega \Delta T = \sqrt{\frac{2V_r}{V_P}}
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## EXAMPLEHalf-Wave Rectifier Analysis

**Problem:** Find the dc output voltage, output current, ripple voltage, conduction interval, and conduction angle for a half-wave rectifier.**Given data:** secondary voltage  $V_{rms} = 12.6$  (60 Hz),  $R = 15 \Omega$ ,  $C = 25,000 \mu F, V_{on} = 1 V$ **Analysis:**

$$
V_{dc} = V_p - V_{on} = (12.6\sqrt{2} - 1)V = 16.8 \text{ V}
$$
  
\n
$$
I_{dc} = \frac{V_p - V_{on}}{R} = \frac{16.8V}{15\Omega} = 1.12 \text{ A}
$$
  
\n
$$
V_r \approx \frac{(V_p - V_{on})}{R} \frac{T}{C} = 0.747 \text{ V}
$$

Using discharge interval  $T = 1/60$  s,

$$
\theta_c = \omega \Delta T = \sqrt{\frac{2V_r}{V_P}} = 0.290 \text{ rad} = 16.6^{\circ}
$$

$$
\Delta T = \frac{\theta_c}{\omega} = \frac{\theta_c}{2\pi f} = \frac{0.29}{120\pi} = 0.769 \text{ ms}
$$

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Peak Diode Current



In rectifiers, nonzero current exists in the diode for only a very small fraction of period *T*, yet an almost constant dc current flows out of the filter capacitor to load.

The total charge lost from the filter capacitor in each cycle is replenished by the diode during a short conduction interval causing high peak diode currents. If the repetitive current pulse is modeled as a triangle of height  $I_P$  and width  $\Delta T$ ,

$$
I_P = I_{dc} \frac{2T}{\Delta T} = 48.6 \text{ A}
$$

using the values from the previous example.

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

## Surge Current

In addition to the peak diode currents, there is an even larger current through the diode called the **surge current** that occurs when power is first turned on.

During first quarter cycle, current through diode is approximately

$$
i_d(t) = i_c(t) \approx C \left(\frac{d}{dt}V_p \sin \omega t\right) = \omega CV_p \cos \omega t
$$

The peak value of this initial surge current occurs at  $t = 0^+$ :

$$
I_{\rm SC} = \omega C V_{\rm P} = 168 \, \text{A}
$$

using values from previous example.

Actual values of surge current won't be nearly as large as predicted above because of the neglected series resistances associated with both the rectifier diode and transformer.

#### Peak Inverse Voltage Rating



The peak inverse voltage (PIV) rating of the rectifier diode is the diode breakdown voltage.

When the diode is off, the reverse-bias across the diode is  $V_{dc}$  -  $v_S$ . When  $v_S$ reaches its negative peak,

$$
PIV \geq V_{dc} - v_s^{\min} = V_p - V_{on} - (-V_p) \cong 2V_p
$$

The PIV value corresponds to the minimum value of Zener breakdown voltage required for the rectifier diode.

**Jaeger/Blalock 4/29/11**

#### Diode Power Dissipation

Average power dissipation in a diode is given by

$$
P_{D} = \frac{1}{T} \int_{0}^{T} v_{D}(t) i_{D}(t) dt = \frac{1}{T} \int_{0}^{T} V_{on} i_{D}(t) dt = V_{on} \frac{I_{P}}{2} \frac{\Delta T}{T} \approx V_{on} I_{dc}
$$

The simplification is done by assuming a triangular approximation for the diode current and the voltage across the diode is constant at *Vdc*.

Average power dissipation in the diode series resistance is given by

$$
P_D = \frac{1}{T} \int_0^T i_D^2(t) R_S dt = \frac{1}{3} I_D^2 R_S \frac{\Delta T}{T} = \frac{4}{3} \frac{T}{\Delta T} I_{dc}^2 R_S
$$

This power dissipation can be reduced by minimizing peak current through the use of a minimum size of filter capacitor or by using fullwave rectifiers.

**Jaeger/Blalock 4/29/11**

#### Full-Wave Rectifiers





Full-wave rectifiers cut capacitor discharge time in half and require half the filter capacitance to achieve a given ripple voltage. All specifications are the same as for halfwave rectifiers.

Reversing polarity of the diodes gives a fullwave rectifier with negative output voltage.

**Jaeger/Blalock 4/29/11**

#### Full-Wave Rectifier Equations



**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**

#### Full-Wave Bridge Rectification



The requirement for a centertapped transformer in the fullwave rectifier is eliminated through use of 2 extra diodes. All other specifications are the same as for a half-wave rectifier except  $\mathbf{P} \mathbf{IV} = V_{P}$ .

**Jaeger/Blalock 4/29/11**

## Rectifier Topology Comparison

• Filter capacitors are a major factor in determining cost, size and weight in design of rectifiers.

• For a given ripple voltage, a full-wave rectifier requires half the filter capacitance as that in a half-wave rectifier. Reduced peak current can reduce heat dissipation in diodes. Benefits of full-wave rectification outweigh increased expenses and circuit complexity (an extra diode and center-tapped transformer).

• The bridge rectifier eliminates the center-tapped transformer, and the PIV rating of the diodes is reduced. Cost of extra diodes is negligible.

## Rectifier Topology Comparison and Design Tradeoffs



## DESIGN EXAMPLERectifier Design Analysis

**Problem:** Design a rectifier with given specifications.

**Given data:**  $V_{dc} = 15 \text{ V}$ ,  $V_r < 0.15 \text{ V}$ ,  $I_{dc} = 2 \text{ A}$  **Assume:**  $V_{on} = 1 \text{ V}$ .

**Analysis:** Use a full-wave bridge rectifier that needs a smaller value of filter capacitance, smaller diode PIV rating, and no center-tapped transformer.

$$
V = \frac{V_p}{\sqrt{2}} = \frac{V_{dc} + 2V_{on}}{\sqrt{2}} = \frac{15 + 2}{\sqrt{2}}V = 12.0 \text{ V}_{rms} \quad | \quad C = I_{dc} \left(\frac{T/2}{V_r}\right) = 2A \left(\frac{1}{120} s\right) \left(\frac{1}{0.15V}\right) = 0.111 \text{ F}
$$
  
\n
$$
\Delta T = \frac{1}{\omega} \sqrt{\frac{2V_r}{V_p}} = \frac{1}{120 \pi} \sqrt{\frac{2(0.15V)}{17V}} = 0.352 \text{ ms} \quad | \quad I_p = I_{dc} \left(\frac{2}{\Delta T} \right) \left(\frac{T}{2}\right) = 2A \frac{(1/60)s}{0.352ms} = 94.7 \text{ A}
$$
  
\n
$$
I_{surge} = \omega C V_p = 120 \pi (0.111)(17) = 711 \text{ A} \quad | \quad PIV = V_p = 17 \text{ V}
$$

**Jaeger/Blalock 4/29/11**

## Dynamic Switching Behavior of Diodes



The non-linear depletion-layer capacitance of the diode prevents the diode voltage from changing instantaneously and determines turn-on and recovery times. Both forward and reverse current overshoot the final values when the diode switches on and off as shown. Storage time is given by:



**Jaeger/Blalock 4/29/11**

**Chap 3 - 61**

#### Photo Diodes and Photodetectors



If the depletion region of a *pn* junction diode is illuminated with light with sufficiently high frequency, photons can provide enough energy to cause electrons to jump the semiconductor bandgap to generate electron-hole pairs:

$$
E_p = h v = \frac{hc}{\lambda} \ge E_G
$$

*h* =Planck's constant =  $6.626 \times 10^{-34}$  J-s

 $v =$  frequency of optical illumination

$$
\lambda = wavelength of optical illumination
$$

 $c$  = velocity of light = 3 x 10<sup>8</sup> m/s

 Photon-generated current can be used in photodetector circuits to generate an output voltage

$$
v_o = i_{\rm PH} R
$$

The diode is reverse-biased to enhance depletion-region width and electric field.

**Jaeger/Blalock 4/29/11**

#### Solar Cells and Light-Emitting Diodes



In solar cell applications, optical illumination is steady, and dc current  $I_{PH}$  is generated. The goal is to extract power from the cell, and the *i-v* characteristics are plotted in terms of cell current and cell voltage. For a solar cell to supply power to an external circuit, the  $I_{C}V_{C}$  product must be positive, and the cell should be operated near the point of maximum output power  $P_{\text{max}}$ .

Light-Emitting Diodes (LEDs) use recombination processes in the forward-biased *pn* junction diode to produce light. When a hole and electron recombine, an energy equal to the bandgap of the semiconductor is released as a photon.

**Jaeger/Blalock 4/29/11**



## End of Chapter 3

**Jaeger/Blalock 4/29/11**

**Microelectronic Circuit Design, 4E McGraw-Hill**