9A DC MODELS FOR BIPOLAR TRANSISTORS

INSTRUCTIONAL OBJECTIVES

Given a bipolar transistor, you should be able to:

a. Determine if the transistor is PNP or NPN;

b. Identify the base, collector, and emitter leads;

c. Measure the reverse breakdown voltage for the base-emitter junction;

d. Devise a circuit to plot the I_C vs. V_{CE} for different values of I_B;

e. Devise a circuit to plot I_B vs. V_{BE}.

f. Determine β_{DC}, I_{CEO}, R_{BB}, and V_0 and draw and label a dc model for a transistor.

1.0 PRELAB ACTIVITIES

1.1 Read Section 2.0. Given a bipolar transistor, write procedures to:

Identify the Base Lead and Type (NPN or PNP) using a suitable multimeter.

Identify the Emitter Lead. Assume the transistor is NPN and that the base lead is known.

1.2 Read Section 3.0. Complete the design of Figure 2.3, the zener diode test set.

Assume: $6\ V \leq V_{BR} \leq 8\ V$ (typical for bipolar transistors).

Limit the zener current to 6 mA. (Zener power dissipation will be less than 50 mW.)

Determine V_S^{MIN}:

Hint: To protect the zener from high forward currents, V_S is always positive.

Determine V_S^{MAX}:

Hint: Try V_{BR} = 8 volts and I_Z = 6 mA. Calculate V_S^{MAX}.
What is the maximum zener current if V_{BR} is 6 V?

Try V_{BR} = 6 volts and I_Z = 6 mA. Calculate V_S^{MAX}.
What is the maximum zener current if V_{BR} is 8 V?

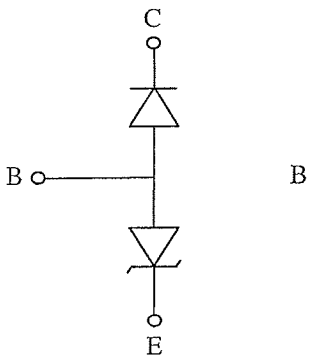
Which value of V_S^{MAX} properly limits all zener currents to 6 mA?

Sketch and Label the Test Set.

1.3 Skim Appendix 9-1, 9-2, and 9-3 which follow Experiment 9B. What are their titles?

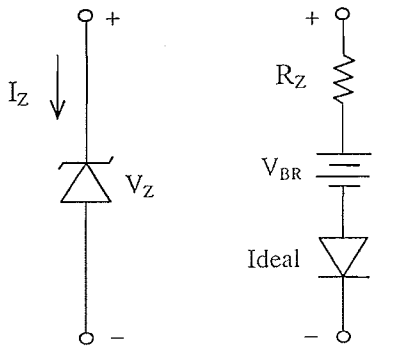
2.0 A MODEL FOR IDENTIFYING BIPOLAR TRANSISTORS

A circuit model for an electronic device provides a way of thinking about the device which allows the designer to treat the device as if it were composed of simple, easily understood components. A model for a device is chosen to serve a specific purpose. The models shown in Figure 2.1 are used to identify the transistor type and to determine the base, collector, and emitter leads.



a. NPN b. PNP

Fig. 2.1. Identification Model.



a. Zener b. Model

Fig. 2.2. Zener Diode Symbol and Reverse Breakdown Model.

An ohmmeter, having sufficient source voltage, can be used to determine the type of transistor and identify the base lead. (In Experiment 1, you learned to use an ohmmeter to check diodes.)

The "zener diode" connecting the base to the emitter has a breakdown voltage of 6 to 8 volts. The avalanche breakdown voltage for the "diode" connecting the collector to the base is much greater than 8 volts. Therefore, the emitter may be identified with a test set as shown in Figure 2.3.

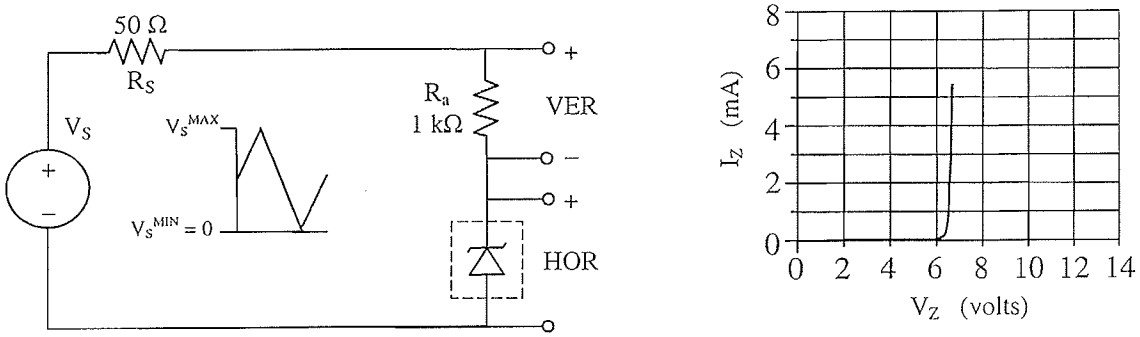


Fig. 2.3. A Test Set to Determine Reverse Breakdown Voltage of a Zener Diode.

3.0 DC MODELS FOR BIPOLAR TRANSISTORS

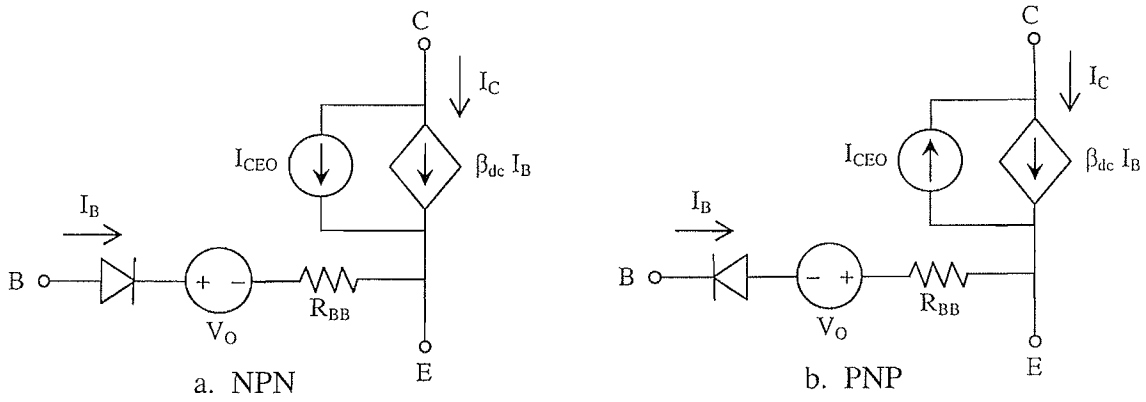


Fig. 3.1. DC Models Showing the Base-Emitter Diodes.

The models shown in Figure 3.1 include base-emitter diodes. These diodes indicate that current must flow into the base of the NPN and out of the base of the PNP. For the NPN, no base current will flow until V_{BE} is greater than V_O. For the PNP, no base current will flow until V_{BE} is less than V_O. Since these dc models are used for operating point design calculations, it is assumed that the base currents will have the correct polarity; therefore, the base-emitter diodes need not be shown.

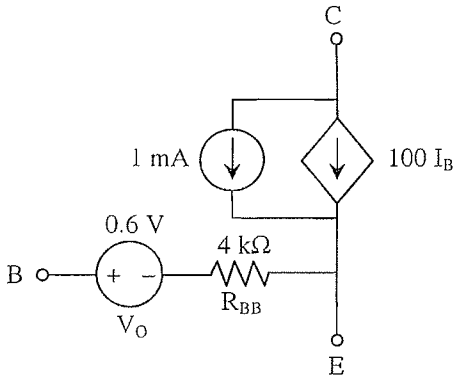


Fig. 3.2. DC Model for an NPN Transistor, $\beta_{dc} = 100$.

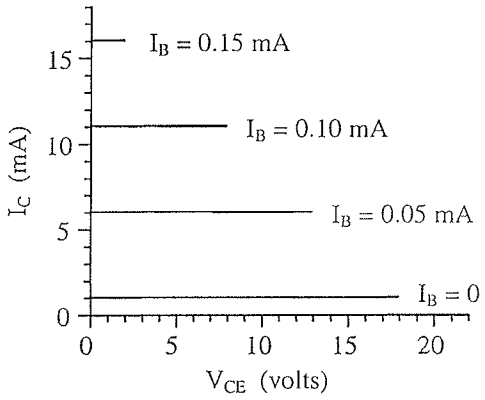


Fig. 3.3. Collector Characteristics for the DC Model in Figure 3.2.

Figure 3.2 shows a model for a particular transistor. The curves shown in Figure 3.3 are the *collector characteristics* of the transistor. Each curve (horizontal line segment) is the IV characteristic of the collector-emitter terminals for a constant base current. β_{dc} and I_{CEO} may be determined from the collector characteristics (and vice-versa):

I_{CEO} is the collector current that flows when $I_B = 0$. $I_{CEO} = 1$ mA. (Exaggerated for illustration)

From the model: $I_C = \beta_{dc} I_B + I_{CEO}$. Therefore, $\beta_{dc} = (I_C - I_{CEO}) / I_B$. $\beta_{dc} = 100$.

V_O and R_{BB} are determined from the input curve (I_B vs. V_{BE}). See Section 5, below.

4.0 A TEST SET TO OBTAIN: Collector Characteristics, I_{CEO}, and β_{dc}.

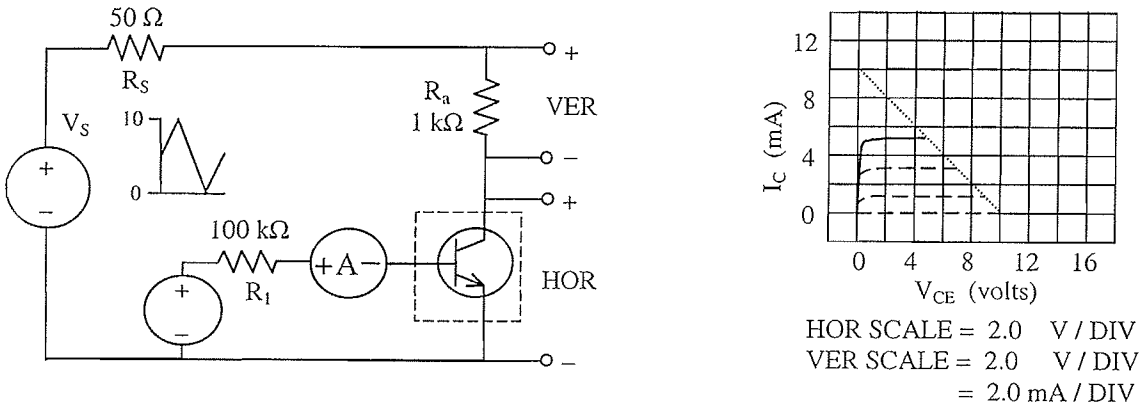


Fig. 4.1. A Test Set to Obtain Collector Characteristics of an NPN Transistor.

The test circuit of Figure 4.1 consists of two loops:

Collector Loop: V_S sweeps the collector supply from 0 to 10 V.

R_a limits the collector current and conveniently displays I_C at 1 volt/mA.

R_S is negligible.

Base Loop: V_{BB} adjusts the base current.

R_1 limits the base current.

I_B is measured with a VOM.

To obtain the solid characteristic curve shown in Figure 4.1, the base current is set to a desired value and V_S is automatically swept from 0 to a peak voltage of 12 V. The dashed curves represent characteristics obtained using other, evenly spaced, values of base current.

Determination of I_{CEO}. The dashed line along the $I_C = 0$ axis is I_{CEO}. This curve is obtained when $I_B = 0$. Since I_{CEO} is very small, considerable care is required to set the scope to a more sensitive scale and measure it.

Determination of β_{dc} is more complicated. Unlike the curves shown in Figure 3.3, the curves shown in Figure 4.1 are not, necessarily, evenly spaced. This uneven spacing indicates that β_{dc} is not a constant. This variation of β_{dc} across the operating region is dealt with by determining β_{dc} near the desired operating point. For example, the solid curve in Figure 4.1 passes through the point (V_{CE} = 5 V, I_C = 5 mA). To determine β_{dc} at that operating point:

From the model: $I_C = \beta_{dc} I_B + I_{CEO}$. Therefore, $\beta_{dc} = (I_C - I_{CEO}) / I_B$.

If I_B, the constant base current for the curve, is 33 μA (0.033 mA) and $I_{CEO} \approx 0$, then

$\beta_{dc} \approx (5 \text{ mA} - 0) / 0.033 \text{ mA}$

$\beta_{dc} \approx 150$ at the operating point (5 V, 5 mA).

5.0 A TEST SET TO OBTAIN: The Input Curve, V_O, and R_{BB}.

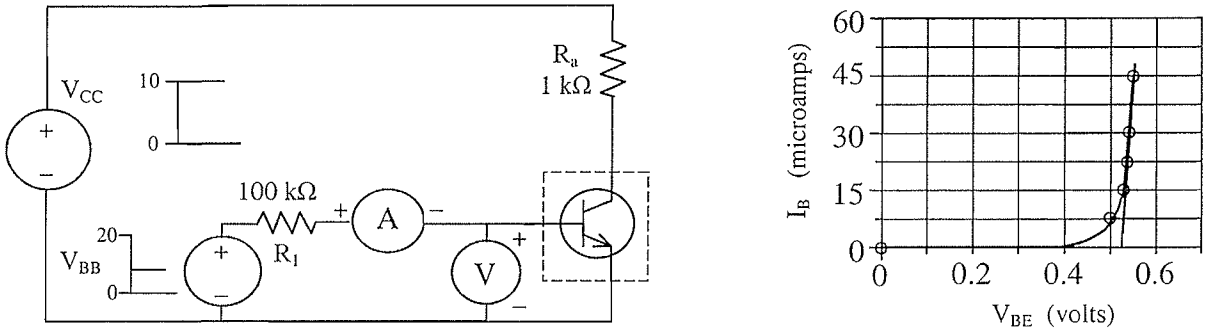


Fig. 5.1. A Test Set to Obtain the Input Characteristics of an NPN Transistor.

The test circuit of Figure 5.1 consists of two loops:

Collector Loop: V_{CC} is held constant at 10 V

R_a limits the collector current.

Base Loop: V_{BB} adjusts the base current.

R_1 limits the base current.

I_B is measured with a VOM.

V_{BE} is measured with a DMM.

To create the graph, each point (V_{BE}, I_B) is plotted and the curve is sketched in.

Determination of V_O. Since the desired operating point (V_{CE} = 5 V, I_C = 5 mA) lies on the curve for a constant base current of 33 μA (0.033 mA), the straight line model is drawn tangent to the input curve at that point. See Figure 5.1. This line intersects the $I_B = 0$ axis at V_{BE}= 0.52 volts. Therefore, V_O = 0.52 volts.

Determination of R_{BB}. R_{BB} is the inverse slope of the straight line model. To choose convenient points for the calculation, it is noted that the line passes through (0.55 V, 45 μA) and (0.52 V, 0 μA). Then, the inverse slope is computed:

$$R_{BB} = \frac{\Delta V_{BE}}{\Delta I_B} \approx \frac{0.55\,V - 0.52\,V}{45\,\mu A - 0\,\mu A} \approx \frac{0.07\,V}{45\,\mu A} \approx 1555\Omega$$

6.0 SUMMARY: THE DC MODEL FOR THE TESTED TRANSISTOR

From the Output Curves (Section 4.0): $\beta_{dc} \approx 150$ and $I_{CEO} \approx 0$ mA.

From the Input Curves (Section 5.0): $V_O \approx 0.52$ V and $R_{BB} \approx 1555\ \Omega$.

The dc model is a drawing, similar to Figure 3.2 labelled with these parameters.

7.0 EXERCISES

7.1 Your procedure from Prelab 1.1 describes how to test a bipolar transistor to determine if it is PNP or NPN and identify its leads. Test your procedure on a 2N3702 and a 2N3704. If necessary, rewrite the procedure. Make drawings that show the leads of these transistors.

7.2 Design a test set to safely determine which "diode" in a transistor is a 6 to 8 volt zener diode. Write a procedure to identify the emitter lead assuming the base lead and type are known. Test your procedure on a 2N3702 (PNP) and a 2N3704 (NPN). Complete the drawings identifying the leads of these transistors.

7.3 Your TA will provide you with a mystery transistor. Determine if it is an NPN or a PNP. Identify the base, collector, and emitter leads.

7.4 Construct the test set shown in Figure 4.1. Use the test set to test a 2N3704.

NOTE: Use the HP33120 Function Generator to generate V_S.

Adjust the AMP (Amplitude) of the triangle wave to 10 V peak to peak.

Adjust the OFFSET to 5.00 V.

(The HP 33120 limits its outputs to ± 10.00 V.)

a. Plot the family of collector characteristic curves for $I_B = 0$, 15, 30, and 45 μA.

b. Determine β_{dc} for the transistor at the operating point: $V_{CE} = 5$ V and $I_C = 5$ mA.

Hint: Adjust the base current to obtain a collector characteristic curve that passes through this operating point. Assume $I_{CEO} \approx 0$.

c. Determine I_{CEO} for the transistor. I_{CEO} will be very small.

Hint: Remove all connections from the base lead. I_B must then be 0.
Increase the sensitivity of the scope vertical.

7.5 Construct the test set shown in Figure 5.1. Test the 2N3704 used in 7.4 above.

a. Make a table of I_B vs. V_{BE} for $I_B = 0$, 7.5, 15, 22.5, 30, and 45 μA.

For best results, use the Simpson VOM for the ammeter. Set the Simpson to its 50 μA range, + DC polarity, and use the 50 μA and COMMON input jacks. Use a DMM for the voltmeter.

b. Sketch the input curve and determine V_O and R_{BB}. See Section 5.0.

7.6 Draw and label the dc model of the transistor using the parameters determined above.

7.7 Reserve this transistor for use in future Experiments.