5 PRECISION GAIN AMPLIFIER DESIGN

INSTRUCTIONAL OBJECTIVES See Appendix 5-1 attached.

Upon completion of this experiment you should be able to design, build, and test a single transistor amplifier that will meet a provided set of specifications using any 2N3904 transistor.
Satisfactory performance of this objective includes the following:

1. THEORY. Explain thoroughly the basis for selection of all non-specified components. Use your own words and cite your reference(s). Use the terms and notation defined in Section 3. How do you know that your design will meet the requirements for any 2N3904 transistor?
2. DESIGN a precision gain amplifier to interface a specified sensor to a specified load. Use the nominal 2N3904 parameters (provided) to determine the:
   a. Operating Point to achieve the required transistor gain and output swing;
   b. Bias Resistors to achieve the operating point and input resistance;
   c. Capacitors to achieve the required Low Frequency Corner (lower 3 dB frequency).
3. CONSTRUCT and TEST the amplifier to verify that the:
   a. Operating Point, Mid-band Gain, and Output Swing are as designed;
   b. Low Frequency Corner is as designed.
4. RESULTS. Perform measurements to prove that the amplifier works as specified.
   a. Obtain the results requested in Section 3.0, below;
   b. Submit a copy of your laboratory results to your TA at the end of the period. That includes a copy of your laboratory notebook and oscilloscope displays;
   c. Present your results in your formal report per Appendix 5-1.
5. DISCUSS how you revised the first circuit to arrive at the final circuit.
6. ANALYSIS. Discuss how changing each resistor would affect the bias point and output signal.
7. CONCLUSIONS. Compare expected results to theoretical results. Other conclusions might include proposed improvements and discussions of the limitations of the circuit.

1.0 PRELAB ACTIVITIES

1.1 Read the Background Section and the Appendices.

1.2 Per Section 3.1, write the theory and preliminary design in your lab notebook.

1.3 Per Section 3.2, record the result of your simulation in your lab notebook. Note that you will need to attach your simulation to your final report.

2.0 BACKGROUND FOR THE PROBLEM

Figure 2.1 shows an amplifier that interfaces a sensor to a signal processing system that has a 100 kΩ input resistance. Design the amplifier so that it will work for every 2N3904 NPN transistor.

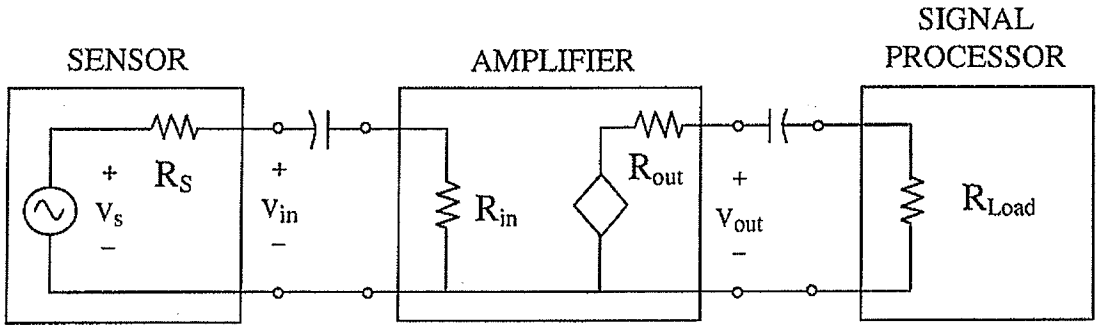

Fig. 2.1. Sensor and amplifier driving a signal processing system.

Specifications:

System:

A_{VS}	≈ 10	$\lvert v_{out} \rvert / \lvert v_S \rvert = 10 \pm 0.5$ with 100 kΩ load.

Source:

V_S^{max}	≦ 0.2 Vpp	(nominal maximum, 100 Hz – 10 kHz).
R_S	= 1 kΩ	(± 10 %)

Amplifier

V_{CC}	= 6.0 V	(a single supply)
R_{in}	= 10 kΩ	
R_{out}	= 2.2 kΩ	
R_{load}	= 100 kΩ	
ΔV_{out}	= 2 Vpp	(undistorted output signal)
Minimum 3 dB Bandwidth		30 Hz to 100 kHz. 30 Hz is the Lower 3db Corner.[1]

2N3904 NPN transistor:

$\beta_{DC} \approx \beta_0 \approx$	130	(nominal value assumed for the region of interest).
$V_{BE(on)} =$	0.60V	(for model incorporating R_{BB}).
$V_{CE(SAT)} =$	0.2 V	(for $I_C = 1$ mA)
f_T =	300 MHz	at $I_C = 10$ mA and $V_{CE} = 20$ V.

Special Requirements for ECE208:

C1 + C2 ≦ 100 μ	From Kit Values.
R_1, R_2, R_C, R_E	From Kit Values (series or parallel combinations, ok)

[1] A "*3 dB corner*" is a frequency for which the magnitude of the voltage gain is 0.707 times the magnitude of the mid-frequency voltage gain. For this experiment your "Upper 3dB Corner" will be well above 100 KHz.

3.0 SUMMARY OF THE PROBLEM. (See Jaeger, 13.6 thru 13.8)

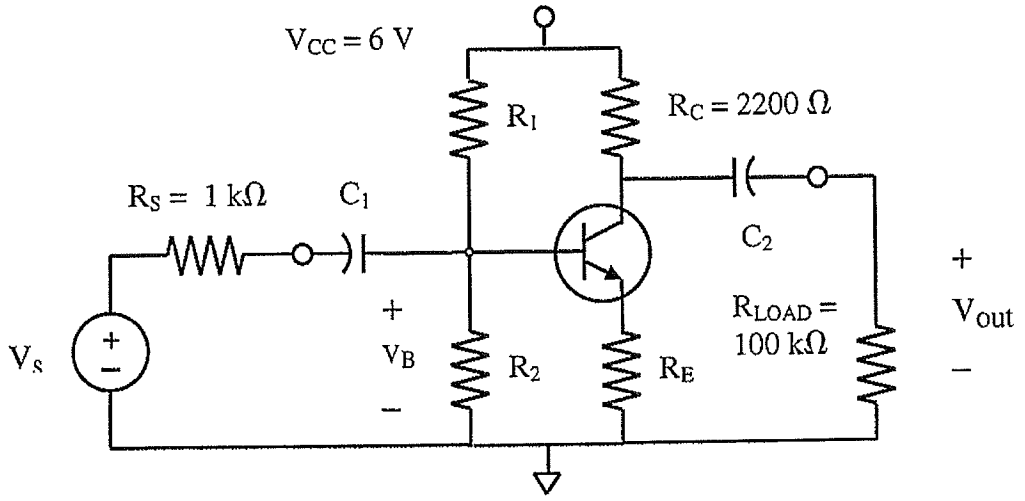

Fig. 3.1. Amplifier Circuit For Experiment 5

3.1 Preliminary Design (Refer to Section 2.0 for specifications and requirements.)

a. Draw a schematic of the circuit in your laboratory notebook.
b. Label all components with the labels as above.
c. Select an operating point and provide a clear, concise, and compelling technical explanation of how and why you selected that particular operating point.
d. Show complete hand calculations of R_1, R_2, R_E and any other components that affect the operating point. Clearly indicate the final results of these calculations by enclosing them with a label in a box.
e. Determine capacitors C_1 and C_2 so that the low-frequency 3 dB corner frequency is less than 30 Hz.

3.2 Development of Final Design

a. Using PSpice, MatLab, or any other means, simulate your design to show that your design meets the gain and swing requirements for any 2N3904.
b. Attach your simulation to your formal report as an appendix.

3.3 CONSTRUCT and TEST the amplifier. (Diagram your circuit design.)

a. Construct the circuit. (Add a 1 kΩ resistor to simulate the source.)
b. Verify the circuit. For each of several 2N3904 transistors, use a 0.2 Vpp triangle wave input signal to obtain and label oscilloscope plots that:
   i) Show $(V_{CE})_Q$ and $(I_C)_Q$
   and
   ii) Show that the undistorted output signal swing is 2 Vpp and that the system gain is 10 ± 0.5.
c. For one 2N3904, plot the frequency response from 1 Hz to 10 MHz. Determine the low frequency 3 dB corner frequency.
d. Compare your results to the expected results.

4.0 A SOLUTION TO CONSIDER (See Jaeger, 13.6 thru 13.8)

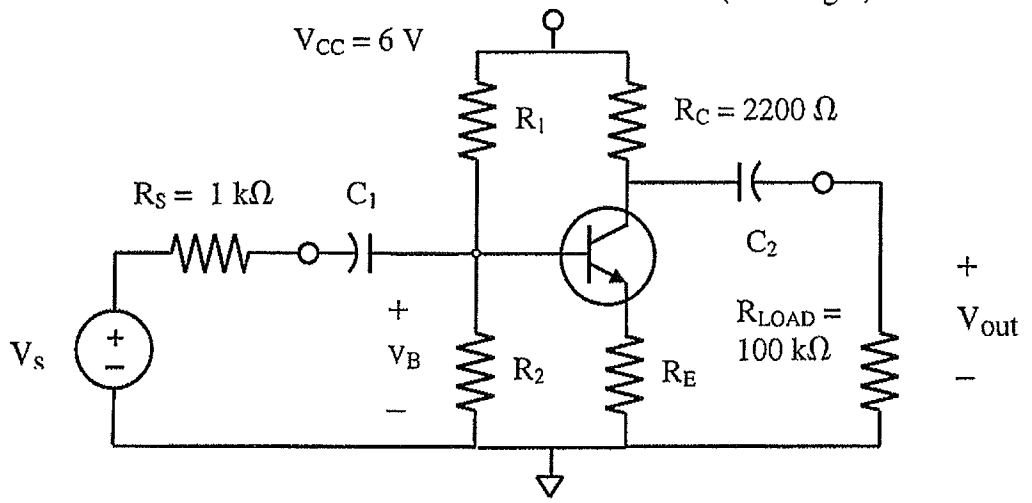

Fig. 3.1. Amplifier Circuit For Experiment 5 (repeated here)

4.1 GETTING STARTED – Preliminary Design:

a. Draw the schematic (above). Label all components.

b. The input impedance of common emitter amplifier is to be 10 kΩ; therefore, some of the input signal will be lost across R_S. Since the system gain is to be -10, the gain of the common emitter, $|v_{out}| / |v_B|$, needs to approximately -11. Why?

4.2 BEGIN WITH THE OUTPUT CIRCUIT – Determine R_E, $(V_{CE})_Q$, $(I_C)_Q$.

a. The collector loop equation is: $V_{CC} \approx (V_{CE})_Q + (I_C)_Q R_C + (I_C)_Q R_E$; (1)
therefore, from $6\text{ V} = (V_{CE})_Q + (I_C)_Q\, 2200 + (I_C)_Q R_E$, we can estimate that $(V_{CE})_Q \approx 3$ volts and that $(I_C)_Q \approx 1$ mA. Why? Then, $g_m \approx 40$ mS.[2] Why?

b. To determine R_E, we can apply our estimate of g_m to Jaeger Equation 13.51 which gives the magnitude of the gain for this common emitter amplifier configuration as $g_m R_C/(1+g_m R_E)$. In order to achieve a system gain of 10, the magnitude of the amplifier gain needs to be 11. Therefore, $R_E \approx [\,(R_C/11) - (\,1/g_m\,)\,]$.

c. The maximum voltage swing will occur when $(V_{CE})_Q \approx (I_C)_Q R_C$. Why?
Then, find $(I_C)_Q$ using this fact, the estimate of R_E, and the saturation voltage:

$$V_{CC} - V_{CE(SAT)} \approx (I_C)_Q R_C + (I_C)_Q R_C + (I_C)_Q R_E . \quad (2)$$

Using $6 - 0.2 = (I_C)_Q (\,2 R_C + R_E\,)$ yields $(I_C)_Q$ and $(V_{CE})_Q$.

4.3 INPUT CIRCUIT – Select R_1 and R_2 to bias the transistor at the operating point.

a. The input resistance into the base of the transistor: Jaeger's Equation 13.48 is:
$R_{iB} = r_\pi + (\beta + 1)R_E$ so it is safe to consider $R_{iB} > (\beta + 1)R_E$.

b. Select $R_1 \| R_2$, then R_1 and R_2 to bias the transistor for $(V_{CE})_Q$ and $(I_C)_Q$. Remember, the input resistance to the amplifier is to be greater than 10 kΩ and that means: $R_{iB} \;\|\; (R_1 \| R_2) > 10\ k\Omega$.

c. Since $(V_B)_Q = (V_E)_Q + V_0$ and $(V_E)_Q \approx R_E \times (I_C)_Q$, R_1 and R_2 may be determined.

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[2] $g_m \approx I_C / V_T \approx 40\, I_C$ amps/volt $= 40\, I_C$ Siemens. The unit mS means milli-siemen.

APPENDIX 5-1: FORMAL REPORT REQUIREMENTS

Experiment 5 should be presented in a formal style. It is preferred that the report be written in the 3rd person, past tense and focused on the work that was done, not who was doing it. It must be typed using double spacing. Figures can be drawn using the computer or neatly by hand. Equations must be typed. Be sure to check your spelling and grammar; part of your grade will be based on them. If you need help with your writing, the web site at "http://owl.english.purdue.edu" may be used to get tutorial help and fairly prompt information.

Your report should include the following sections:

1. **Title Page.** This page should contain the report title, your name, your lab partner's name, the day and time that your laboratory class meets, and the date of the report.
2. **Table of Contents.** The Table of Contents for this manual may be used as an example.
3. **Abstract.** The required abstract is a brief summary written in 3rd person, past tense. This section should be exactly one paragraph comprised of four to eight sentences. The abstract should answer these four questions:

   What was the purpose of the work?
   What was done?
   What was found?
   What was concluded?

   Only material germane to these questions is acceptable in your abstract.
   Part V, Page 6, of this manual provides examples of **good** and **bad abstracts**.
4. **Introduction.** This section should state the problem and, briefly, describe your solution.
5. **Theory.** As if you were teaching it, present the way your circuit works. Step-by-step, from a starting point to the end products, describe the signals and signal processing. Provide numbered equations to describe the signal processing steps. These equations will be the basis for the calculations given in the design section. Refer to the complete circuit diagram and graphs determined in the design section. Discuss how changing each circuit component would affect the bias point and the output signal.
6. **Design.** Refer to the equations in the theory section to make initial calculations for the values of circuit elements. If you "choose" a value, explain why you choose *that* value. Show a complete circuit diagram labeled with initial values. Provide graphs and values of expected system signals based on the equations given in the Theory section.
7. **Results.** Describe what happened when you first built and tested your initial circuit and provide oscilloscope plots and other data, if appropriate. If you change any component values to achieve the desired performance, explain why here. Be sure to include graphs that are needed to show your final circuit performing within specifications. Compare your expected results (Design Section) with your actual results.
8. **Conclusions.** A conclusion is a judgment based on facts in evidence. State, specifically, that the circuit did (or did not) perform to within the x % requirement. Conclusions, such as suggestions for improvement or explanations of failure are of great value to others who read your report. Be sure they are based on facts in evidence.
9. **Appendix.** Simulations. (ECE255 Spice Design Project #2 simulations are acceptable.)

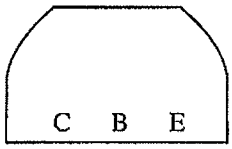
APPENDIX 5-2: DATA SHEET FOR 2N3903 AND 2N3904.

NPN Silicon
General Purpose Switching and Amplifier Transistors

------ABSOLUTE MAXIMUM RATINGS -------

at 25 C Free-Air Temperature (unless noted)

Collector-Base Voltage ..... 60 V
Collector-Emitter Voltage (Base open) ..... 40 V
Emitter-Base Voltage ..... 6 V
Total Dissipation (25 C Free-Air) See Note 1 ..... 360 mW
Collector Current ..... 200 mA
Junction Temperature (Operating) ..... +150 C
Lead Temperature 1/6 inch from case for 10 sec ..... +260 C
Storage Temperature Range ..... -55 C to +150 C



BOTTOM VIEW

ELECTRICAL CHARACTERISTICS at T_{air} = 25 C (unless otherwise noted)

			2N3903		2N3904		
Parameter	Symbol	Test Conditions	Min	Max	Min	Max	Unit
Collector-Base Breakdown Voltage	$V_{CBO}(BR)$	I_C = 10 µA, I_E = 0	60	–	60	–	V
Collector-Emitter Breakdown Voltage	$V_{CEO}(BR)$	I_C = 1 mA, I_B = 0 (Note 2)	60	–	60	–	V
Emitter-Base Breakdown Voltage	$V_{EBO}(BR)$	I_E = 10 µA, I_C = 0	6	–	6	–	V
Collector Cutoff Current	I_{CO}	V_{CE} = 30 V, V_{BE} = -3 V	–	50	–	50	nA
Base Cutoff Current	I_{BO}	V_{CE} = 30 V, V_{BE} = -3 V	–	50	–	50	nA
Static Forward Current Transfer Ratio	h_{FE}	V_{CE} = 1 V, I_C = 100 µA	20	–	40	–	–
		V_{CE} = 1 V, I_C = 1 mA	35	–	70	270	–
		V_{CE} = 1 V, I_C = 10 mA (Note 2)	50	150	100	300	–
		V_{CE} = 1 V, I_C = 50 mA (Note 2)	30	–	60	–	–
		V_{CE} = 1 V, I_C = 100 mA (Note 2)	15	–	30	–	–
Collector-Emitter Saturation Voltage	$V_{CE}(SAT)$	I_C = 10 mA, I_B = 1 mA (Note 2)	–	0.2	–	0.2	V
		I_C = 50 mA, I_B = 5 mA (Note 2)	–	0.2	–	0.2	V
Base-Emitter Saturation Voltage	$V_{BE}(SAT)$	I_C = 10 mA, I_B = 1 mA (Note 2)	0.65	0.85	0.65	0.85	V
		I_C = 50 mA, I_B = 5 mA (Note 2)	–	0.95	–	0.95	V
Small Signal Parameters							
Small Signal Current Gain	h_{fe}	V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	50	200	60	230	–
		V_{CE} = 20 V, I_C = 10 mA, f = 100 MHz	2.5		3.0		–
Voltage Feedback Ratio	h_{re}	V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	0.1	5	0.5	8.0	$x10^{-4}$
Input Resistance	h_{ie}	V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	0.5	8	1.0	10	kΩ
Output Admittance	h_{re}	V_{CE} = 10 V, I_C = 1 mA, f = 1 kHz	1.0	40	1.0	40	µmhos
Output Capacitance	C_{ob}	V_{CB} = 5.0 V, I_E = 0, f = 1 MHz	–	4.0	–	4.0	pF
Input Capacitance	C_{ib}	V_{EB} = 0.5 V, I_C = 0, f = 1 MHz	–	8.0	–	8.0	pF
Cutoff Frequency	f_T	V_{CE} = 20 V, I_C = 10 mA, f = 100 MHz	250		300		MHz