ID\# $\qquad$
Name $\qquad$
EE255 Exam 2 October 12 ${ }^{\text {th }}, 2000$
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The exam consists of 16 multiple choice questions and 4 workout problems. Record the answers to the multiple choice on this page. Return the entire exam. There will be no partial credit for the multiple choice portion. There may be partial credit for the workout problems and hence show all your work.

## DO NOT BEGIN UNTIL INSTRUCTED TO DO SO

| 1) | a | b | c | d | e |
| :--- | :--- | :--- | :--- | :--- | :--- |
| 2) | a | b | c | d | e |
| 3) | a | b | c | d | e |
| 4) | a | b | c | d | e |
| 5) | a | b | c | d | e |
| 6) | a | b | c | d | e |
| 7) | a | b | c | d | e |
| 8) | a | b | c | d | e |
| 9) | a | b | c | d | e |
| $10)$ | a | b | c | d | e |
| $11)$ | a | b | c | d | e |
| $12)$ | a | b | c | d | e |
| $13)$ | a | b | c | d | e |
| $14)$ | a | b | c | d | e |
| $15)$ | a | b | c | d | e |
| $16)$ | a | b | c | d | e |

1. Given the MOSFET biased as shown below, in which region will the device operate ? $V_{T}=|1|$

(a) Saturation
(b) Linear
(c) Cut-off
(d) active
(e) inverse active
2. Given the MOSFET biased as shown below, in which region will the device operate ? $\mathrm{V}_{\mathrm{T}}=|1|$

(a) Saturation
(b) Linear
(c) Cut-off
(d) active
(e) inverse active
3. The transistor below has $K_{p}=2 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|3|, \mathrm{V}_{\mathrm{A}}=6 \mathrm{~V}$, and $\mathrm{V}_{\mathrm{B}}=10 \mathrm{~V}$ What is the value of $\mathrm{I}_{\mathrm{D}}$ ?

(a) 0 mA
(b) 2 mA
(c) 6 mA
(d) 16 mA
(e) 18 mA
4. For the transistor biased as shown in the circuit below, find the value of $\mathrm{I}_{\mathrm{D}}$ ? Assume that $R_{D}$ is such that the device is in saturation.
$\mathrm{K}_{\mathrm{N}}=0.2 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|3|$

(a) 3.2 mA
(b) 6.4 mA
(c) 12.8 mA
(d) 25.6 mA
(e) 51.2 mA
5. For the circuit shown above in problem 4 , Find $R_{D}$ such that the transistor is in saturation?
(a) $90 \Omega$
(b) $180 \Omega$
(c) $220 \Omega$
(d) $360 \Omega$
(e) $450 \Omega$
6. For the circuit show below, find the value of $\mathrm{V}_{\mathrm{DS}}$ ? $\mathrm{K}_{\mathrm{N}}=2 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|1|$

(a) 0.5
(b) 1
(c) 4
(d) 5
(e) 7
7. For the circuit shown below, when $\operatorname{Vin}=5 \mathrm{~V}$ and Vout $=0.2 \mathrm{~V}$, find the $\mathrm{I}_{\mathrm{D}}$ ? $\mathrm{K}_{\mathrm{N}}=0.1 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|2|$

(a) 0.11 mA
(b) 0.22 mA
(c) 0.33 mA
(d) 0.44 mA
(e) 0.55 mA
8. Given the circuit shown in the figure below and the output characteristics of the transistor shown in the adjacent figure, what is the value of $I_{D}$ and $V_{D S}$ for the transistor?
(a) $\mathrm{I}_{\mathrm{D}}=8 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS}}=8 \mathrm{~V}$, (b) $\mathrm{I}_{\mathrm{D}}=16 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS}}=6 \mathrm{~V}$, (c) $\mathrm{I}_{\mathrm{D}}=6 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS}}=8 \mathrm{~V}$, (d) $\mathrm{I}_{\mathrm{D}}=$ $24 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS}}=4 \mathrm{~V}$, (e) $\mathrm{I}_{\mathrm{D}}=8 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS}}=6 \mathrm{~V}$
9. What is the input impedance of the circuit shown below;

(a) $\mathrm{R}_{1}$
(b) $\mathrm{R}_{1} \| \mathrm{R}_{\mathrm{L}}$
(c) $1 / g_{m}$
(d) $R_{1}\left\|R_{L}\right\| 1 / g_{m}$
10. For the MOS circuit shown below, determine the value of $\mathrm{I}_{\mathrm{D} 2}$ and $\mathrm{V}_{\mathrm{DS} 2}$ ? Assume that $\mathrm{K}_{\mathrm{N} 1}=\mathrm{K}_{\mathrm{N} 2}$.

(a) $\mathrm{I}_{\mathrm{D} 2}=2 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS} 2}=5 \mathrm{~V}$
(b) $\mathrm{I}_{\mathrm{D} 2}=2 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS} 2}=8 \mathrm{~V}$
(c) $\mathrm{I}_{\mathrm{D} 2}=1 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS} 2}=4 \mathrm{~V}$
(d) $\mathrm{I}_{\mathrm{D} 2}=1 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS} 2}=8 \mathrm{~V}$
(e) $\mathrm{I}_{\mathrm{D} 2}=3 \mathrm{~mA}, \mathrm{~V}_{\mathrm{DS} 2}=8 \mathrm{~V}$
11. Given a hypothetical 3 terminal device, the current voltage relationships are shown below. Determine the transconductance for this device. Input is taken at node 1 and output is taken at node 2 .
$\mathrm{I}_{23}=\mathrm{AV}_{13}+\mathrm{BV}_{13}{ }^{2}+\mathrm{CV}_{23}$

(a) $2 \mathrm{~A}+\mathrm{BV}_{13}$
(b) $A V_{13}+B$
(c) $\mathrm{A}+2 \mathrm{BV}_{13}$
(d) $\mathrm{BV}_{13}+\mathrm{C}$
(e) $2 B V_{13}+C$
12. The numerical value of the small signal voltage gain of the amplifier shown below is; $\mathrm{K}_{\mathrm{N}}=1 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|2|, \lambda \mathrm{n}=0$. Assume the device is in saturation.

(a) +16
(b) -16
(c) +8
(d) -8
(e) -32
13. The input impedance for the circuit shown below, assuming that the transistor is biased in saturation, is;

(a) $\mathrm{Rss} \| \mathrm{R}_{1}$
(b) $\mathrm{Rss}+\mathrm{R}_{1} \mid 1 / \mathrm{g}_{\mathrm{m}}$
(c) $\mathrm{Rss}\|\mathrm{R} 1\| 1 / \mathrm{g}_{\mathrm{m}}$
(d) $\mathrm{Rs}\left\|\mathrm{R}_{1}\right\| 1 / \mathrm{g}_{\mathrm{m}} \| \mathrm{R}_{\mathrm{D}}$
(e) $1 / g_{m}$
14. Determine the regions for operation for the transistors in the circuit shown below; $\mathrm{K}_{\mathrm{N}}=1 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=|1|$

(a) Q1 linear, Q2 Saturation
(b) Q1 Saturation, Q2 Saturation
(c) Q1 Saturation, Q2 Linear
(d) Q1 Cut-off, Q2 Linear
(e) Q1 linear, Q2 Cut-off
15. If the transistor is biased in saturation, changing Rs from 0 to $1 \mathrm{k} \Omega$ in the circuit below does the following;

(a) increases the magnitude of the ac voltage gain and lowers Rout
(b) increases the magnitude of the ac voltage gain and increases circuit stability
(c) decreases the magnitude of the ac voltage gain and increases circuit stability
(d) decreases the magnitude of the ac voltage gain and increases Rin
(e) does nothing to the magnitude of the ac voltage gain or Rin
16. A CMOS inverter circuit is shown below. In region 1 of the transfer curve, the transistors are in the following regions of operation;

(a) NMOS Saturation, PMOS Linear
(c) NMOS Saturation, PMOS Cut-off,
(e) NMOS Active, PMOS Passive

(b) NMOS linear, PMOS Saturation,
(d) NMOS Cut-off, PMOS Linear,

17-20 pertain to the circuit diagram below.

$\mathrm{K}_{\mathrm{N}}=0.1 \mathrm{~mA} / \mathrm{V}^{2}, \mathrm{~V}_{\mathrm{TH}}=1, \lambda=0$
17. Calculate the maximum value of $\mathrm{R}_{\mathrm{D} 1}$ so that Q 1 is in saturation.
18. Calculate Rs so that Q 2 is in saturation, and $\mathrm{I}_{\mathrm{D} 2}$ is 0.9 mA .
19. Draw the ac small signal equivalent circuit with the transistor models, and the DC transfer curve of the circuit.
20. Calculate the approximate numerical value of the ac small signal voltage gain.

