Wide-Band Packet Radio for Multipath Environments

JEFFREY H. FISCHER, MEMBER, IEEE, JOHN H. CAFARELLA, MEMBER, IEEE, CHARLES A. BOUMAN, GERARD T. FLYNN, MEMBER, IEEE, VICTOR S. DOLAT, AND RENE BOISVERT, MEMBER, IEEE

Abstract—**A direct-sequence spread-spectrum packet radio is described which has versatile signal processing and local control capabilities designed to support the functions required of a robust mobile communications network. Noteworthy capabilities include 11 selectable data rates with accurate range measurements in a fading multipath channel. The radio employs a hybrid analog/digital signal processor and nonrepeating spreading codes for suppression of intersymbol interference and jamming. It incorporates two sets of monolithic surface-acoustic-wave convolvers as programmable matched filters with time-bandwidth products of 64 and 2000. The analog matched filters are coupled with binary postprocessing for the functions of detection, RAKE demodulation, and ranging measurements over a wide multipath spread. The data rate can be selected, in response to varying channel conditions, from 1.45 Mbits/s down to 44 bits/s with an almost ideal tradeoff in signal processing gain from 18 dB up to 61 dB prior to multipath combining.**

I. Introduction

THE need for high performance and flexibility in digital communications has caused considerable interest in packet radio networks [1]–[4]. Packet radio usually implies a data network (although it is sometimes applied to digitized voice) which uses multiple repeater sites shared among the users to forward information between two points in the network. Each message is parsed into packets of data which are individually routed through the network and recombined at the destination. The flexible resource sharing obtained with packet switching, combined with versatile computer control of radios for networking, makes packet radio well suited to communication between large numbers of computers.

Ground-to-ground radio communications is often severely hampered by multipath. Narrow-band communications are typically subject to multipath fades of 20–30 dB in an urban environment. Often these losses are compensated by increasing the transmit power, which can exacerbate interference in a network environment. Alternatively, direct-sequence spread-spectrum communications provide an inherent frequency diversity which makes it highly resistant to multipath. Additionally, the correlation peaks that result from the demodulation of the spread-spectrum signal at the receiver are readily detected allowing the multipath channel to be estimated and diversity combined to improve reception [5]. Direct-sequence spread spectrum overcomes the problems of communicating over widely varying multipath channels.

This paper describes the development of a demonstration packet radio which exploits advanced signal processi technology for high performance mobile network communic tions. The network must withstand multipath and interferen and maintain privacy. In this paper, the discussion regardi anti-multipath processing will be highlighted. More deta regarding the operational protocols and network requireme are presented in [6].

The signal processing is based on surface-acoustic-wa (SAW) convolvers used as 100-MHz-bandwidth programm ble matched filters for demodulating the pseudonoise (P spread-spectrum waveform [7], [8], [9]. SAW convolve exhibit a number of noteworthy attributes, among which a the combination of large processing bandwidth and lar interaction time. These characteristics allow completely asy chronous-matched filter operation, thus alleviating the oft encountered problem of PN code acquisition time.

Another advantage is the programmability which allows t reference to be changed constantly at the full signal ban width. Thus, each data bit can have a new PN code. Amo the advantages of having a continuously changing PN code the multipath resistance when using high data rates. Data ra on the order of 1 Mbit/s and higher can suffer fr intersymbol interference in typical broadcast environments. this situation, the multipath generated from each bit exten into one or more successive data bits. The changing codes w decorrelate the intersymbol multipath between successive d bits.

Because of the requirements imposed by changing netw situations, it is desirable to provide a means for trading d rate for processing gain. Thus, in an environment with sev interference, the communication link could be restored employing a lower data rate to achieve the necessary incre in receiver processing gain. Two sets of SAW convolvers used in this radio, depending on data rate selection, providi 18 or 33 dB of processing gain. A hybrid correlator techni has been devised which combines convolvers functioning matched filters with full bandwidth binary-quantized integ tion [8] to further increase the processing gain when nec sary. The total processor provides data rates from 1.45 Mb s to 44 bits/s, with a nearly ideal trade of data rate processing gain from 18 dB to over 61 dB, thus allowing "graceful degradation" in severe conditions. Although it unrealistic to expect that the lowest data rates will support overhead required to maintain a mobile network, it does all for a realistic operation where a brief but essential mess must be communicated to a radio suffering severe chan difficulties.

The variability of multipath profiles between mobile us creates problems with data demodulation and with recei signal arrival time measurements. Techniques have b developed to sound out the multipath channel and perfo RAKE demodulation of the data [10]. Precise measurement time of arrival (TOA) and information on the time of trans are required in the network to determine the signal transit ti and the clock offset between radios. The transit time is u for interradio range measurements which allow the network determine the relative location of each of the radio nod

Paper approved by the Editor for Mobile Communication of the IEEE Communications Society. Manuscript received February 6, 1987; revised October 20, 1987. This work was supported by the Defense Advanced Research Projects Agency.

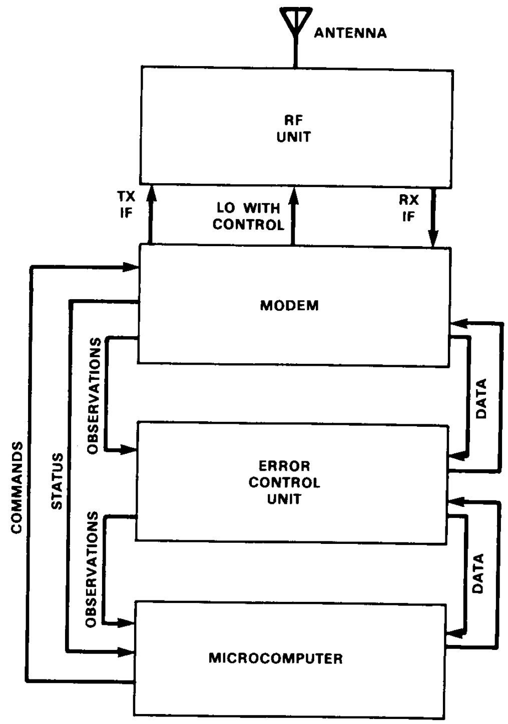
J. H. Fischer and J. H. Cafarella are with MICRILOR, Inc., Wakefield, MA 01880.

C. A. Bouman is with the Department of Electrical Engineering, Princeton University, Princeton, NJ 08544.

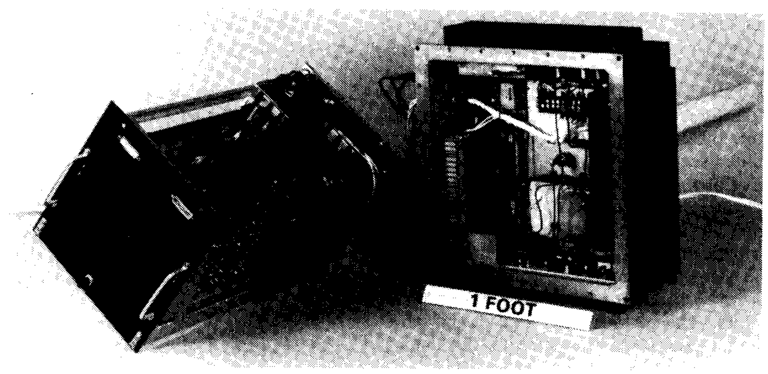
G. T. Flynn, V. S. Dolat, and R. Boisvert are with Lincoln Laboratory, Massachusetts Institute of Technology, Lexington, MA 02173.

IEEE Log Number 8820406.

0090-6778/88/0500-0564$01.00 © 1988 IEEE



(a)



(b)

Fig. 1. (a) Block diagram of the radio with the control interface on the left and the data interface on the right. (b) Photograph of the radio hardware. The L band RF unit is on the right. The other three units reside in the chassis on the left.

which must be constantly updated in a mobile network. In a diffuse multipath environment, the TOA will generally be incorrect because the line-of-sight propagation path will be blocked. Both coherent and noncoherent integration techniques have been developed for detecting leading multipath components which are too weak to be simply detected at the output of the matched filter. Detection of weak multipath precursors provides significant improvement in range-measurement accuracy. Anticipated multipath processing requirements are based in part on propagation measurements taken early in the packet radio program at Stanford Research Institute [11] and aspects of the architecture are based on results obtained by Turin [5], [12]. The L band and RF link parameters were taken from the DARPA experimental packet radio program [1].

The radio described combines a collection of unique features which together provide robust, private communications in spite of multipath, interference, and jamming. The number of controllable parameters and observable features is quite large, and it should be kept in mind that the ability to take advantage of all these features is beyond the state of the art of current network protocols. Substantial work will be required to understand how these radios can best to used to support tactical packet radio networks.

II. Radio Architecture

Fig. 1(a) shows a block diagram of the radio, which consists of an RF unit, a modem, an error control unit (ECU), and a microcomputer. A photograph of the hardware is shown in Fig. 1(b). The RF unit performs the required frequency translation and contains the AGC and transmit power control. It is designed to operate between the allocated experimental packet radio RF band centered at 1.8 GHz and the convolver IF band centered at 300 MHz. The modem exploits the SAW-based technology to provide multifunction spread-spectrum signal processing. It performs the modulation and demodulation between the baseband data from the ECU and the IF waveform from the RF unit, respectively. There are several data bit modulations used depending on data rate and channel conditions as discussed in later sections and the IF modulation used is minimum shift keying (MSK). The ECU performs convolutional encoding and sequential decoding [13], cyclic redundancy check, and data interleaving of baseband data between the microcomputer and the modem. The microcomputer runs low-level network algorithms, packetizes the messages, and sets up the local ratio activity, transferring data packets to and from the ECU. This paper will primarily discuss the design and operation of the modem.

During data transmission, a packet is sent from the microcomputer to the ECU to be encoded. The encoded data packet then goes to the modem where a data link level header is attached and the entire packet is modulated into the IF band. In the RF unit, the modulated packet is upconverted to the carrier frequency and transmitted. During receive, the signal enters the RF unit where it is downconverted to the IF band, normalized by automatic gain control, and directed to the modem. The modem synchronizes to the packet, determines the packet parameters [6], and demodulates the IF signal into baseband data bits which are sent to the ECU for decoding. The data link header, which describes the modulation and coding parameters of a packet, is stripped off in the modem so the type of signal processing, error correction, and packet length are known by the modem and ECU. From the ECU the decoded data packet is sent to the microcomputer for network level processing.

The time scale for radio control is divided into 10 ms control time slots that allow the microcomputer to read the radio status, change parameters, and generate activity in the radio [14]. In addition, the network uses these time slots to change spreading code seeds (PN start vector), control contention, and align global time of day. The modem must react to the control-time slot activity with much finer resolution and consequently implement radio utilities, such as transmit/receive prioritization, and perform packet communication. Interface logic allows bidirectional information flow between the network-level microcomputer and the modem signal-processing circuits. The modem may thus relay information regarding channel characteristics such as number of multipaths resolved for demodulation in a particular packet. In this way the channel statistics may be correlated with network level data such as the self-location information. Packets are typically 1000 bits long but can vary from 256 bits to over 8000 bits depending on network conditions.

III. Signal Processing

Comparison of Matched Filtering and Correlation

There are two receiver processes that are used under differing network conditions, creating two distinct operating modes of the radio. In general, the process of matched filtering the data bit provides a completely asynchronous method of demodulating the received signal. The process of correlation against an actively generated reference code [15] provides a synchronous method of demodulation. While matched filtering creates an output that is continuous in time representing all time relationships of the reference and the signal, correlation creates only one output sample, representing one value of the time relationship between reference and signal. As a consequence, a matched filter using convolvers requires simultaneous interaction with the entire reference waveform, whereas the correlator does not. Lowering the data rate for greater signal-processing gain in a matched-filter receiver require longer interaction time which is limited by available techn ogy. For example, a wide-band SAW devices have upper tin bandwidth product limits of about 2000 because the interacti time is typically limited to 20 μs for 100 MHz devices [1 [17]. On the other hand, higher processing gain in t correlator is readily accomplished by integrating over a long period of time [18].

A single correlator requires an accurate prior estimate of t arrival time of the signal for rapid acquisition. Alternatively bank of correlators running simultaneously can be operat each with a relative time shift of the waveforms incremen by the inverse of the bandwidth. Thus, a less accurat estimated arrival time may be accommodated by framing t expected time window with the correlator bank. For init detection, this correlator bank requires a total search ti which equals the uncertainty in receiver timing multiplied the processing gain, divided by the number of paral correlators in the bank of detectors. In the matched filter, the other hand, initial detection of a signal of unknown arri time is immediate once the signal passes completely throu the filter. Thus, the matched filter exhibits no code acquisiti problem.

The radio described here uses a receiver which functions the matched-filter model when that provides sufficient pr essing gain; otherwise, it uses a parallel-correlator mode. circumvent the correlator code acquisition problem wh using the very high-processing gain mode for initial detect the timing uncertainty is reduced by prescheduling the arri of packets. This prescheduled receive is treated as a spec case in the local control by the microcomputer. Af synchronizing to the earliest detectable multipath with matched filter (as described in a later section), the multip echos that are used for RAKE demodulation appear at output delayed in time. Alternatively, once detection l occurred for the correlator, the reference waveform and correlator bank are retimed to align the correlator bank w the multipath processing window. Sequential readout of correlator directly provides the multipath samples over a de spread similar to that of the matched filter.

The correlator is also used in a special packet format wh the modem asynchronously detects with the matched filt synchronizes, and then the data portion is further process with the correlator. As well as data demodulation, the m accurate range measurements are performed in this way.

The Hybrid Processor

A simplified block diagram of the signal processing in modem is shown in Fig. 2. It consist of a programma analog matched filter, an analog-to-binary interface, an digital postprocessor. The matched filter uses two 22 μs l convolvers or four 1.4 μs long convolvers, depending on d rate, to provide continuous input time coverage by alternat steering the time-reversed reference waveforms between e convolver. The multiple convolvers are required to implem the specific data-bit demodulations used in each data rate will be described in the analog processor section. T interface performs both coherent (I and Q) and envel detection creating several different 200 MHz bandwi binary-quantized input streams which are directed to digital processor which selects from among these fo particular operating mode. The different modes are introdu here and described in more detail later.

If there is sufficient input signal-to-noise ratio (SNR) digital processor performs the initial detection process dire on the output of the matched filter. Alternatively, if additio processing gain is needed, the binary integrator is used implement a correlator bank and initial detection is t performed at the integrator output, as indicated in Fig. Similarly, with sufficient signal input, RAKE processing n

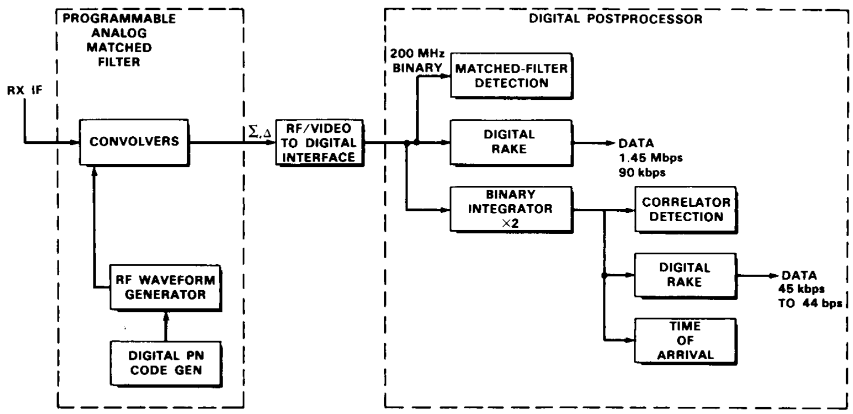


Fig. 2. The hybrid analog/digital signal processor is located in the modem. The analog processing (left) feeds the digital processing (right) through the analog-to-200 MHz binary interface. The block-labeled convolvers consist of two 22 μs-long and four 1.4 μs-long devices used in time-staggered fashion in order to process continuous input time at the for DPSK and orthogonal signaling with continuously changing, propagating reference codes.

be performed directly on the matched filter output as in the 1.45 Mbit/s and the 90 kbit/s data rates,while the flower input–SNR operation, binary integration will occur prior to RAKE processing. When RAKE is performed at the 90 kbit/s rate, the binary integrator is also used to perform background processing for TOA.

There are actually two binary integrator channels. For the extreme in receiver processing gain when conditions allow, correlation is performed coherently with in-phase and quadrature channels. Noncoherent processing at medium data rates also makes use of both channels, as discussed later; however, noncoherent processing at the lowest data rates uses only one channel. When the TOA processing is performed in a background mode to the 90 kbits/s data rate, only a single integrator channel is used to look for the low-level precursor. However, for the most accurate TOA processing, specialized packets are transmitted without data and coherent integration utilizing both channels are deployed to extract the precursor. These various modes of operation tend to complement each other. For example, when the single channel of the binary integrator performs background TOA for the 90 kbits/s data rate, part of the circuitry for the other channel is free to store the multipath profile used for the RAKE demodulation. In this manner, the wide range of operation is accomplished with surprisingly compact equipment.

The output of the analog matched filter is approximately the impulse response of the communication channel, since the multipath signals will occur as delayed convolution peaks. The input time resolution of the output multipath profile is 10.8 ns, corresponding to the reciprocal of the spreading bandwidth of the waveform. The binary RAKE processor [8], [9] noncoherently combines the multipath energy, within a processing window, to form a data decision. The accumulation of multipath energy can provide significant signal-processing gain. Although binary–digital RAKE is not as effective as maximal ratio combining, almost any process that adapts to the channel performs substantially better than a nonadaptive system [cf. 5, p. 347, Fig. 26]. The RAKE circuit described here is readily implemented in conjunction with the SAW convolvers.

The binary integrator accumulates many successive matched filter outputs on a sample-bin-by-sample-bin basis to extend the maximum 33 dB processing gain provided by the convolver. By selecting the number of matched filter outputs used in a binary integration, the modem uses a data bit with selectable duration, and thus energy, so as to attempt to optimize the tradeoff of throughput versus processing gain for varying channel characteristics. The hardware limit in this implementation is 1000 iterations, providing 30 dB of additional processing gain.

The analog preprocessing and binary postprocessing make it possible to overcome the limitations encountered when using either technology along. Analog signal processing components can handle very wide bandwidths, although they provide only modest processing gain, e.g., 33 dB, and dynamic range, e.g., 45 dB [20]. Convolvers with 100 MHz bandwidth perform the equivalent of 10^{11} digital arithmetic operations per second [21]. Digital processors, on the other hand, support large processing gains and dynamic ranges, but require excessive power for wide-band applications. By comparison, a 1982 technology analog–analog convolver implemented with digital design techniques operating at 40 Msamples/s with 4096 point FFT's [22] has been sized at 5600 W and 6000 chips. Single-chip analog–binary convolvers are available [23] with 20 MHz bandwidth and only 64 point capability. The overall digital capabilities are thus far below SAW convolver designs.

Fig. 3 shows the influence of analog processing used prior to binary processing when implementing a hybrid correlator. The binary integrator used along is particularly susceptible to non-Gaussian interference as can be seen in the left side of the curve when there is no analog preprocessing. However, any interference presented to the convolver input has Gaussian-like statistics at the convolver output because of the PN reference waveform, resulting in the near-Gaussian performance at the right side of the curve. Thus, in addition to, and more fundamental than the bandwidth advantage, analog preprocessing overcomes the problem of using a stand-alone binary integrator in a non-Gaussian channel [19]. (Multilevel digital quantization will recover some of this loss; however, it offers a serious hardware penalty [24].) The conclusion is that at least the first 20–30 dB of correlation gain should be done in analog before entering the binary–digital postprocessor.

Analog Processor

A diagram of the monolithic SAW elastic convolver [8], [9] is shown in Fig. 4(a). The input signal and time-reversed reference waveform are counterpropagated along a wave-guided region of a piezoelectric delay line. The resulting

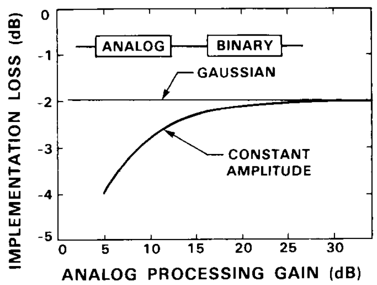


Fig. 3. Effect of analog processing gain on hybrid-correlator implementation loss. Note that with more than 25 dB of analog signal processing gain the binary integration is only 2 dB inferior to a fully analog approach.

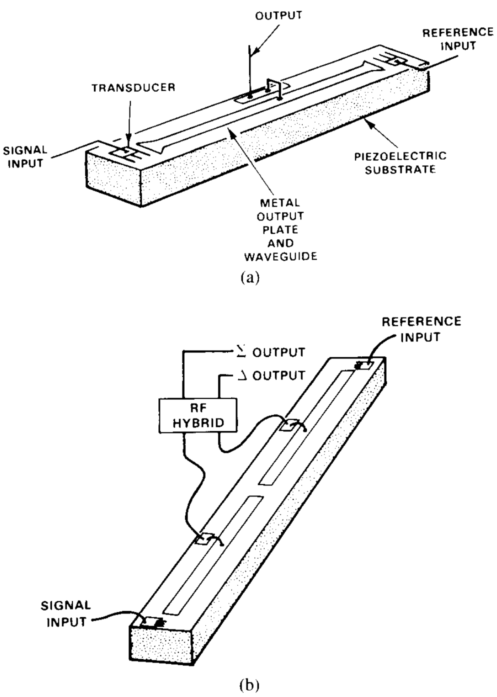


Fig. 4. (a) Simplified side view of a SAW convolver. The horn-shaped waveguide creates an acoustic-beam compression resulting in sufficient power level to drive the piezoelectric crystal into nonlinearity. (b) Simplified diagram of a DPSK convolver.

nonlinear acoustic-wave interaction creates an instantaneous product of the waveforms which is summed along a metal collecting plate to provide the convolution output. The processing gain of the convolver is the product of the interaction time of the convolver and bandwidth, referred to as the time-bandwidth product. The finest resolution output of the full-bandwidth PN code generator is referred to as a chip. The time-bandwidth product is also the number of chips per data bit, called the bandwidth-spreading factor. The waveform processed in the convolver is a 2048-chip section of a long m sequence generated at 92.5 Mchips/s, then MSK modulated onto a 300 MHz carrier [25]. The output is a function of the relative delay of the two waveforms, and since the two waveforms are counterpropagating the relative velocity is increased by a factor of two, resulting in a center frequency and bandwidth doubling at the convolver output. For the 92.5 Mchips/s input rate, the output digital-signal-processing c cuits must therefore be clocked at 185 MHz.

Data modulation on the PN-coded waveform is impl mented with differential phase transitions. Two concatenat convolvers formed with a segmented waveguide on o crystal, as shown in Fig. 4(b), are used to directly demodula a differential phase shift keyed (DPSK) signal [8], [19], [2 The outputs of each 11 μs convolver segment are combin coherently in an RF hybrid. When data creates a pha transition between two consecutive bits, the convolution pe appears at the difference port of the hybrid and only noi comes out of the sum port. If no phase transition is present, t output comes out of the sum port.

The spreading code is composed of serially aligned sectio of a much longer sequence which is generated using a 3-by start vector (PN seed). A new start vector is delivered to t modem from the microcomputer over the command interfa each 10 ms. At present the 92.5 MHz code generator is bas in ECL technology; however, most of these circuits will so be replaced by a highly parallel NMOS chip which has be fabricated at the DARPA MOSIS silicon foundry [27]. T MSK modulation is generated by offset PSK modulation weighted quadrature channels [28]. For the nominal 90 kbit data rate of the radio, 1024 chips of the PN sequence a transmitted per data bit. Two data bits worth of energy a used in each DPSK demodulation. The 1.45 Mbit/s high da rate is implemented using shorter convolvers with 64 chip per-bit binary orthogonal keying for almost 18 dB of sign processing gain [29]. An RF switching matrix allows t multiplexing required for the input MSK waveforms and t the convolver outputs.

Using a convolver that is two data-bits long requires that entire two bits of time reversed reference code fill t convolver before it produces a useful output. Thus, the DP convolver can only produce an output every other data bit a therefore acts as a two-bit long binary orthogonal demod lator. To demodulate data at the full DPSK data rate, two 22 convolvers are used, with their references staggered by o data bit. When processing delayed multipath signals, since t codes are the same length as the convolver for data demodu tion, code alignment occurs when part of the reference co has past the convolver interaction region. Thus, a sm amount of code is not used and the convolution in this ca suffers an implementation loss called the filling-factor lo placing a limit on the duration of multipath delay that can effectively processed. This limitation does not artificia hinder the practical performance of the receiver since lar multipath spreads can be tolerated. The interference marg (in dB) obtained in the presence of centerband interference given by

$$[P_s/P_i]_{\max} = [T_sB_n]_{\mathrm{dB}} - \mathrm{SNR}_{\min} - L_s + [1 - T_d/T_s]_{\mathrm{dB}}$$

where P_s and P_i are the carrier signal power and t interference power, respectively, T_s is the symbol durati which is 11 μs for the DPSK demodulator, B_n is the no equivalent bandwidth of the spread-spectrum signal, and SNR is the minimum signal-to-noise ratio (in dB) for DP demodulation to produce a satisfactory bit error rate (e.g., dB SNR is approximately 10^{-3} bit error rate uncoded). L_s is t aggregate system implementation loss (typically 3 dB) due filtering which includes the affect of the convolver bandwi response. The expression ($1 - T_d/T_s$) is the filling factor l incurred by a long multipath delay. T_d is the delay from t path that was used to synchronize the codes (the fi detectable path) and T_s, as before, is the symbol duration one half the convolver length. The maximum filling loss tha path will incur (at the maximum processed multipath sprea is 2.5 dB, and more typical spreads will incur a fraction o dB. The actual SNR of each path must be computed determining the RAKE processing gain.

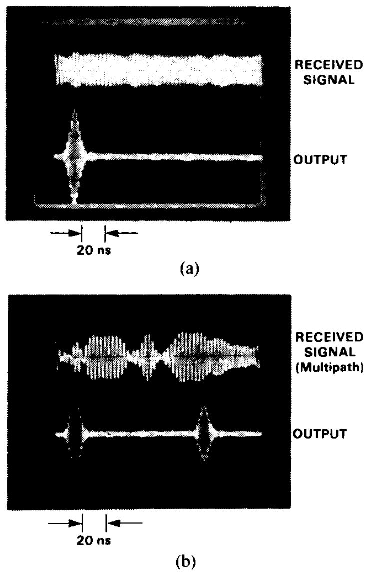


Fig. 5. (a) Convolver signal input (upper trace; only 200 ns of the 22 μs-long input is shown) without multipath and the consequent output (lower trace). (b) Convolver signal input (upper trace) with a single, strong multipath, and the consequent output (lower trace). The superposition of the second path on the original creates substantial AM which is linearly decomposed at the convolver output. Time scales are 20 ns/div.

For the 1.45 Mbit/s data rate, the convolvers are two data-bits long to allow for loss-free multipath processing when there is not as much processing gain available and consequently, the filling factor loss is zero.

Fig. 5(a) shows the constant-amplitude MSK IF inputs to the convolver and the resulting output. Fig. 5(b) shows the same MSK waveform, combined with a single multipath component, produced by delaying a fraction of the signal power by approximately 30 m of cable. The AM seen in the input waveform has clearly been resolved at the output.

Synchronization

The arrival time of a received packet is generally unknown to the matched filter receiver, although the first codes of an incoming packet are known. Since the reference is propagating, the preamble of the packet is recirculated to the convolver until a detection occurs, indicating a synchronized code match with the received waveform. Also, since the code propagates through the convolver, a reference that is twice as long as the convolver interaction region is used to obtain the full processing gain over all arrival times of the signal, and to achieve unambiguous detection timing. The synchronization process is discussed in great detail in [8], [30], and particularly [31]. Synchronization is simplified by using a preamble without data transitions, thus the detection process is performed on only the sum port of the convolver. The second convolver, required for DPSK, is used coincidently for synchronization with time-staggered codes to improve performance. The preamble codes are time reversed on 44-μs segments, and staggered by 22 μs. Thus, two full convolvers are used for matched-filter detection with the minor sacrifice of 22 μs of extra signal that must be transmitted. The synchronization process is essentially immediate. After detection, the codes are made the same length as the convolver and the receiver realigns its reference code generator to the received signal, assuming the code timing of the earliest detected output. The realignment occurs in microseconds and synchronization is accomplished. The detection process is repeated to verify the reception so as to reduce the likelihood of receiver blanking due to false alarms. The multipath processing window begins looking for delayed detections within a symbol starting from the first detected output.

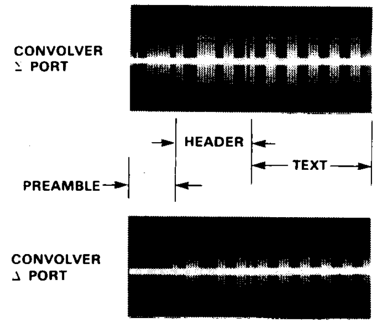


Fig. 6. Sum- and difference-port outputs from a DPSK convolver while receiving a packet. The preamble, which includes the synchronization outputs, occurs only in the sum port. The header and text appear in both ports depending on the value of the data. The text shown is at 90 kbits/s and it contains alternating sets of ones (difference-port output) and zeros (sum-port output).

A typical packet of convolver outputs (without multipath) is shown in Fig. 6. The preamble occurs only in the sum port (top oscilloscope trace) and the data-link header and text appear in both ports. The data, at the 90 kbit/s rate as specified in the header, comprises an alternating sequence of four zeros and four ones, in this example.

Digital Processing

1) Detection and RAKE Demodulation: During the preamble, which contains no data transitions, correlation peaks appear at the sum port of the convolver, and both the sum and the difference port will have equal power, uncorrelated noise. Linear envelope detection and a low-pass filter on the difference port thus provides a simple implementation of a constant false alarm rate (CFAR) threshold (Fig. 7). The excess sidelobes due to interpath interference, which is of interest at low SNR where the CFAR becomes critical, is balanced in each channel making the CFAR multipath resistant. The CFAR circuit drives the analog input of a multiplying D/A converter (MDAC) which generates the detection threshold. The digital value in the MDAC scales the detection threshold and is set by the microcomputer through the interface and control logic.

It has been observed that the envelope decorrelation due to multipath fading [5] occurs over a time scale substantially greater than 10 ms for ground vehicle speeds. Thus, it is possible to sample and store the multipath profile only once per packet for nominal length packets at 1.45 Mbits/s and 90 kbits/s. During the packet preamble the output of the CFAR detector is sampled and stored in shift registers whose clock timing defines the processing window [Fig. 8(a)]. The multipath profile is thus stored for the 90 kbit/s and the 1.45 Mbit/s data rates. The preamble always uses 90 kbit/s signaling in the long convolver, thus acting to sound out the channel for the high data rate with excess SNR and without the burden of intersymbol interference to disturb the profile.

The digital RAKE uses a counter running at 185 MHz to sample the full multipath resolution. The stored profile is recirculated each data bit in order to enable the RAKE counter to sample, while the running DPSK decision is applied to the count up/count down input. Shown in Fig. 8(b) are the RAKE circuit and digital waveforms for the data and the multipath. Only when the profile indicates the presence of a path (a logic one in the figure) is the DPSK input allowed to vote, thus

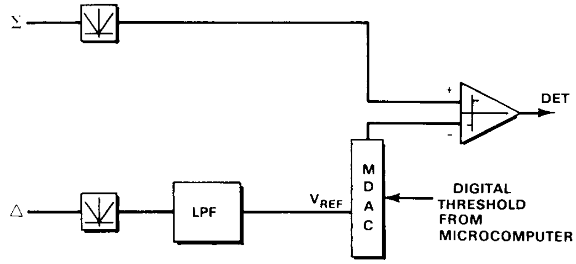


Fig. 7. Multipath-resistant CFAR detection. The DPSK convolver difference-port output is used as a noise reference.

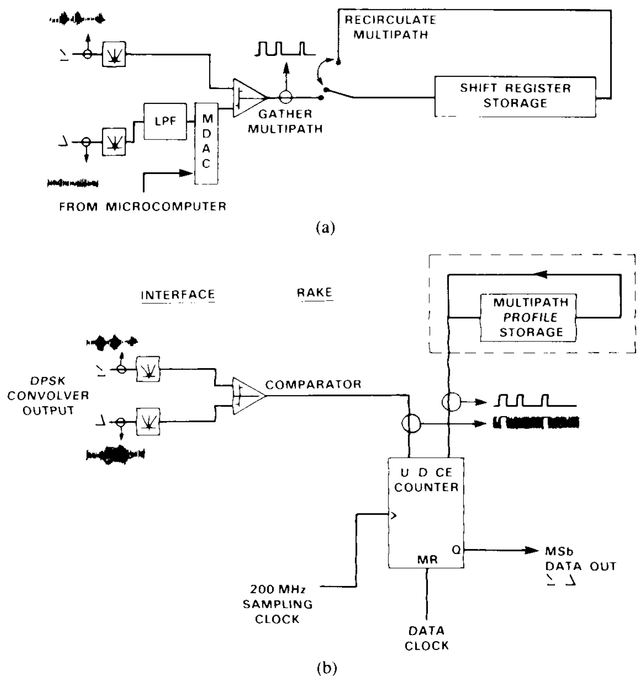


Fig. 8. RAKE demodulation. (a) Multipath-profile storage during the message preamble. (b) Demodulation using the stored profile as it recirculates.

eliminating the noise-only parts of the DPSK stream. The most significant bit of the count yields the results of the majority vote process providing the resulting data decision [8], [19]. This method of accumulating multipath is actually correlation against the multipath profile.

Fig. 9 shows oscilloscope traces of the fully digital RAKE working at 185 MHz with 10 dB SNR at the convolver output. The top trace is the stored multipath profile being recirculated. The second trace is the running DPSK decision provided by the sum/difference comparator. The next four traces are the least significant internal states of the RAKE counter with the least significant on the top. The single sample within the first multipath detection cases the counter to count down, then the wider, second detection causes the counter to count further down for four samples resulting in a strong data decision.

The calculated probability of error performance (P_e) of the RAKE circuit for different numbers (K) of equal energy multipaths is shown in Fig. 10. The horizontal axis is the ratio of total received energy in the data bit per path, to the noise power density (E_b/N_0). No fading statistics are included in the calculations; however, the gross effect of binary-digital combining as a function of signal strength can be see Increasing K from four equal paths to 16 equal paths, f example, increases the total signal energy available by 6 d while the curve improves by only 3–4 dB. Most of t implementation loss is due to the detection process used for t multipath channel sounding. For example, while 10 dB of E N_0 may result in a typical P_e of 10^{-5} for demodulation, t detection part of the RAKE can only obtain a probability detection (P_d) of 20 percent for a probability of false ala (P_{fa}) of 10^{-4} [cf. 32, p. 300]. For a Gaussian channel, a sing false detection in the multipath window of several hundr samples results in a substantial increase in P_e for the data b Two curves are plotted for the $K = 1$case. These indicate t effect of detection operating point on the demodulati characteristics. These curves saturate in performance becau of the P_{fa}. At large E_b/N_0, the chance of an error due to a fal detection of a path places a lower bound on the probability error. It is only necessary to push this bound below the syste operating requirements based on coding or other constrain Although for a $P_{fa} = 10^{-3}$, the lower bound is higher than f the curve with $P_{fa} = 10^{-5}$, the P_e for 10^{-3} is better at the lo

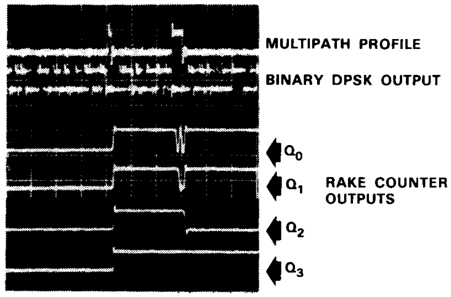


Fig. 9. Scope traces of the operation of the fully digital RAKE circuits clocked at 185 MHz. The top trace is the recirculated multipath profile. The second trace is the DPSK binary decision. Notice the steadiness of the samples that occur under the multipath which indicates the presence of significant signal energy. The next four traces are the least significant bits of the RAKE counter. All the counts are in the same direction (down) indicating strong SNR on the active paths.

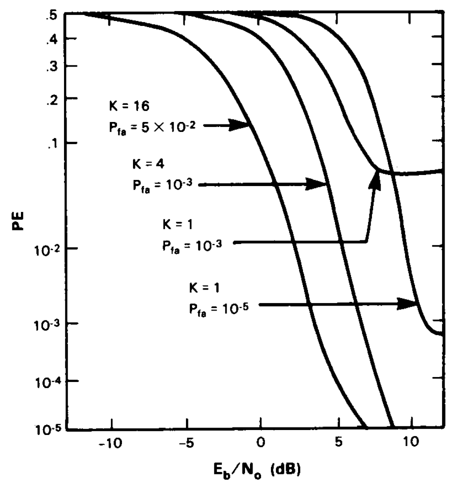


Fig. 10. Calculations of the RAKE performance. K is the number of equal energy paths. The horizontal axis is the ratio of signal energy per path to the noise power density. The vertical axis is the probability of bit error.

E_b/N_0 points where the error correction unit is usable, thus it is a preferable operating point.

In a diffuse channel, false alarms have less impact than for a single path and the lower bound occurs at very low P_e. The curves plotted for $k = 4$ and $k = 16$ illustrate this. These two curves have been calculated using the P_{fa} that provides the best performance. It is apparent that the P_{fa} for best performance must be selected according to the multipath channel characteristics. The degree of diffuseness in the channel changes on a slow enough time scale so that the network level microcomputer can adjust the digital threshold in the CFAR circuit to set the required P_{fa} as a function of the number of detected paths. The channel measurements taken by the modem, and those shared with neighboring radios provide sufficient information for network-level software to determine the proper threshold setting.

The $k = 1$, $P_{fa} = 10^{-5}$ curve indicates an implementation loss of 4 dB compared to ideal PSK at $P_e = 10^{-3}$ (2.5 dB loss compared to DPSK). Recognizing the adaptability of the RAKE technique, this loss should be contrasted with the typical 20–30 dB of loss that results from narrow-band communications in multipath. Much of the RAKE loss is recovered in diffuse channels such as the $K = 16$ *case*. Although analog or multibit diversity combining would perform closer to ideal than the binary-quantized RAKE [5], [33], the high bandwidth used here makes those techniques prohibitive.

An improvement of the imbalance between the detection and demodulation processes in the digital RAKE processor can be achieved by using a higher processing gain for the detection of the multipath profile. In the modem, the multipath profile is actually obtained by the logical AND (incoherent binary combining) of detection profiles of two consecutive data bits resulting in approximately a 2 dB improvement in detectability. This technique could be extended for further improvement by combining over more data bits at the expense of a long preamble to initialize the RAKE profile.

For RAKE processing in the 90 kbit/s mode, a 5.5 μs input time window, or a quarter bit in output time, is used. The 1.4 Mbit/s mode processing window is the entire bit length minus 40 ns to read out the data. Although the typical number of resolved paths has been measured to be on the order of 10, the wider processing window is necessary to handle the time span of the spread [11]. If too many paths occur such that the processing gain of the high data rate cannot suppress the interpath interference, the 90 kbit/s data rate is used even though the SNR could support the 1.4 Mbit/s rate.

2) Correlation: The operation of the binary integrator is shown in Fig. 11. The multipath processing window of the convolver is of high bandwidth and short duration, lending itself to low bandwidth, long duration postprocessing. The sample and binary-quantized output is stored in parallel shift registers at high speed during the active output window and is read out at a fraction of the speed into an accumulating memory between windows [8], [19]. We show one of the two binary integrator channels which comprise a fast in/slow out (FISO) storage and an accumulating memory. The accumulating memory is a bank of shift registers that recirculate through an arithmetic logic unit. An exclusive OR function is used to remove data transitions and for chopper stabilization of the integrator.

The binary quantization simplifies the integrator circuitry. The FISO storage registers are four TTL chips fed by a few ECL chips. The accumulating memory uses about 12 TTL chips. In total, the two channels of binary integration including clocking circuits occupy approximately 15 square inches and most of that is reused for the other modes of the radio. As a more compact alternative, a 5 μm NMOS binary integrator chip was made with the DARPA MOSIS [27] silicon foundry.

A variety of options are available with the binary integration as determined by the microcomputer and received-packet header. Coherent integration, noncoherent integration, and double-threshold detection are three techniques described in this paper.

For the coherent integration (Fig. 12), the RF waveform from the convolver is heterodyned with in-phase and quadrature carriers to obtain the bipolar baseband signals. These are then compared to zero and integrated separately in the two channels of the binary integrator. The results are squared and summed, and then this magnitude-squared value is compared to a threshold for detection. The detections are used for preamble detection of a scheduled reception, and are stored and updated as multipath for demodulation. Data may be demodulated using this coherent integration by performing DPSK between each integrated data bit. In this case, all the matched filter outputs integrated into a bit have no phase transitions, but an adjacent bit may have a 180° inversion on the carrier phase on all convolver outputs. The signs of the data-bit accumulations are compared on a sample-bin-by-sample-bin basis. RAKE demodulation is performed using the detection profile obtained from the sum-of-squares process. For these lower data rates, the multipath must be updated each data bit since the longest data bit could be over 20 ms (44 bits/s).

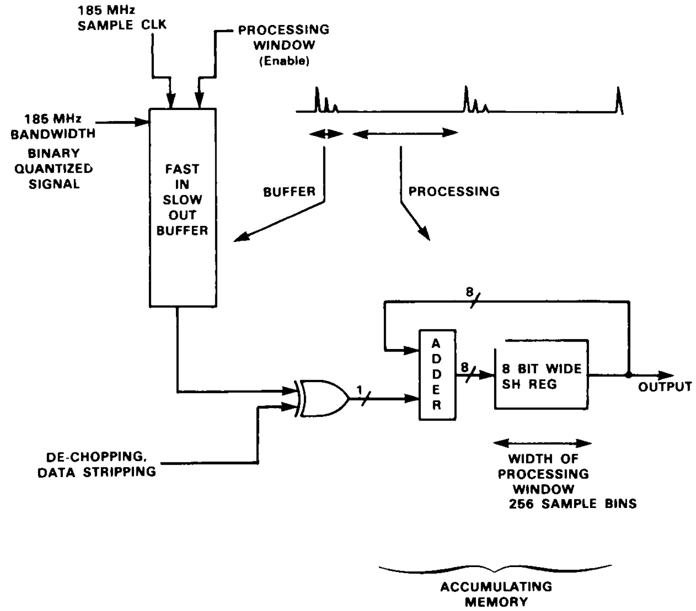


Fig. 11. The binary integration technique for SAW-convolver outputs. The short-duration outputs are stored in the FISO buffer and then processed in the accumulating memory.

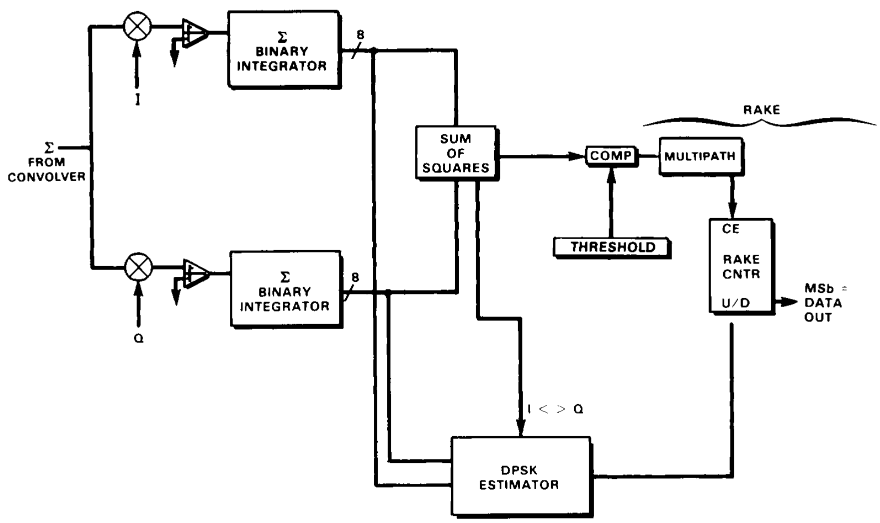


Fig. 12. Coherent correlation for DPSK data demodulation.

If there is excessive Doppler or clock offset, coherent integration cannot be used and less efficient noncoherent integration is employed as in Fig. 13. Noncoherent integration uses the envelope-detected sum and difference port of the convolver outputs compared to each other to create a binary DPSK decision in each sample bin of the processing window. The DPSK output is fed to one channel of the binary integrator which accumulates the results to form a bipolar data decision. The resulting outputs of the integrator are accumulated using RAKE. The bipolar output of the integrator must be magnitude-detected to determine the multipath profile and the sign bit provides the bipolar decision for each active path.

The binary integration results in a binomial distribution, which for a large number of samples approximates a conti ous Gaussian distribution. If the number of matched fil outputs per data bit is small, for example, 16 or 32 instead 1000, it becomes impossible to set a meaningful detecti threshold for multipath profiling or for initial detection. T threshold has very few values to take on, all of which ha poor false alarm versus detection probability characteristi By applying an analog threshold to the envelope-detec signals, instead of comparing sum port to difference port, probability of occurrence entering the binary integrator any sample in the binomial distribution is weighted in analog fashion, thus allowing meaningful digital thresh settings at the integrator output. Some number M, out of

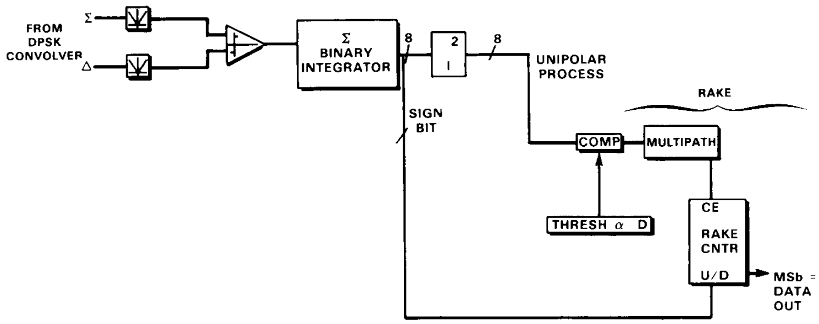


Fig. 13. Incoherent correlation for BOK data demodulation.

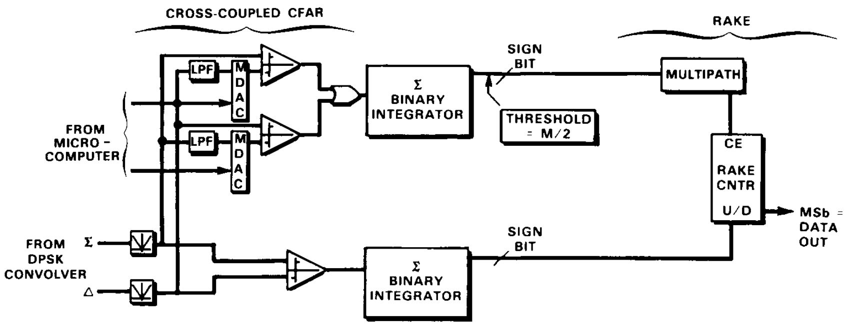


Fig. 14. Incoherent correlation with double-threshold detection for BOK data demodulation. The CFAR detection is cross coupled between the two output ports.

accumulated analog detections, are chosen as a threshold. For $N > 8$, it is best to let $M = 1/2\ N$. This M of N detection method has been used for some time in radar [34]. The analog threshold is applied by cross-coupled CFAR circuits as in Fig. 14. The output from the sum port uses the CFAR threshold from the difference port, and the output from the difference port, which only occurs when there is noise in the sum port, uses the sum port CFAR threshold. The data decisions at the integrator output that feed the RAKE counter are still created by integrating the sum–difference DPSK comparison in the other binary integrator channel.

The implementation loss for RAKE demodulation with M of N detection is illustrated in the calculated curves of Fig. 15. As in Fig. 10, the horizontal axis is the E_b/N_0 per equal-energy multipath and no fading statistics are included. Shown are a pair of curves for M of N = 8 of 16, and a pair for M of N = 16 of 32. Each pair compares the cases of $K = 4$ and $K = 16$ multipaths. As expected, increasing the number of multipaths shifts the curves to the left, indicating an improvement, since there is more total energy in the data bit. However, as illustrated by the 8 of 16 case, a crossover can occur. This is due to each curve having a different P_{fa} which is chosen for the best performance. Some shift in P_{fa} is required as a function of the values of M and N; although, this dependency is not as great as the dependency on K. A thorough discussion of the dependency of detection operating point on M and N is given in [34]. The 16 of 32 curves have a higher implementation loss because the input SNR is scaled down accordingly for the longer data bits to keep the E_b constant. The binary quantization and the incoherent combining at low SNR accounts for this loss.

These losses are small compared to the increase in processing gain. Combining only 32 samples coherently and with analog values would provide 15 dB of additional processing

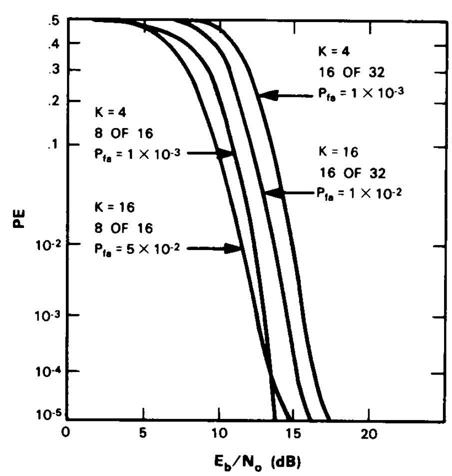


Fig. 15. Calculated performance of incoherent correlation with double-threshold detection using RAKE processing. The horizontal axis is the ratio of signal energy per path to the noise power density. The vertical axis is the probability of bit error.

gain over the 33 dB of the convolver. At an E_b/N_0 of 10 dB, this corresponds to an SNR of -38 dB at the convolver input. The SNR at the convolver output, prior to the incoherent combining would be -5 dB, resulting in approximately a 3 dB combining loss.

For each application of the hybrid correlator for demodulation, the RAKE processing window at the output of the binary integrator is 2.76 μs of convolver input time representing 256

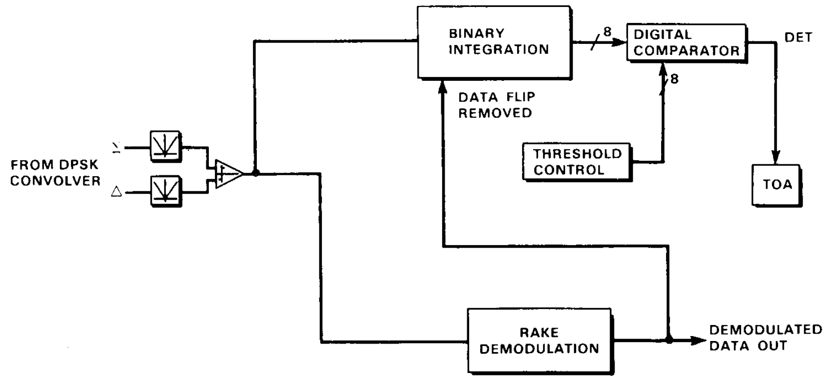


Fig. 16. Incoherent correlation in the presence of data to extract the TOA precursor.

parallel correlations. The binary-integrator RAKE runs at less than 25 MHz due to the FISO buffering, although it is otherwise like the higher rate RAKE circuits. Because initial detection of a packet with the binary integrator is a correlation process, a prior estimate must be made of where to place the processing window; however, the correlation search time that is normally encountered is reduced by the number of resolution elements in the window (256).

3) Time of Arrival Measurements: At the 90 kbit/s rate, the TOA precursor search is performed noncoherently as a nonintrusive background process (Fig. 16) [35], [36]. The precursor processing time window just precedes the RAKE processing window. The integration is done after the bit demodulation so the data transitions may be removed using the exclusive OR function [19], [37]. The data value that is imposed on the matched filter output frame must be removed so the integration occurs on the energy of the precursor. The binary integrator stores the sampled matched filter output frame while the data bit is being demodulated. The data value is then available when the stored samples are accumulated. The precursor search has 3-m resolution due to the 100 MHz convolver bandwidth. For a 1000 bit data packet, the processing gain is 15–30 dB over the original 30 dB of the matched filter. The result is that a window can be searched that represents a half mile in propagation and therefore potential improvement in registering the time of arrival. (Earlier half-mile segments can also be searched by moving the multipath window under network-level control.) The 15–30 dB range of processing gain results from the noncoherent accumulation in the integrator. As seen in Fig. 17, at low SNR, the noncoherent processing gain is a strong function of the input SNR. Coherent integration may instead be selected; however, to avoid doubling the binary integrator hardware, no data may be transmitted. Thus, a specialized packet type is used.

The 90 kbit/s data with the noncoherent integration for precursor detection is illustrated in Fig. 18. The figure does not show the limits in performance but rather illustrates the operation. The top photograph shows the time-domain waveform of a received MSK signal contaminated with laboratory generated noise with a small multipath precursor. The large signal is of the order of -10 dB SNR and the small precursor is of the order of -30 dB SNR at the convolver input. The second photograph shows the detectable main lobe which is used for demodulation and the initial estimate of the time of arrival of the signal. The precursor is barely visible and is indicated by the arrow. The bottom trace is the binary-quantized running data decision which has only noise when not located under a multipath peak. The next figure is a consecutive frame at the output of the matched filter. Where there is no multipath present, the DPSK decision is seen to change randomly. Under the large mainlobe, the data are clearly

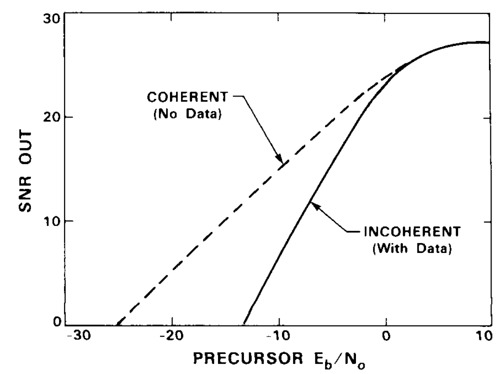


Fig. 17. Detectability of the multipath precursor for TOA as a function input SNR for coherent and incoherent processing. Coherent processi performs better, but would require a duplication of both binary integrat channels in order to simultaneously process data.

stable as the signal dominates the noise. Under the precurso the output is only somewhat stable since it is substantial influenced by the noise. In the fourth photograph, the top tra is the readout clock and the bottom trace is the detected outp from the binary integrator with a compressed time scale fro the 185 MHz bandwidth matched-filter outputs. The detecti to the right is that of the large mainlobe and to the left is t precursor. Each clock cycle represents 3 m in range. T distance between the large signal detection and the precurs detection is the corrected time-of-arrival estimate that available after the data packet is demodulated.

IV. Summary

This paper has described the application of a hybrid analo digital signal processor to realize a spread-spectrum rad uniquely suited for mobile packet radio networks in a varie of multipath environments. The signal processing capabiliti described are made possible through the combination analog SAW technology and binary–digital processing. Wav forms of almost 100 MHz bandwidth with continuous changing spreading codes are matched filtered with over 30 d of processing gain and further correlated with a search windo of 2.7 μs to provide greater than 60 dB of processing gain.

The modem uses the hybrid signal processor (Fig. 2) in multitude of configurations which are application depende and determined by the control logic interpreting the netwo commands. Initial detection of a received signal may accomplished with either the matched filter or the hybr

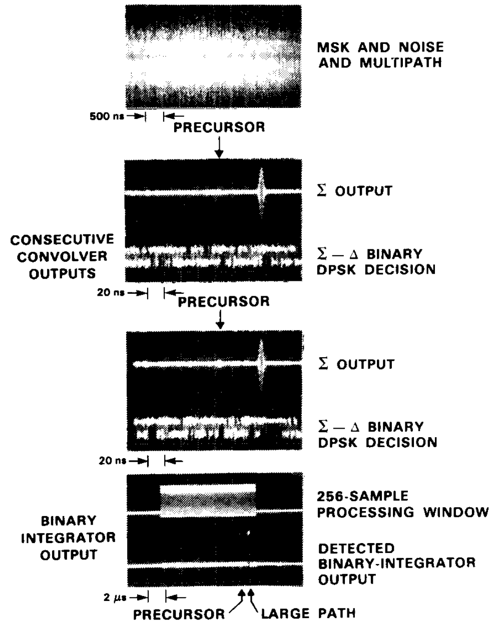


Fig. 18. Incoherent binary integration for finding a precursor. The top photo is the input to the matched filter (time scale = 500 ns/div). The two middle photos are consecutive output frames from the matched filter (time scale = 20 ns/div). The bottom photo shows the result out of the binary integrator after detection (time scale = 2 μs/div).

correlator. The matched filter coherently demodulates at either 1.4 Mbits/s or 90 kbits/s depending on the processing gain required. If additional processing gain is needed the data rate is reduced and the binary integrator is reconfigured into either coherent or noncoherent operation, depending on the application. The multipath is noncoherently accumulated for demodulation at all data rates. The high processing gain is also used for time-of-arrival processing. The performance of a system incorporating this technology is very powerful, yet requires relatively modest size, power, and cost. The modem unit consumes approximately 100 W occupies a fraction of a cubic foot, and excluding the convolvers, is made with "off-the shelf" parts. The major functions were field tested at various stages of development and agreement with the designed performance was generally good. The final radio was not field tested, however, all of the functions were demonstrated in the lab between two independently running radios at short range and proved to be satisfactory.

The combining of adaptive anti-jam and data-rate capabilities, pseudonoise bandwidth spreading with continuously changing codes, and anti-multipath processing for the ground-communication environment achieves an important goal for network communication.

Acknowledgment

The authors gratefully acknowledge the creative technical support of M. Seaver, C. Koulman, K. Bennett, D. Prentiss, and J. Holtham. Their diligence over several years allowed us to bring the ideas put forth here to fruition as a working piece of hardware. The NMOS binary integrator chip and code generator chip described were designed by I. Yao. We also thank P. Grant for his technical expertise in editing the manuscript.

References

[1] R. E. Kahn, S. A. Gronemeyer, J. Burchfiel, and R. C. Kunzelman, "Advances in packet radio technology," *Proc. IEEE,* vol. 66, pp. 1468–1496, Nov. 1978.

[2] V. G. Cerf, "Packet communication technology," in *Protocols & Techniques for Data Communication Networks,* F. F. Kuo, Ed. Englewood Cliffs, NJ: Prentice-Hall, 1981.

[3] D. Huynh and F. F. Kuo, "Mixed-media packet networks," in *Protocols & Techniques for Data Communication Networks,* F. F. Kuo, Ed. Englewood Cliffs, NJ: Prentice-Hall, 1981.

[4] G. Lauer, J. Westcott, J. Jubin, and J. Tornow, "Survivable protocols for large scale packet radio networks," presented at IEEE GLOBECOM '84 Conf. Proc., New York, 1984.

[5] G. L. Turin, "Introduction to spread-spectrum antimultipath techniques and their application to urban digital radio," *Proc. IEEE,* vol. 68, pp. 328–353, Mar. 1980.

[6] J. H. Fischer, J. H. Cafarella, D. R. Arsenault, G. T. Flynn, and C. A. Bouman, "Wideband packet radio technology," *Proc. IEEE,* vol. 75, pp. 100–115, Jan. 1987.

[7] M. K. Simon, J. K. Omura, R. A. Scholtz, and B. K. Levitt, *Spread Spectrum Communications,* Vol. 1-3. Rockville, MD: Computer Science, 1985.

[8] I. Yao and J. H. Cafarella, "Applications of SAW convolvers to spread-spectrum communication and wideband radar," *IEEE Trans. Sonics Ultranson.,* Special Issue on SAW Convolvers and Correlators, vol. SU-32, pp. 760, Sept. 1985.

[9] J. H. Cafarella, "Surface-acoustic-wave devices for spread-spectrum communications," in *Proc. of the 11th Conf. (1979 International) on Solid State Devices,* Tokyo, Japan, 1979; *Jpn. J. Appl. Phys.,* vol. 19, Supplement 19-1, pp. 667–674, 1980.

[10] R. Price and P. E. Green, Jr., "A communication technique for multipath channels," *Proc. IRE,* vol. 46, pp. 555–570, Mar. 1958.

[11] D. L. Nielson, "Microwave propagation and noise measurements for mobile digital radio application," Packet Radio Note 4, Stanford Res. Inst., Menlo Park, CA, Advanced Res. Proj. Agency, contract DAHC15-73-C-0187, Jan. 1975.

[12] G. L. Turin, "Antimultipath techniques for packet radio systems," Packet Radio Temporary Note 262, Telecommun. Sci. Cen., Stanford Res. Inst. Int., Menlo Park, CA, Advanced Res. Proj. Agency Order 2302-18, contract MDA 903-78-C-0126 Nov. 22, 1978.

[13] These functions are supported by the LS56 LSI circuit provided by LINKABIT Corp., San Diego, CA.

[14] J. H. Fischer, J. H. Cafarella, G. T. Flynn, C. A. Bouman, D. R. Arsenault, J. D. Kurtze, and R. R. Boisvert, "A wideband packet radio based on hybrid analog/digital signal processing and layered architecture," presented at IEEE MILCOM '85 Conf. Rec., New York, Oct. 1985.

[15] J. J. Spilker, Jr., *Digital Communications by Satellite.* Englewood Cliffs, NJ: Prentice-Hall, 1977.

[16] S. A. Reible, "Acoustoelectric convolver technology for spread-spectrum communications," *IEEE Trans. Microwave Theory Tech.,* vol. MTT-29, pp. 463–473, May 1981.

[17] I. Yao, "High performance elastic convolver with parabolic horns," in *Proc. IEEE Ultranson. Symp.,* New York, 1980, pp. 37–42.

[18] R. W. Ralston, D. H. Hurlburt, F. J. Leonberger, J. H. Cafarella, and E. Stern, "A new signal-processing device, the integrating correlator," in *Proc. IEEE Ultrason. Symp.,* New York, 1977, pp. 623–628.

[19] J. H. Cafarella, "Advanced SAW-based signal processing for packet communications," presented at IEEE MILCOM '82 Conf. Rec., New York, 82CH1734-3, Oct. 1982.

[20] P. M. Grant and R. S. Withers, "Recent advances in analog signal processing," submitted to *Trans. Aerosp. Electron. Syst.*

[21] J. H. Cafarella, "Wideband signal processing for communication and radar," presented at IEEE NTC'83 Nat. Telesyst. Conf. Proc., New York, Nov. 1983.

[22] E. E. Swartzlander, Jr., and G. Hallnor, "Frequency-domain digital filtering with VLSI," in *VLSI and Modern Signal Processing,* S. Y. Kung, H. J. Whitehouse, and T. Kailath, Eds. Englewood Cliffs, NJ: Prentice-Hall, 1985.

[23] TRW Semiconductors TMC 2220.

[24] J. V. Harrington, "An analysis of the detection of repeated signals in noise by binary integration," *IRE Trans. Inform. Theory,* vol. IT-1, Mar. 1955.

[25] F. Amoroso and J. A. Kivett, "Simplified MSK signaling technique," *IEEE Trans. Commun.,* vol. COM-25, pp. 433–441, Apr. 1977.

[26] S. A. Reible, J. H. Cafarella, R. W. Ralston, and E. Stern, "Convolvers for DPSK demodulation of spread-spectrum signals," in *Proc. IEEE Ultrason. Symp.,* New York, 1976, pp. 451–455.

[27] F. Guterl, "In pursuit of the one-month chip," *IEEE Spectrum,* vol. 21 p. 28, Sept. 1984.

[28] S. Pasupathy, "Minimum shift keying: A spectrally efficient modulation," *IEEE Commun. Mag.,* pp. 14–22, July 1979.

[29] V. S. Dolat and G. T. Flynn, "Integration of multiple elastic

convolvers into a communication signal processor," presented at 1984 IEEE Ultranson. Symp. Proc., New York, 1984.
[30] D. P. Morgan, J. H. Collins, and J. G. Sutherland, "Asynchronous operation of an analog convolver," *Proc. IEEE,* pp. 1556–1557, Dec. 1972.
[31] J. H. Fischer, "Autocalibrating circuitry for processing SAW convolver outputs," presented at 1985 Ultrason. Symp. Proc., New York, Oct. 1985.
[32] J. V. DiFranco and W. L. Rubin, *Radar Detection.* Dedham, MA: Artech House, 1980.
[33] J. M. Wozencraft and I. M. Jacobs, *Principles of Communication Engineering.* New York: Wiley, 1965.
[34] P. Swerling, "The "double threshold" method of detection," Rand Corp., Memo RM-1008, Dec. 1952.
[35] J. H. Fischer, J. Cafarella, and G. T. Flynn, "SAW convolvers and signal processing in a packet radio," *Conf. Rec. IEEE MTT-S 1986,* New York, June 1986.
[36] J. H. Fischer and J. H. Cafarella, "Hybrid analog/digital signal processing for data communications in multipath," presented at the Meet. Union Radio Scientists, Vancouver, B.C., Canada, June 17–23, 1985 (unpublished).
[37] This architecture is an outgrowth of discussions with G. L. Turin.

★

Jeffrey H. Fischer (M'86) was born in Brooklyn, NY, on February 15, 1958. He received the B.S.E.E. degree in 1979 and the M.E.E.E. degree in 1980, both from Cornell University, Ithaca, NY.

From 1980 to 1986 he was a member of the technical staff of the Analog Device Technology Group at the Massachusetts Institute of Technology, Lincoln Laboratory, Lexington, MA. His work involved the development of signal processing algorithms, architectures, and circuits for the application of advanced analog signal-processing devices. He has worked in analog, digital, and RF circuit and subsystem design for spread-spectrum communications, focusing on the development of the spread-spectrum radio described in this paper. He has authored a number of papers and meeting presentations on various aspects of this radio. In October 1986 he joined MICRILOR, Inc., Wakefield, MA, to work on advanced signal-processing technology for applications in communications, radar, and instrumentation. His interests include circuit synthesis, classical control theory, and communication system design.

★

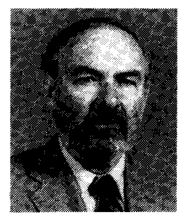
John H. Cafarella (S'70–M'84) received the Sc.D. degree from the Massachusetts Institute of Technology, Cambridge, in 1975. His graduate studies concentrated in electromagnetic and acoustic fields solid-state physics, and microwave circuits. His thesis research was in surface-acoustic-wave signal-processing devices, particularly convolvers and memory correlators.

While attending the M.I.T. Graduate School, he was Research Assistant at Lincoln Laboratory, Lexington, MA, and he subsequently joined the Laboratory as Staff Member in 1974. He demonstrated the first engineered acoustoelectric convolver in 1975 and began to pursue the application of this device to spread-spectrum communication. While continuing work on various SAW devices, in subsequent years he began to work actively with systems groups to explore the radar and communications applications of these devices. He established an activity aimed at rapidly connecting emerging components to systems. This has resulted in the development of a complete spread-spectrum radio suited to the needs of tactical communication and the development of a hybrid radar signal processor which offers a solution to radar problems of both tactical and strategic importance. He was the Leader of the Analog Device Technology Group when he left Lincoln Laboratory in 1984 to cofound MICRILOR, Inc., located at Wakefield, MA, which applies advanced signal-processing technology to communications and radar subsystems.

Charles A. Bouman was born in Philadelphia, P in 1958. He received the B.S.E.E. degree from t University of Pennsylvania, Philadelphia, in 19ŧ and the M.S. degree from the University of Calif nia at Berkeley, in 1982.

From 1982 to 1985, he was a staff member in t Analog Device Technology Group at the Massact setts Institute of Technology, Lincoln Laborato Lexington, MA. There his work involved t development of algorithms, architectures, and c cuits for the application of advanced analog sig processing devices. This work included design and analysis for the spre spectrum radio described in this paper and the development of adapt clutter-suppression techniques using nonrepeating pseudonoise radar wa forms. He is currently a graduate student at Princeton University, Princet NJ, where his interests are in the areas of digital signal processing a statistical image modeling.

★



Gerard T. Flynn (S'58–M'65) received the B degree in physics electronics from LaSalle Colle Philadelphia, PA, in 1963.

He is currently a staff member at Massachus Institute of Technology, Lincoln Laboratory, L ington, MA, engaged in the design of airborne ra systems. From 1980 to 1986 he worked in Analog Device Technology Group at Lincoln La ratory where he was responsible for the design the RF and IF portions of the spread-spectrum ra described in this paper. Prior to his work on radio he had been involved in the development of detection systems for de space optical surviellance, ECM for strategic missile systems, and bandwi compression for television. He has authored and coauthored a numbe papers in these areas. His interests are in microwave circuit design and sig processing.

★

Victor S. Dolat received the Ph.D. degree physics from Purdue University, West Lafaye IN, in 1971.

Since April 1971, he has been a staff membe Massachusetts Institute of Technology, Linc Laboratory, Lexington, MA. He joined the Ana Device Technology Group in 1973 where he l been involved in the design and development various surface acoustic wave devices. These clude the reflective array compressor, monolit convolver, and SAW/FET programmable transv sal filter. He was involved in the design of the SAW convolvers used in radio described in this paper. His current work is focused on advanced la trimming techniques of analog signal processing devices.

★

Rene Boisvert (S'80–M'80) was born in Fitchbu MA, in 1942. He graduated from technical sch and class A and class C electronic school in the U Navy.

He was an electronic fire control technician in Navy from 1962 to 1966 aboard the USS Cambar He joined the Massachusetts Institute of Techn ogy, Lincoln Laboratory, Lexington, MA, in 19 In 1977 he joined the Analog Device Technolc Group at the laboratory, where his work invol the development of architectures and circuits for demonstration and application of advanced analog signal-processing devic He has worked in analog, digital, and RF circuit design and instrumentati for spread-spectrum communications, focusing on the development of radio described in this paper.