KLI-5001G

5000 Element Linear CCD Image Sensor

Performance Specification

Eastman Kodak Company

Image Sensor Solutions

Rochester, New York 14650-2010

Revision 8

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Eastman Kodak Company - Image Sensor Solutions
For the most current information regarding this product:
Phone: (585) 722-4385 Fax: (585) 477-4947 Web: www.kodak.com/go/imagers E-mail: imagers@kodak.com

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Features

- High resolution: 5000 pixels
- On-chip Sample/Hold
- Wide Dynamic Range
- No Image Lag
- High Charge Transfer Efficiency
- Up to 2V peak-peak Output
- Two-Phase Register Clocking
- On-chip Dark Reference

Description

The KLI-5001G is a high resolution, linear array designed for scanned imaging applications. This device contains a row of 5000 active photoelements, consisting of high performance 'pinned diodes' for improved sensitivity, lower noise and elimination of lag. Readout of the pixel data is accomplished through the use of dual CCD shift registers, positioned on either side of the detector array. The sensors are positioned on 7µm centers with an associated 7µm aperture spanning the length of the array.

The device architecture has on-chip correlated, double-sampling circuitry. The device is manufactured using NMOS, buried channel processing and utilize dual layer polysilicon and dual layer metal technologies. The die size is 36.00mm X 1.12mm and the chip is housed in a 24-pin, 0.600" wide, dual in-line package. Cover glass options include standard clear, or multi-layer anti-reflection coated (MAR).

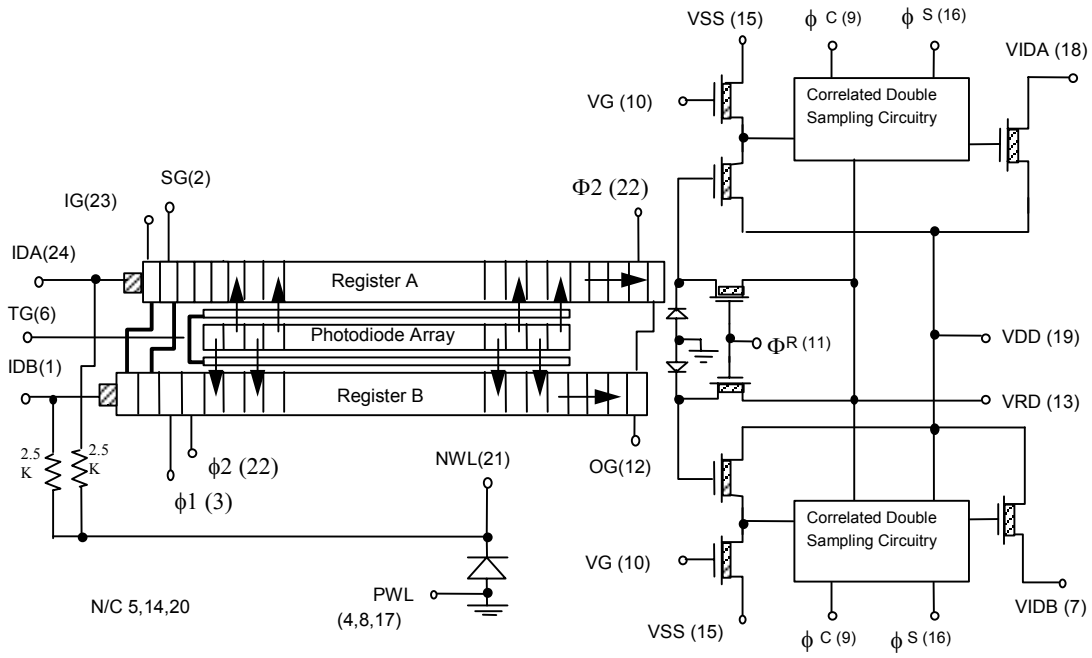


Figure 1 - Imager Schematic

Imaging

During the integration period, an image is obtained by collecting electrons generated by incident photons. The charge stored in the photodiode array is a linear function of the local exposure. The charge is isolated from the CCD shift registers during this period by the transfer gate TG, which is held at a barrier potential. At the end of the integration period, the CCD register clocking is stopped and the clock phase adjacent to the photodiode, $\phi 1$, and the TG gate, are turned 'on'. The charge is drained from the photosites through the transfer gate and into the $\phi 1$ region. The odd photodiodes are drained to the 'A' register while the even photodiodes are drained to the 'B' register. After this transfer is complete, TG is turned 'off' once again, isolating the two regions, while the current line is read out and the next line is integrated.

Charge Transport and Sensing

The readout of the signal charge is accomplished by two-phase, complementary clocking of the $\phi 1$ and $\phi 2$ gates. The data in both registers is clocked simultaneously toward the output structures. The data is transferred to the two output structures in parallel format at the falling edge of the $\phi 2$ clock. Resettable floating diffusions are used for the charge-to-voltage conversion while source followers provide buffering to external connections. The potential change on the floating diffusion is dependent on the amount of signal charge and is given by $\Delta V_{FD} = \Delta Q/C_{FD}$. Prior to each pixel output, the floating diffusion is returned to the RD level by the reset clock, ϕR. The device incorporates circuitry to implement correlated double-sampling (CDS) of the output. This effectively removes kTC noise and reduces in 1/*f* noise, as well as providing a sampled and held output.

Package Configuration

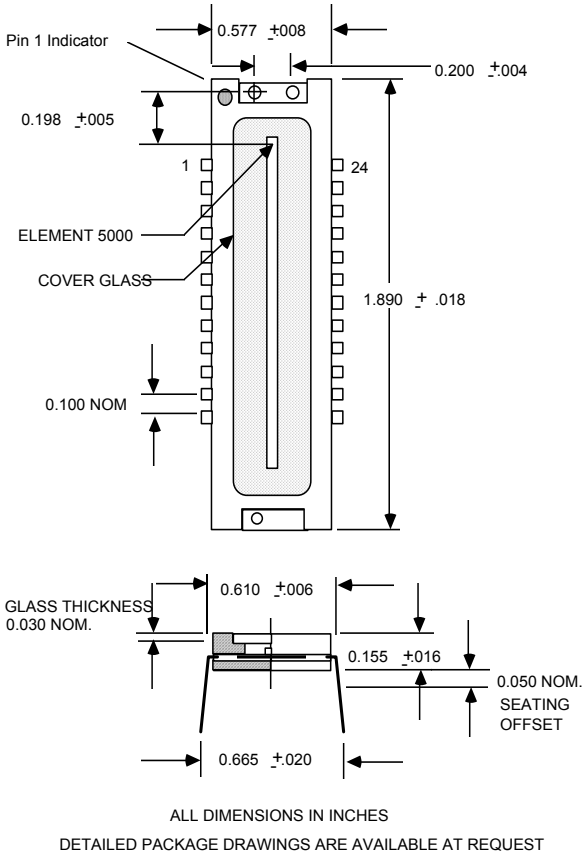


Figure 2 - Packaging Diagram

Pin Description

Pin Number	Symbol	Description
1	IDB	B Channel Input Diode (Test Pin)
2	SG	Signal Gate (Test Pin)
3	ϕ1	Phase 1 Register Clock
4	PWL	Substrate
6	TG	PD-CCD Transfer Gate
7	VID_B	B Channel Output
8	PWL	Substrate
9	ϕC	Clamp Clock for CDS
10	VG	Load Gate Bias
11	ϕR	Reset Clock
12	OG	Output Gate Bias
13	RD	Reset Drain Reference
15	VSS	Output Buffer Return
16	ϕS	Sample Clock for CDS
17	PWL	Substrate
18	VID_A	A Channel Output
19	VDD	Output Buffer Supply
21	NWL	Scavenger/Light Shield Bias
22	ϕ2	Phase 2 Register Clock
23	IG	Input Gate (Test Pin)
24	IDA	A Channel Input Diode (Test Pin)
5, 14, 20		No Connection

Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Remarks
Gate Pin Voltages	V_{GATE}	-16	+16	V	Notes 1,2
Pin to Pin Voltage	$V_{PIN-PIN}$		20	V	Note 3
Diode Pin Voltages	V_{DIODE}	-0.5	+16	V	Notes 1,4
Output Bias Current	I_{DD}		-10	mA	Note 5
Output Load Capacitance	$C_{VID, LOAD}$		15	pF	
CCD Clocking Frequency	f_C		15	MHz	Note 6
Operating Temperature	T_{OP}	0	70	^oC	Note 7
Storage Temperature	T_{ST}	-25	+80	^oC	

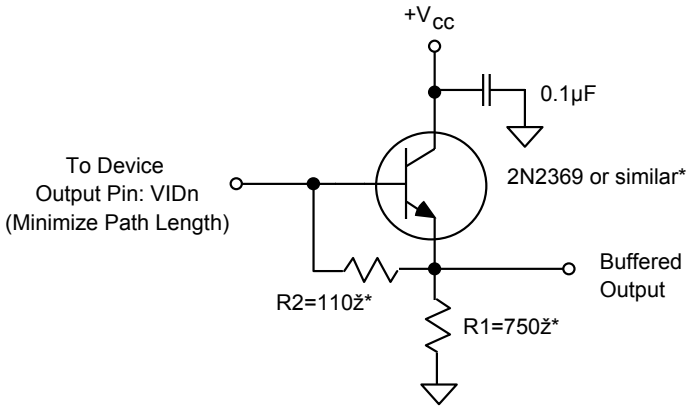
Notes:
1. Referenced to substrate voltage.
2. Includes pins: ϕ1, ϕ2, IG, SG, TG, ϕR
3. Voltage difference (either polarity) between any two pins.
4. Includes pins: VRD, VDD, IDA, IDB, VIDA, VIDB, VSS, NWL, OG, VG, ϕC, ϕS
5. Care must be taken not to short output pins to ground during operation as this may cause serious damage to the output structures.
6. Charge transfer efficiency will degrade at frequencies higher than the nominal (12.5 MHz) clocking frequency.
7. Noise performance will degrade with increasing temperatures.

CAUTION:
To allow for maximum performance, this device contains limited I/O protection and is sensitive to electrostatic discharge damage. ISS image sensors are rated as Class 0 (<250V per JESD22 Human Body Model test), or Class A (<200V JESD22 Machine Model test.)
Devices should be handled in accordance with strict ESD handling procedures!

DC Conditions

Symbol	Parameter	Min.	Nom.	Max.	Units	Remarks
V_{PWL}	Substrate	-0.5	GND	+0.5	V	
V_{SS}	Lower Output Supply	+0.50	+0.75	+1.00	V	
V_{VG}	1st Stage Load Bias	+2.5	+3	+3.5	V	
V_{RD}	Reset Drain Bias	+10.5	+11	+11.5	V	
V_{DD}	Output Buffer Supply	+14.5	+15	+15.5	V	
I_{ddn}	Output Bias Current/Ch.	-5.0	-5.5	-6.0	mA	Note 1
V_{OG}	Output Gate Bias	+4.5	+5.0	+5.5	V	
V_{NWL}	Light Shield Bias	+4.5	+5.0	+15.5	V	
V_{IG}	Test Pin-Input Gate	-0.5	GND	+0.5	V	
V_{SG}	Test Pin-Signal Gate	-0.5	GND	+0.5	V	
V_{IDA} , V_{IDB}	Test Pin-Input Diodes	+14.5	+15.0	+15.5	V	

Notes:
1. A current sink must be supplied for each output. Load capacitance should be minimized so as not to limit bandwidth. See example below.



* Choose values optimized for specific operating frequency. R2 should not be less than 75Ω

Figure 3 - Typical Output Bias/Buffer Circuit

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AC Clock Level Conditions

Symbol	Parameter	Min.	Nom.	Max	Units	Remarks
$V_{\phi 1H}$,$V_{\phi 2H}$	CCD Clocks High	+6.25	+6.5	+7.0	V	
$V_{\phi 1L}$,$V_{\phi 2L}$	CCD Clocks Low	-0.1	GND	+0.1	V	
V_{TGH}	Transfer Clocks High	+3.5	+5.0	+5.5	V	
V_{TGL}	Transfer Clocks Low	-4.5	-5.0	-5.5	V	
$V_{\phi RH}$	Reset Clock High	+4.5	+5.0	+5.5	V	
$V_{\phi RL}$	Reset Clock Low	-4.5	-5.0	-5.5	V	
$V_{\Phi SH}$, $V_{\Phi CH}$	CDS Clocks High	+11	+13	+13.5	V	Note 1
$V_{\Phi SH}$, $V_{\Phi CL}$	CDS Clocks Low	-0.1	+5	+5.5	V	Note 1

Notes:
1. Excessive clock swings may increase feedthroughs.

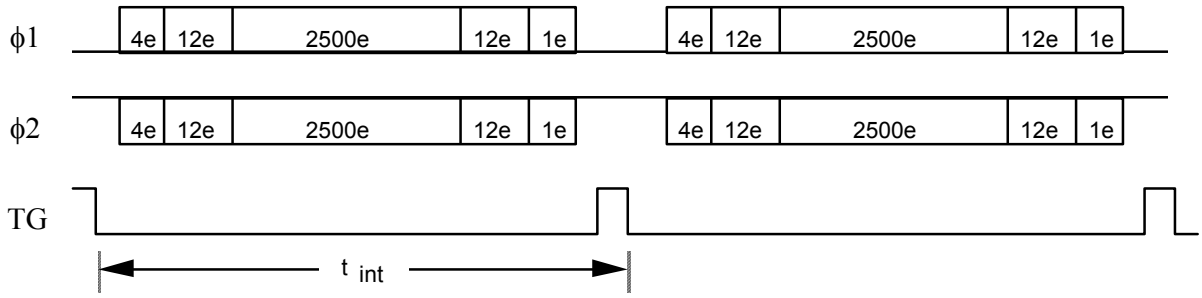
AC Timing

Symbol	Parameter	Position/Width	Remarks
1e	CCD Element Duration	80 ns min.	Note 1
1L= t_{int}	Line/Integration Period	203.2 µs min.	Notes 1, 2
t_{pd}	PD-CCD Transfer Period	800 ns min.	
t_{tg}	Transfer Gate Clear	80 ns min.	
t_{rst}	Reset Pulse Duration	8 ns min. @ $V_{\phi RH}$ min.	
t_{clp}	Clamp Pulse Duration	8 ns min. @ $V_{\phi CH}$ min.	
t_{spl}	Sample Pulse Duration	12 ns min. @ $V_{\phi SH}$ min.	
t_{cd}	Clamp to ϕ2 Delay	4 ns min. @ $V_{\phi CL}$max.	
t_{sd}	Sample to Reset Edge Delay	4 ns min. @ $V_{\phi SL}$ max.	
t_r	CCD Clock Rise Time	10 ns typ.	

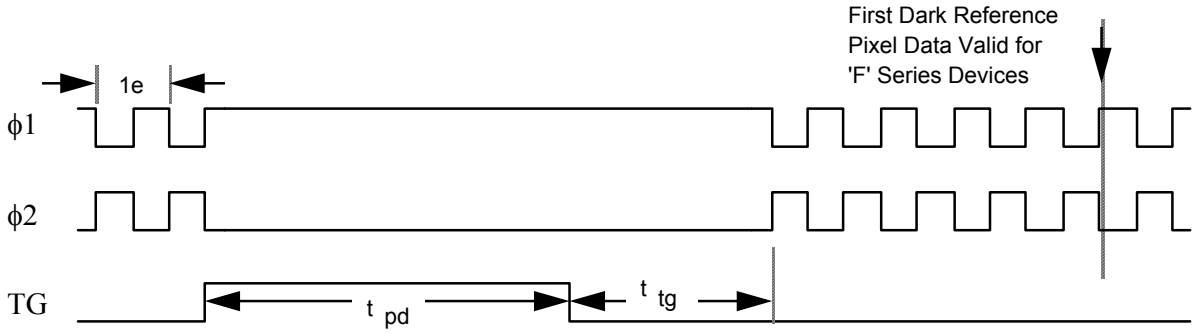
Notes:
1. Values given for 12.5 MHz clock rate.
2. Values given for 2540 counts per line. (4 + 12 + 2500 + 12 +1 + t_{pd} + t_{tg}) = 2540 counts

Timing Diagram

Line Timing:



Photodiode-to-CCD Transfer:



Output Timing:

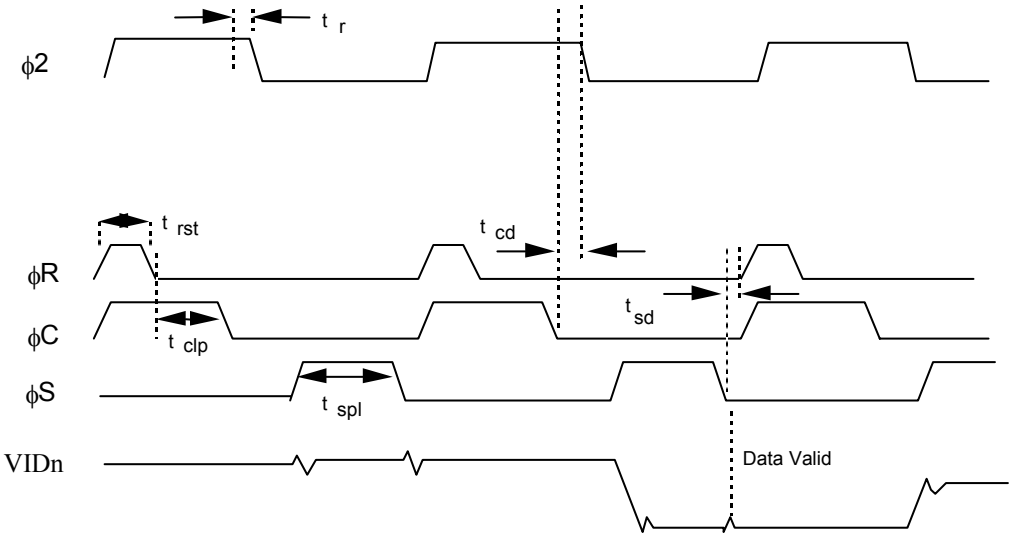


Figure 4 - Device Timing

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Clock Line Capacitance

Specifications given for KLI-5001G under normal operating conditions @ 25^{O}C ambient and f_{CLK} = 12.5 MHz unless otherwise specified.

Symbol	Parameter	Min.	Nom.	Max.	Units	Remarks
C_{H1n}	Phase 1 Clock Capacitance		830		pF	Note 1
C_{H2n}	Phase 2 Clock Capacitance		900		pF	Note 1
C_{TGn}	Transfer Gate Capacitance		130		pF	
C_{PHIR}	Reset Gate Capacitance		8		pF	

Notes:
1. This is the total load capacitance per CCD phase.

Image Specifications

Specifications given for KLI-5001G under normal operating conditions @ 25°C ambient and f_{CLK} = 12.5 MHz unless otherwise specified.

Symbol	Parameter	Min.	Nom.	Max.	Units	Remarks
V_{sat}	Saturation Output Voltage	0.9	1.0	1.1	Vpp	Note 1
$?V_o/?N_e$	Output Sensitivity	3.3	3.7	4.1	μV/e-	
$N_{e,sat}$	Saturation Signal Charge		300K		electrons	
R	Responsivity		3.5		V/μJ/cm^2	Note 6
f_{-3dB}	Output Buffer BW		25		MHz	@ C_{load} = 13 pF
$N_{e,dark}$	RMS Dark Noise			150	electrons	Note 2
SNR	Dynamic Range		66		dB	
I_{dark}	Dark Current			0.01	pA	Note 3
DSNU	Dark Signal Non-Uniformity		1.5	3.0	mV	Note 7
CTE, h	Charge Transfer Efficiency		.99999		-	Note 4
L	Lag		0.4	1	%	1st Field
$V_{o.dc}$	DC Output Offset	8.5	9.5	10.5	Volts	
PRNU	Photoresponse Uniformity			5	% p-p	Note 5
$V_{a/b}$	A/B Chan. DC Offset			200	mV	
$?R_{a/b}$	A/B Chan. Response Offset			5	%	

Notes:

1. Defined as the maximum output level achievable before linearity or PRNU performance is degraded. This value can be affected by choice of output bias load. See DC Conditions section for typical bias circuit. Use of high impedance loads such as Siliconix J511 devices can improve device responsivity and increase the saturated output value.
2. Specified at room temperature (25° C) @ 12.5 MHz data rate. This device utilizes 2-phase clocking for cancellation of driver displacement currents. Hence, symmetry between Φ1 and Φ2 phases must be maintained to minimize clock noise.
3. Measured at room temperature (25° C). Dark current doubles approx. every +9°C.
4. Measured per transfer at 12.5 MHz clock rate. For total line $\eta < (.99999)^{5058} = 0.951$.
5. Low frequency response across array.
6. Measured at 550 nm with standard 7059 coverglass or equivalent (clear glass).
7. Measured at integration time (t_{int}) = 10.0 msec, temperature extrapolated to 25°C.

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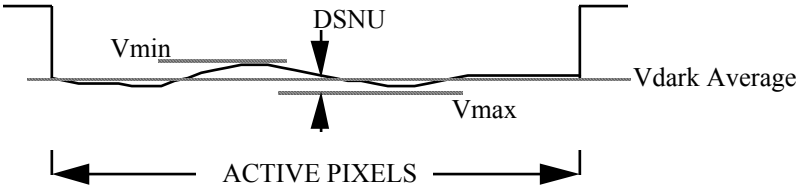

Figure 5 - Dark Signal Non-uniformity Definition

Defect Classification

Test conditions: T=25^{o}C, f_{CLK}=12.5MHz, t_{int}= 203.2µsec

Field	Defect Type	Threshold	Units	Remark	Number
Dark	Bright	10.0	mV	Notes 1, 2	0
Bright	Bright/Dark	5.0	%	Notes 1, 3	0

Notes:
1. Defective pixels will be separated by at least one non-defective pixel within and across channels.
2. Pixels whose response is greater than the average response by the specified threshold. See line 1 in figure below.
3. Pixels whose response is greater or less than the average response by the specified threshold. See lines 2 and 3 in figure below.

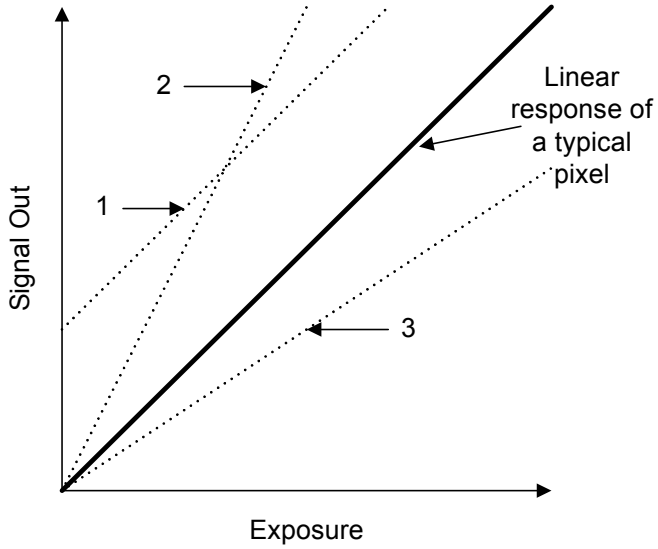

Figure 6 - Defect Classification

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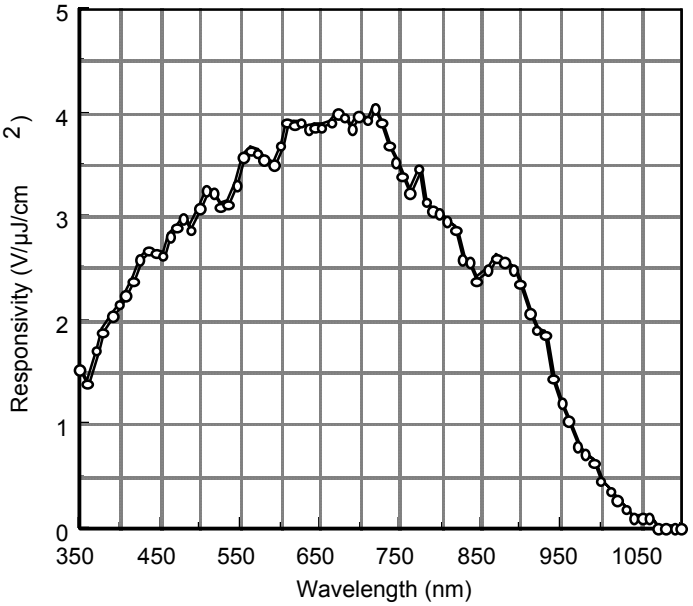

Figure 7 - Device Responsivity

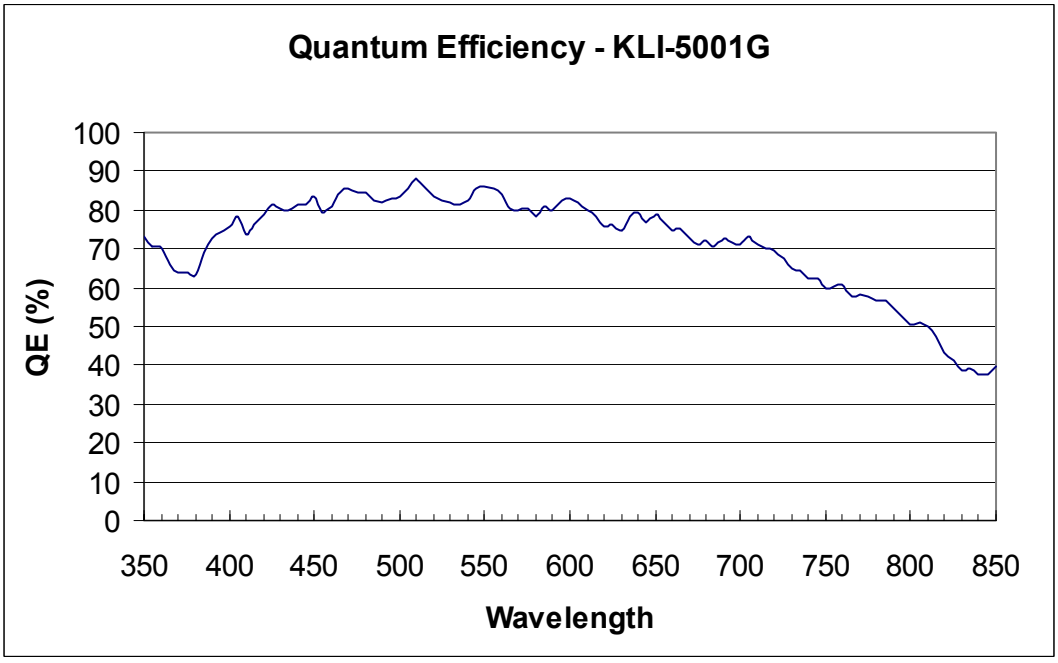

Figure 8 - Device Quantum Efficiency

Quality Assurance and Reliability

Quality Strategy: All image sensors will conform to the specifications stated in this document. This will be accomplished through a combination of statistical process control and inspection at key points of the production process. Typical specification limits are not guaranteed but provided as a design target. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Replacement: All devices are warranted against failure in accordance with the terms of Terms of Sale. This does not include failure due to mechanical and electrical causes defined as the liability of the customer below.

Liability of the Supplier: A reject is defined as an image sensor that does not meet all of the specifications in this document upon receipt by the customer

Liability of the Customer: Damage from mechanical (scratches or breakage), electrical (ESD), or other electrical misuse of the device beyond the stated absolute maximum ratings, which occurred after receipt of the sensor by the customer, shall be the responsibility of the customer.

Cleanliness: Devices are shipped free of mobile contamination inside the package cavity. Immovable particles and scratches that are within the imager pixel area and the corresponding cover glass region directly above the pixel sites are also not allowed. The cover glass is highly susceptible to particles and other contamination. Touching the cover glass must be avoided. See ISS Application Note MTD/PS-0237, Cover Glass Cleaning, for further information.

ESD Precautions: Devices are shipped in static-safe containers and should only be handled at static-safe workstations. See ISS Application Note MTD/PS-0224 for handling recommendations.

Reliability: Information concerning the quality assurance and reliability testing procedures and results are available from the Image Sensor Solutions and can be supplied upon request. For further information refer to ISS Application Note MTD/PS-0292, Quality and Reliability.

Test Data Retention: Image sensors shall have an identifying number traceable to a test data file. Test data shall be kept for a period of 2 years after date of delivery.

Mechanical: The device assembly drawing is provided as a reference. The device will conform to the published package tolerances.

Ordering Information

Please contact Image Sensor Solutions for available part numbers.

Address all inquiries and purchase orders to:

Image Sensor Solutions
Eastman Kodak Company
Rochester, New York 14650-2010
Phone: (585) 722-4385
Fax: (585) 477-4947
E-mail: imagers@kodak.com

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WARNING: LIFE SUPPORT APPLICATIONS POLICY

Kodak image sensors are not authorized for and should not be used within Life Support Systems without the specific written consent of the Eastman Kodak Company. Product warranty is limited to replacement of defective components and does not cover injury or property or other consequential damages.

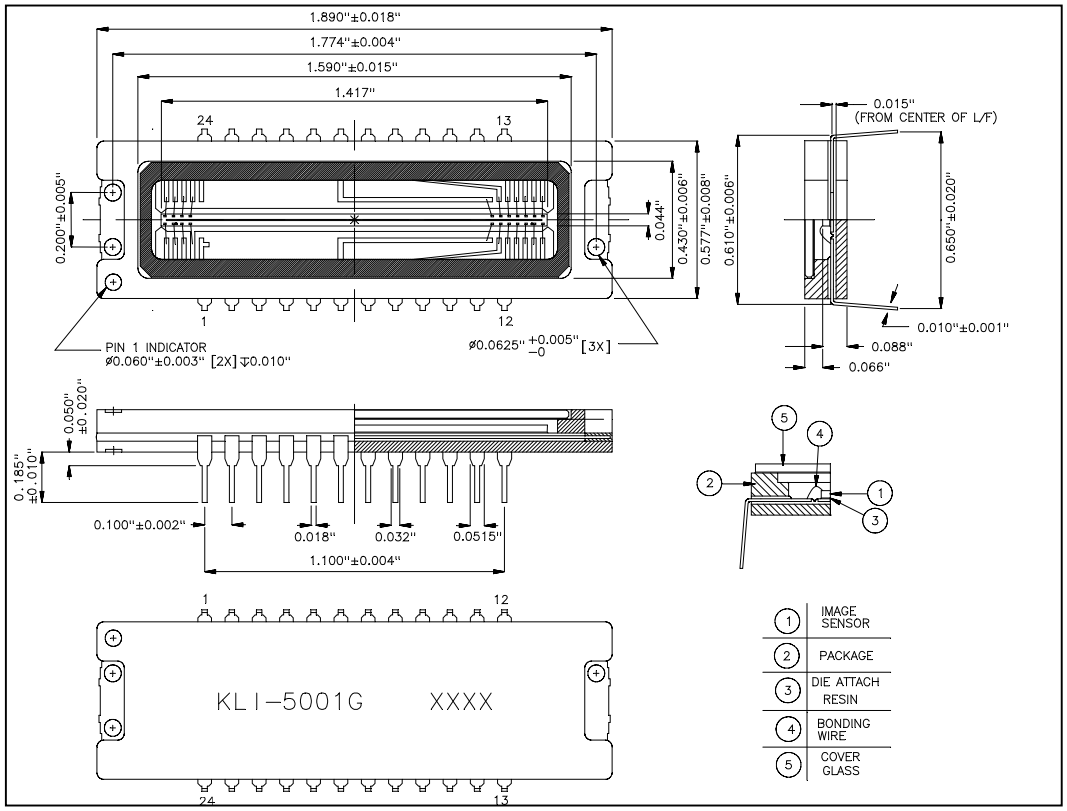

Figure 9 - Device Package Configuration