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PROGRAM

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP)

2010

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IEEE COMPUTER SOCIETY

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) 2010

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The TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) is organized by the Tutorials & Education Group of the IEEE COMPUTER SOCIETY Test Technology Technical Council (TTTC).

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members’ professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology. TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members. TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. To learn more about TTTC offerings and membership benefits, please visit: **http://tab.computer.org/tttc**.

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) 2010
INTRODUCTION

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes in 2010 a comprehensive set of Test Technology Tutorials to be held in conjunction with TTTC sponsored technical meetings. The tutorials are part of the successful annual Test Technology Educational Program (TTEP). TTEP is intended to serve both test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC.

The Test Technology Educational Program 2010 includes tutorial units presented in the following TTTC technical meetings.

- Design, Automation & Test in Europe Conference (DATE ‘10), March 8-12, Dresden, Germany
- Latin American Test Workshop (LATW ‘10), March 28-31, Punta del Este, Uruguay
- VLSI Test Symposium (VTS ‘10), April 19-22, Santa Cruz, California, USA
- International Test Conference (ITC ‘10), October 31 - November 5, Austin, Texas, USA
- Asian Test Symposium (ATS ‘10), December 1-4, Shanghai, China

In addition to the tutorials, certified university courses and industrial seminars related to test technology are also included in TTEP and the participation in these credited similar to TTEP tutorials. For more information please contact the Tutorials and Education Group Chair Dimitris Gizopoulos (dgizop@unipi.gr).

TTEP accomodates a wide range of areas, from mature test topics of high interest to industrial test engineers to emerging test topics with emphasis on novelty. Topics of interest include (but are not limited to):

- Automatic test equipment
- Board-level testing
- Built-In Self-Test
- Defect oriented testing
- Design for testability
- DFT testers

- Diagnosis and debug
- Embedded core testing
- High-speed interface testing
- Interconnect characterization
- Memory testing
- Mixed-Signal/Analog testing
- Nanometer technology testing
- On-line and field testing
- Performance/Delay testing
- Power issues in testing
- System-level testing
- Test economics
- Test synthesis
- Test resource partitioning
- Validation
- Verification
- Wafer testing
- Yield optimization and test

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) 2010 CERTIFICATION

TTEP offers tutorial participants the opportunity to earn official certification from IEEE TTTC. Each full day tutorial at any TTEP site corresponds to four TTEP units and each half-day tutorial corresponds to two TTEP units. Upon completion of each sixteen TTEP units official acreditation in the form of an “IEEE TTTC Test Technology Certificateî ispresented to the participants. TTEP certification units will also be earned in the future for participation in TTEP-certified Industrial Seminars and University Courses. Up to eight out of the sixteen units required for earning an “IEEE TTTC Test Technology Certificate” will be possible to be earned from an Industrial Seminar or a University Course.

REGISTRATION INFORMATION

Attendees can register for TTEP tutorials through the respective conference registration forms. Conference registration is not necessary to attend TTEP tutorials. For further information, contact the TTTC office:

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TTTC-TTEP web page
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TT-01: POWER-AWARE TESTING AND TEST STRATEGIES FOR LOW POWER DEVICES

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Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability. EDA solutions for considering power during test and design-for-test are also discussed in the last part of the tutorial.

TT-02: DESIGN FOR YIELD AND RELIABILITY

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In addition to designing the functionality, today's SOC necessitates designing for yield and reliability. This necessitates embedding a special family of IP blocks, called Infrastructure IP blocks. These are meant to ensure manufacturability of the SOC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This tutorial analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate the use of such Infrastructure IP. Then, it concentrates on several examples of such embedded IPs for detection, analysis and correction.

TT-03: IC YIELD, RELIABILITY AND PROGNOSTIC METHODS USING NANOSCALE TEST STRUCTURES

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The mounting issues of decreased yield and reliability from nanoscale IC processes require advanced approaches to the measurement and mitigation of device degradation and variance. Shrinking process geometries, with their corresponding reduction in device lifetimes, have broad implications to critical applications having long intended design lifetimes. Nanoscale transistor sizes are emerging as a major concern to the long term reliability of safety-critical systems in aerospace and automotive applications. Common semiconductor failure modes include Time Dependent Dielectric Breakdown (TDDB), hot carrier damage (HCI), and Negative Bias Temperature Instability (NBTI). Die-level prognostic test structures can detect and help mitigate the untimely failures in critical systems. These test structures, with variance measurement capabilities, also provide an effective platform for improved process-aware design for improved yields. This tutorial will address concepts of in-situ test structures as a solution to yield, reliability and prognostic applications and include practical application examples.

TT-04: TESTING LOW-POWER INTEGRATED CIRCUITS: CHALLENGES, SOLUTIONS, AND INDUSTRY PRACTICES

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The push for portable, battery-operated, and “cool-and-green” electronics has elevated power consumption as the defining metric of integrated circuit (IC) design. Testing ICs built for such applications requires judicious consideration of test power implications on various aspects of the design cycle (e.g., packaging and power grid design), test engineering (multi-site ATE power supply limitations and board design), power-aware test planning (DFT and ATPG), and developing the enabling EDA tool infrastructure (SW for estimation, reduction and low-power test generation). Furthermore, with power optimization and power management techniques becoming “de-facto” in almost all emerging 45nm and lower chips, systematic testing of these structures and the device in the presence of these structures becomes mandatory. This tutorial is intended to provide an in-depth and up-to-date understanding of low-power IC testing covering (a) dimensions of power-aware testing, (b) techniques for estimation and reduction of test power consumption and (c) test of power managed designs. Case-studies illustrating industrial design deployment practices and existing EDA vendor support will be outlined to illustrate capabilities and gaps in the state-of-the-art.

TT-05: PRACTICES IN ANALOG, MIXED-SIGNAL AND RF TESTING

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The objective of this course is to present existing industry ATE solutions and the alternative solutions to ATE testing for mixed-signal and RF SoCs. These techniques greatly rely upon DFT and BIST structures. Tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, EVM, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs, PMDs, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, delta-sigma converters, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high speed IO interfaces, such as, PCI-Express, and XAUI, etc, and the new design trends in RF systems such as MIMO and SiP based systems and their testability are also presented in this tutorial.

TT-06: PARAMETER VARIATIONS AND LOW-POWER DESIGN: TEST ISSUES AND ON-CHIP CALIBRATION/REPAIR SOLUTIONS

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Variations in device and interconnection characteristics resulting from process imperfections, environmental, (e.g. temperature, voltage), temporal (e.g. NBTI, HCI, TDDB) and workload effects degrade the parametric yield and systems robustness. Such variations result in increased test cost and reduced yield due to test challenges due to new failure mechanisms and increased parametric failure rate. Low-power design techniques such as voltage scaling, body biasing and dual-Vth further aggravate these issues. Post-manufacturing approaches for on-chip calibration and self-repair of degraded systems constitute a promising class of solutions to improve the parametric yield through pro-active delay compensation and enhanced power management. To provide a comprehensive coverage on parameter variations and its impact on test, this tutorial will focus on: 1) intrinsic device physics and process limitations that cause variations; 2) design and test issues associated with parameter variations; 3) impact on yield and reliability; 3) test issues for low-power designs under variations; and 4) on-chip calibration and repair schemes for logic, memory and mixed-signal circuits to improve parametric yield and reliability. On-chip monitoring systems for self-calibration and in-field predictive diagnosis will be presented. Design and test approaches that address within-die parameter variations will be discussed with emphasis on power management. Finally, the tutorial will discuss online adaptation techniques for reliability improvement under temperature fluctuations and device degradations.

TT-07: HIGH-QUALITY AND LOW-COST DELAY TESTING FOR VDSM DESIGNS: CHALLENGES & SOLUTIONS

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As technology scales to 32nm and functional frequency and density continue to rise, many factors and parameters have shown significant impact on design and test of chips. Test engineers must now deal with many new challenges such as IR-drop and power supply noise (PSN) effects on chip performance, signal integrity and crosstalk effects on path delay, high test pattern volume, low fault/defect coverage, small delay defect test pattern generation and fault simulation, process variation effects, high cost of test implementation and application, and un-modeled faults. This tutorial provides practice-oriented solutions to the above challenges. The tutorial is designed to provide design and test engineers with in-depth knowledge on high-quality delay test generation for reduced escape and increased in-field reliability.

TT-08: RELIABILITY, AVAILABILITY, AND SERVICEABILITY OF NETWORKS-ON-CHIP

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This tutorial presents an overview of the issues related to the test, diagnosis and fault-tolerance of NoC-based systems. First, the characteristics of the NoC design (topologies, structures, routers, wrappers, and protocols) are presented, as well as a summary of the terms used in the field and an overview of the existing industrial and academic NoCs. Then, the challenges to test, diagnose and tolerate faults in NoC-based systems are discussed. Current test strategies are presented: re-use of the network for core testing, test scheduling for the NoC reuse, test access methods and interface, efficient re-use of the network, and power-aware and thermal-aware NoC-based SoC testing. In addition, the challenges and solutions for the NoC (interconnects, routers, and network interface) test and diagnosis are presented. Finally, since quality-of-service is one of the main challenges for the NoC use, fault tolerance techniques for the NoC are discussed.

TT-09: THE ECONOMICS OF TEST AND TESTABILITY

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Test economics provides a way of quantifying the costs and benefits of test, and helps a test engineer to choose the most effective test strategy. Most test economics in the past has been concerned with the modeling of these, but real economics is far more sophisticated. Recent work in behavioral economics, known to the public through bestsellers such as “Freakonomics,” “Super Freakonomics” and “Predictably Irrational” have shown that much of what we know about the behavior of economic actors is wrong. For instance, giving consumers too much choice may decrease sales. This tutorial will summarize existing work in test economics, provide background on microeconomic and behavioral economics concepts that are of interest to test and DFT engineers, and will show their applicability to test. The student will emerge with the ability to do traditional cost and benefit modeling, but more importantly, with a much deeper understanding of the economic principles that affect the cost and benefits of test and the profitability of a company. The researcher will emerge with the tools to make a much better case for the benefits of his or her research.

TT-10: TESTING TSV-BASED 3D STACKED ICS

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Three-dimensional stacked ICs offer dense integration of possibly heterogeneous technologies at a small footprint. Interconnection of the various tiers by means of Through-Silicon Vias (TSVs) promises to increase the interconnect bandwidth and performance while lowering power and manufacturing cost, and hence might help the semiconductor industry to extend the momentum of Moore’s Law into the next decade. Testing for manufacturing defects is considered by many as a major, still largely unresolved obstacle to make 3D integrated circuits a reality. There are concerns about the cost, or even worse, feasibility of testing such TSV-based 3D chips. In this tutorial, we present the challenges and solutions for a practical 3D test approach. We discuss the various test flows in 3D-SIC testing based on Known-Good Die (KGD) and Known-Good Stack (KGS) testing, and the role of modular testing. We present the new defects and tests for intra-die defects (e.g., due to wafer thinning) and TSV-based interconnects, and the wafer test access challenges related to KGD and KGS testing. Finally, we discuss an on-chip Design-for-Test (DfT) architecture that supports our approach.

TT-11: THE CONVERGENCE AND INTER-RELATIONSHIP OF YIELD, DESIGN FOR MANUFACTURABILITY AND TEST

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The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm micron and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of testlimited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

TT-12: STATISTICAL ADAPTIVE TEST METHODS TARGETING “ZERO DEFECT” IC QUALITY AND RELIABILITY

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Integrated circuits have traditionally all been tested identically in the manufacturing flow with little sharing of test results between the different test insertions. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize test costs by subjecting “suspect” parts to more extensive testing, and also adaptively bring in additional tests that target the suspected failure mode. The idea is analogous to selective security screening approaches applied at airports. Such statistical methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on production digital and analog circuits from IBM, Intel and LSI Logic, Analog Devices and NXP Semiconductor. Commercial tools offered by a number of new companies that have emerged in the “Adaptive Test” space will also be discussed. Broadly, these aim provide to support for the sharing and leveraging of results from the different tests in the test flow for effective test adaptation and optimization.

TT-13: BRIDGE TO MOORE – IEEE STANDARDS PROVIDE ACCESS TO DEBUG, VALIDATION AND TEST OF EVERMORE COMPLEX ICS; ON ATE, ON BOARD, IN SYSTEM

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Modern chips have a wealth of embedded content and are becoming more complex in architecture with SOCs being made up of multiple cores and with multiple-TAP configurations; and known-good-die being stacked into SIPs and POPs. The need for access to embedded instruments for debug, validation, test and yield analysis on various occasions during a chip’s life-cycle are driving the industry toward “standard” solutions instead of collections of ad hoc access mechanisms. These solutions include IEEE 1149.1, 1500, P1149.7 and P1687, which provide for, respectively, the original standard Test Access Port (TAP), Embedded Core Test, the new Reduced-pin and Enhanced-functionality TAP, and Access and Control of Instrumentation. This tutorial will familiarize the student with these IEEE standards and draft standards, will present the drivers for adoption and use of the standards, will show examples of architectures and usage, and will evaluate pros and cons associated with implementation and use.

TT-14: POST-SILICON VALIDATION AND DEBUG

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Pre-silicon verification methods work with models of the design and are therefore limited by the inherent trade-off between accuracy and runtime. Designs are sent to fabrication when the confidence level is high enough; unfortunately, it still happens that functional and electrical design bugs remain undetected and slip through to prototype silicon. Errors that slip through require fixing as soon as possible once detected on the prototype. Hence, the pre-silicon verification transitions to post-silicon validation and debug upon return of first silicon samples from the fab. The continued need for more effective and efficient debugging methods and instruments is expected to drive innovative and new debug research over the forthcoming years. In this tutorial, we present the basic concepts and the recent advances in this area.

TT-15: DIGITAL TIMING MEASUREMENTS – FROM SCOPES AND PROBES TO TIMING AND JITTER

Wolfgang Maichen, Teradyne, wolfgang@testtechniques.com

As many circuits and applications now enter the Gigahertz frequency arena, accurate digital timing and jitter measurements have become crucial in the design, verification, characterization, and application of electronic circuits. To be successful in this endeavor, an engineer needs a knowledge base covering instrumentation, measurement techniques, jitter and timing concepts, statistics, and transmission line theory. Very often even the most experienced digital test engineer – while mastering some of those subjects – lacks systematic knowledge or experience in others. The goal of this tutorial is to give a compact yet in-depth overview on all those subjects. The emphasis is on practical concepts and real-life guidelines that can be readily put into practice.

IEEE *DESIGN & TEST OF COMPUTERS*

IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers and researchers. D&T features peer-reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

- System Level Design and Test
- Embedded Test Technology
- Low Power Design
- Reconfigurable Systems
- Board and System Test
- Analog and Mixed Signal Design and Test
- System-on-Chip Design and IP Reuse
- Embedded Systems and Software
- Design and Verification/Validation

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IEEE Design&Test of Computers

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Offered Tutorials: TT-03, TT-04 (Half-Day Tutorials)

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http://www.itctestweek.org
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