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ROGRAM
TEST TECHNOLOGY
EDUCATIONAL PROGRAM
(TTEP)
2009
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TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) 2009

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The TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP) is organized by the Tutorials & Education Group of the IEEE COMPUTER SOCIETY Test Technology Technical Council (TTTC).

The Test Technology Technical Council is a volunteer professional organization sponsored by IEEE Computer Society. Its mission is to contribute to members’ professional development and advancement and to help them solve engineering problems in electronic test, and help advance the state-of-the-art in test technology. TTTC is a prime source of knowledge about electronic test via its conferences, workshops, standards, tutorials and education programs, web site, newsletters, and electronic broadcasts. All its activities are led by volunteer members. TTTC membership is open to all individuals directly or indirectly involved in test technology at a professional level. To learn more about TTTC offerings and membership benefits, please visit: **http://tab.computer.org/tttc**.

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP 2009)
INTRODUCTION

The Tutorials & Education Group of the IEEE Computer Society Test Technology Technical Council (TTTC) organizes in 2009 a comprehensive set of Test Technology Tutorials to be held in conjunction with TTTC sponsored technical meetings. The tutorials are part of the successful annual Test Technology Educational Program (TTEP). TTEP is intended to to serve both test and design professionals by offering fundamental education and expert knowledge in state-of-the-art test technology topics and also the opportunity to earn official certification from IEEE TTTC.

The Test Technology Educational Program 2009 includes tutorial units presented in the following TTTC technical meetings.

- Latin American Test Workshop (LATW'09), March 2–5, Buzios, Rio de Janeiro, Brazil
- Design, Automation & Test in Europe Conference (DATE–09), April 20–24, Nice, France
- VLSI Test Symposium (VTS–09), May 3–7, Santa Cruz, California, USA
- European Test Symposium (ETS–09), May 25–29, Sevilla, Spain
- International On-Line Testing Symposium (IOLTS–09), June 24–27, Sesimbra-Lisbon, Portugal
- International Test Conference (ITC–09), November 2–6, Austin, Texas, USA
- Asian Test Symposium (ATS–09), November 23–26, Taichung, Taiwan

In addition to the tutorials, certified university courses and industrial seminars related to test technology are also included in TTEP and participation in these credited similar to TTEP tutorials. For more information please contact the Tutorials and Education Group Chair Dimitris Gizopoulos (*dgizop@unipi.gr*).

TTEP accommodates a wide range of areas, from mature test topics of high interest to industrial test engineers to emerging test topics with emphasis on novelty. Topics of interest include (but are not limited to):

- Automatic test equipment
- Board-level testing
- Built-In Self-Test
- Defect oriented testing

- Design for testability
- DFT testers
- Diagnosis and debug
- Embedded core testing
- High-speed interface testing
- Interconnect characterization
- Memory testing
- Mixed-Signal/Analog testing
- Nanometer technology testing
- On-line and field testing
- Performance/Delay testing
- Power issues in testing
- System-level testing
- Test economics
- Test synthesis
- Test resource partitioning
- Validation
- Verification
- Wafer testing
- Yield optimization and test

TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP 2009) CERTIFICATION

TTEP offers tutorial participants the opportunity for earning official certification from IEEE TTTC. Each full day tutorial at any TTEP site corresponds to four TTEP units and each half-day tutorial corresponds to two TTP units. Upon completion of each sixteen TTEP units official acreditation in the form of an "IEEE TTTC Test Technology Certificate" is presented to the participants. TTEP certification units will also be earned in the future for participation in TTEP-certified Industrial Seminars and University Courses. Up to eight out of the sixteen units required for earning an "IEEE TTTC Test Technology Certificate" will be possible to be earned from an Industrial Seminar or a University Course.

REGISTRATION INFORMATION

Attendees can register for TTEP tutorials through the respective conference registration forms. Conference registration is not necessary to attend TTEP tutorials. For further information, contact the TTTC office:

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TEST TECHNOLOGY EDUCATIONAL PROGRAM (TTEP 2009)

TT-01: ADVANCED TESTING AND TEST DRIVEN SELF-TUNING OF MIXED-SIGNAL/RF CIRCUITS AND SYSTEMS

Jacob A. Abraham, University of Texas at Austin (jaa@cerc.utexas.edu) – Abhijit Chatterjee, Georgia Institute of Technology (chat@ece.gatech.edu)

The impact of process uncertainties on high-speed mixed-signal/RF circuits arising from technology scaling must be taken into account during circuit design and manufacturing test. This tutorial develops advanced mixed-signal/RF test techniques that allow complex specifications to be evaluated at low cost and post-manufacture self-tuning techniques that allow high yield improvement to be achieved.

TT-02: RELIABILITY, AVAILABILITY, AND SERVICEABILITY OF NETWORKS-ON-CHIP

Erika Cota, PPGC – Instituto de Informatica – UFRGS (erika@inf.ufrgs.br)
Marcelo Lubaszewski, PPGEE/PGMICRO – Electrical Eng. Dept. – UFRGS (luba@ece.ufrgs.br)

This tutorial presents an overview of the issues related to the test, diagnosis and fault-tolerance of NoC-based systems. First, the characteristics of the NoC design (topologies, structures, routers, wrappers, and protocols) are presented, as well as a summary of the terms used in the field and an overview of the existing industrial and academic NoCs. Then, the challenges to test, diagnose and tolerate faults in NoC-based systems are discussed. Current test strategies are presented: re-use of the network for core testing, test scheduling for the NoC reuse, test access methods and interface, efficient reuse of the network, and power-aware and thermal-aware NoC-based SoC testing. In addition, the challenges and solutions for the NoC (interconnects, routers, and network interface) test and diagnosis are presented. Finally, since quality-of-service is one of the main challenges for the NoC use, fault-tolerance techniques for the NoC are discussed.

TT-03: DESIGN, TEST, & YIELD IMPLICATIONS AND ANALYSIS UNDER PARAMETER VARIATIONS

Kaushik Roy, Purdue University (kaushik@purdue.edu)

In the sub-65nm regime parameter variations have become increasingly important and can affect yield of integrated circuits severly. The minimum geometry transistors, especially in memories, can lead to new variationinduced failures. In the first part of the tutorial, we will classify different parameter variations -- die to die and within die -- and will consider the impact of variations and corresponding failures in memories. Techniques to improve memory tests to catch such process variation induced failures will be discussed and self-tuning and self-repairing techniques to improve yield will be

discussed. In the second part of the tutorial, we will consider both logic and signal processing systems under parameter variations and discuss test and yield improvement techniques using sensors that senses the process corner that the chip is in, to provide corrective action. Test and validation of such systems with sensors and self-tuning features will be considered.

TT-04: DESIGN FOR MANUFACTURABILITY

Yervant Zorian, Virage Logic (zorian@viragelogic.com) – Juan-Antonio Carballo, IBM (jantonio@us.ibm.com)

In addition to designing the functionality, today's SOC necessitates designing for manufacturability, yield and reliability. Such requirements is fundamentally transforming the current SoC design methodology. Techniques for enhancing manufacturability, yield, and reliability or "DFX" include yield enhancement techniques, resulution enhancement techniques, new or restricted design rules, variability-aware design, and the addition of a special family of embedded IP blocks, called Infrastructure IP blocks. The latter blocks are meant to ensure manufacturability of the SOC and to achieve adequate levels of yield and reliability. The Infrastructure IP leverages the manufacturing knowledge and feeds back the information into the design phase. This tutorial analyzes the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate the use of the above DFX techniques. Then, it concentrates on several examples of each of these techniques.

TT-05: ADVANCED TOPICS AND RECENT ADVANCES IN SILICON DEBUG AND DIAGNOSIS

Srikanth Venkataraman, Intel Corporation (srikanth.venkataraman@intel.com) – Miron Abramovici, DAFCA (miron@dafca.com)
Robert Aitken, ARM (rob.aitken@arm.com)

The increasing design complexity along with the emergence of new failure mechanisms in the nanometer regime has significantly increased the complexity of verification, validation and manufacturing ramp of ICs. When pre-silicon verification and validation uncovers design bugs, the process of diagnosing and debugging these issues is called design error diagnosis. From the time a new chip comes back from the fab until high-volume production can start, the chip goes through functional silicon validation and debug to make sure it is free of design errors, and defect diagnosis and failure analysis to solve yield problems. These activities, referred to as silicon debug and diagnosis, have become the most time-consuming phase in the development cycle of a new design, increasing to about 33% of the total time. This is a consequence of the increasing design complexity, along with the emergence of

new failure mechanisms in nanometer technologies. Long time-to-volume and low manufacturing yield have a great detrimental impact on the economic viability and the overall success of a product. This tutorial covers the state of the art and the full spectrum of topics in silicon validation and debug and defect diagnosis ranging from the basic concepts to advanced applications and new DFD techniques. We will also describe successful debug and diagnosis methods used in real industrial products, industrial experiences, and case studies. Finally we will discuss future directions and challenges.

TT-06:STATISTICAL SCREENING METHODS TARGETING "ZERO DEFECT" IC QUALITY AND RELIABILITY

Adit D. Singh, Auburn University (adsingh@auburn.edu)

Integrated circuits have traditionally all been tested identically in the manufacturing flow. However, as the detection of subtle manufacturing flaws becomes ever more challenging and expensive in aggressively scaled nanometer technologies, innovative new statistical screening methods are being developed that attempt to improve test effectiveness and optimize testcosts by adaptively subjecting "suspect" parts to more extensive testing. The idea is similar to security screening at airports. Such methods fall into two broad categories: those that exploit the statistics of defect distribution on wafers, and those that exploit the correlation in the variation of process and performance parameters on wafers. This tutorial presents test methodologies that span both these categories, and illustrates their effectiveness with results from a number of recently published experimental studies on industrial production circuits.

TT-07: PARAMETER VARIATIONS AND SELF-CALIBRATION/SELF-REPAIR SOLUTIONS IN NANOMETER TECHNOLOGIES

Saibal Mukhopadhyay, Georgia Institute of Technology (saibal@ece.gatech.edu) – Rahul Rao, IBM T. J. Watson Research Center (raorahul@us.ibm.com)
Praveen Elakkumanan, IBM Semiconductor R&D Center (pelakkum@us.ibm.com) – Swarup Bhunia, Case Western Reserve University (skb21@case.edu)

Device level parameter variations caused by process imperfections, environmental variations (e.g. temperature) and aging effects (e.g. NBTI, HCI) manifest as variations in delay, leakage and noise margin in logic and memory circuits leading to manufacturing yield loss and reliability degradation. In this tutorial, we focus on post-silicon on-chip self-calibration and self-repair schemes for logic and memory circuits that can that can improve parametric yield and reliability. This tutorial will discuss causes of parametric variations and aging effects; present efficient techniques on-chip and on-line sensing and characterization of manufacturing variations and aging effects in device and circuit parameters; discuss circuit and system level techniques for

selfcalibration and self-repair of logic and memory circuits; and explore selfrepairing systems for mixed signal design. The audience will be introduced to the post-silicon strategies for self-calibration and self-repair that constitutes a promising class of solutions to address variation induced parametric failures and associated test challenges.

TT-08: SYSTEM-IN-PACKAGE TEST STRATEGIES

Yervant Zorian, Virage Logic (zorian@viragelogic.com)

Today's miniaturization and performance requirements result in the usage of high density advanced packaging technologies, such as System-in-Package (SiP), 3D integration, Direct Chip Attach, Package-inpackage. Due to their physical access limitation,the complexity and cost associated with their test and diagnosis are considered major issues facing their use. This tutorial provides comprehensive knowledge of test solutions for advanced packages by placing particular emphasis on: test and debug approaches for bare dies; testing schemes for 3D packages, flip-chips used in direct chip attach, and SiP packages; testing bare substrates, and finally test, diagnosis and repair techniques for assembled modules.

TT-09: POWER-AWARE TESTING AND TEST STRATEGIES FOR LOW POWER DEVICES

Patrick Girard, LIRMM/CNRS (girard@lirmm.fr) – Nicola Nicolici, McMaster University (nicola@ece.mcmaster.ca)
Xiaoqing Wen, Kyushu Institute of Technology (wen@cse.kyutech.ac.jp)

Power dissipation is becoming a critical parameter during manufacturing test as the device can consume much more power during test than during functional mode of operation. In the meantime, elaborate power management strategies, like voltage scaling, clock gating or power gating techniques, are used today to control the power dissipation during functional operation. The usage of these strategies has various implications on manufacturing test, and power-aware test is therefore increasingly becoming a major consideration during design-for-test and test preparation for low power devices. This tutorial provides knowledge in this area. It is organized into three main parts. The first one gives necessary background and discusses issues arising from excessive power dissipation during test application. The second part provides comprehensive knowledge of structural and algorithmic solutions that can be used to alleviate such problems. The last part surveys low power design techniques and shows how these low power devices can be tested safely without affecting yield and reliability.

TT-10: ANALYZING, MODELING AND UNDERSTANDING HIGH-SPEED INTERFACES USING TIME DOMAIN REFLECTOMETRY

Wolfgang Maichen, Teradyne (wolfgang@testtechniques.com)

Keeping theory and mathematics to a minimum, this presentation aims to develop an intuitive understanding of high-speed transmission line behavior. This is an important topic for anyone concerned with design, analysis, troubleshooting, or qualification of high-speed interconnects like backplanes, printed circuit boards, high-speed serial links, cables, connectors, sockets etc. Using a compact time domain reflectometer (TDR) we will perform a variety of life, real-time demonstrations (free-hand experiments) to investigate topics like delay and characteristic impedance, reflections, impedance mismatches, parasitics, lumped and distributed crosstalk, differential signaling, and others. We will show how to extract quantitative data for transmission lines and parasitics and use them to build equivalent models to be used in transmission path simulation. Towards the end we will compare TDR with the traditionally more common analysis based on network analyzers and show strengths and weaknesses in either approach.

TT-11: POST-SILICON VALIDATION AND DEBUG

Nicola Nicolici, McMaster University (nicola@ece.mcmaster.ca) – Bart Vermeulen, NXP Semiconductors (bart.vermeulen@nxp.com)
Jason Stinson, Intel (jason.stinson@intel.com)

Pre-silicon verification methods work with models of the design and are therefore limited by the inherent trade-off between accuracy and runtime. Designs are sent to fabrication when the confidence level is high enough; unfortunately, it still happens that functional and electrical design bugs remain undetected and slip through to prototype silicon. Errors that slip through require fixing as soon as possible once detected on the prototype. Hence, the pre-silicon verification transitions to post-silicon validation and debug upon return of first silicon samples from the fab. The continued need for more effective and efficient debugging methods and instruments is expected to drive innovative and new debug research over the forthcoming years. In this tutorial, we present the basic concepts and the recent advances in this area.

TT-12: THE ECONOMICS OF TEST AND TESTABILITY

Scott Davidson, Sun Microsystems (scott.davidson@sun.com) – Helen Colby, Rutgers University (HColby@rci.rutgers.edu)
Louis Ungar, A.T.E. Solutions (Testable1@aol.com)

Test economics provides a way of quantifying the costs and benefits of test, and helps a test engineer choose an effective test strategy. Classical microeconomics is far more sophisticated than what is found in test economics papers. Recent work in behavioral economics, known to the public through bestsellers such as "Freakonomics," has shown that classical assumptions about the behavior of economic actors are wrong. This tutorial will summarize existing work in test economics, provide background on microeconomic and behavioral economics concepts that are of interest to test and DFT engineers, and will show their applicability to test. The student will emerge with the ability to do traditional cost and benefit modeling, and with a deeper understanding of the economic principles that affect the cost and benefits of test. The researcher will emerge with the tools to make a much better case for the benefits of proposed research.

TT-13: HIGH-QUALITY AND LOW-COST DELAY TESTING FOR VDSM DESIGNS: CHALLENGES & SOLUTIONS

Mohammad Tehranipoor, University of Connecticut (tehrani@engr.uconn.edu) – Krishnendu Chakrabarty, Duke University (krish@ee.duke.edu)
Jeff Rearick, AMD (jeff.rearick@amd.com)

As technology scales to 32nm and functional frequency and density continue to rise, many factors and parameters have shown significant impact on design and test of chips. Test engineers must now deal with many new challenges such as IR-drop and power supply noise (PSN) effects on chip performance, signal integrity and crosstalk effects on path delay, high test pattern volume, low fault/defect coverage, small delay defect test pattern generation and fault simulation, process variation effects, high cost of test implementation and application, and un-modeled faults. This tutorial provides practice-oriented solutions to the above challenges. The tutorial is designed to provide design and test engineers with in-depth knowledge on high-quality delay test generation for reduced escape and increased in-field reliability.

TT-14: THE CONVERGENCE AND INTER-RELATIONSHIP OF YIELD, DESIGN FOR MANUFACTURABILITY AND TEST

Srikanth Venkataraman, Intel Corporation (srikanth.venkataraman@intel.com) – Robert Aitken, ARM (rob.aitken@arm.com)

The tutorial goal is to show how design for yield (DFY) and design for manufacturability (DFM) are tightly coupled into what we conventionally think of as test. As process geometries shrink, the line between defects and process variation blurs to the point where it is essentially non-existent. As feature sizes reduced to 90 nm micron and below, systematic mechanism-limited yield loss began to appear as a substantial component in yield loss due to the interaction between design and manufacturing. The basics of yield and what fabs do to improve defectivity and manage yield are described. DFM techniques to analyze the design content, flag areas of design that could limit yield, and make changes to improve yield are discussed. In DFM/DFY circles, it is common to speak of defect limited yield, but it is less common to think of testlimited yield, yet this concept is common in DFT (e.g. IDDQ testing, delay testing). Test techniques to close the loop by crafting test patterns to expose the defect prone feature and circuit marginality through ATPG, and by analyzing silicon failures through diagnosis to determine the features that are actually causing yield loss and their relative impact are covered. This tutorial will provide background needed for DFT practitioners to understand DFM and DFY, and see how their work relates to it. The ultimate goal is to spur attendees to conducting their own research in the area, and to apply these concepts in their jobs.

TT-15: PRACTICES IN ANALOG, MIXED-SIGNAL AND RF TESTING

Salem Abdennadher, Intel (salem.abdennadher@intel.com) – Saghir Shaikh (saghir.shaikh@gmail.com)

The objective of this course is to present existing industry ATE solutions and alternative solutions to ATE testing for mixed-signal and RF SoCs. These techniques greatly rely upon DFT and BIST structures. Tutorial presents the basic concepts in analog and RF measurements (eye diagram, jitter, gain, power compression, harmonics, noise figure, phase noise, BER, etc.). Several industrial examples of production testing of mixed-signal and RF devices, such as, SERDES transceivers, PHYs,, HSIO, and RF transceivers are also presented. The block-DFT solutions are presented for PLLs, CDR, equalizers, filters, mixers, AGC, LNAs, DACs and ADCs. The testing of high speed IO interfaces, such as, PCIe, and SATA, etc, and the new design trends in RF systems such as MIMO and SiP based systems and their testability are also presented in this tutorial.

IEEE *DESIGN & TEST OF COMPUTERS*

IEEE D&T is a bimonthly magazine published by the IEEE Computer Society in cooperation with the IEEE Circuits and Systems Society specifically for design and test engineers and researchers. D&T features peer-reviewed original work describing methods and practices used to design and test electronic product hardware and supportive software. Articles explore current practices and experience in:

- System Level Design and Test
- Embedded Test Technology
- Low Power Design
- Reconfigurable Systems
- Board and System Test
- Analog and Mixed Signal Design and Test
- System-on-Chip Design and IP Reuse
- Embedded Systems and Software
- Design and Verification/Validation

In addition, D&T publishes tutorial articles, perspectives, roundtable discussions, book reviews, viewpoints, conference reports, panel summaries, and standards updates contributed by authors working in the industry.

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SPECIAL ISSUES: The theme issues for 2009 are (please check D&T website for submission instructions and deadlines):

Jan/Feb	IEEE Std 1500 and Its Usage
March/April	Managing Emerging SoC Development
May/June	IEEE Std 1500 and Its Usage Part 2 and Meta-modeling for Design and Test
July/August	High-Level Synthesis
Sep/Oct	3D Integration and ITC Special Section
Nov/Dec	Design for Reliability at 32nm and Beyond

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