TTTC/TTEP TEST CLINIC @ ITC'10

In addition to the regular tutorials, TTTC/TTEP is offering at ITC'10 a Test Clinic, particularly geared towards newcomers to the area of test, such as new test engineers and students pursuing graduate studies in test. Its key objective is to offer a broad yet comprehensive review of basic test topics in an accessible way to the lay audience. This year's topic will be *Logic and Memory Testing for SoCs*.

This Test Clinic will be a full-day event on Monday, November 1st. Upon its completion, an official recognition in the form of an IEEE TTTC Test Technology Certificate will be presented to each participant.

For further information regarding TTEP, please visit *http://tab.computer.org/tttc/teg/ttep/* *The Test Clinic requires a separate registration fee* (see ITC registration form or *www.itctestweek.org* for further information). *Admission for on-site registrants is subject to availability.*

Test Clinic attendees receive study material, breakfast, lunch, and coffee breaks. The study material includes a hardcopy of the presentation and bibliographical material. Test Clinic registration, coffee and pastry are available at 7:00 a.m. on Monday.

Test Clinic @ ITC'10: Logic and Memory Testing for SoCs

Monday, November 1st, 8:30 a.m. – 4:30 p.m.

Presenters

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Abstract

Testability is a fundamental requirement for today's systems-on-chip. These integrated circuits are typically designed based on Intellectual Property (IP) block integration to make the best use of millions of gates available. Logic and memory IP blocks require adequate fault detection, silicon debug and yield optimization. All of which are based on testability infrastructure build into the systems-on-chip. This tutorial presents the fundamental knowledge base that any designer or testability engineer must have in order to fulfill the current industrial best practices for design-for-testability. The tutorial discusses the requirements for block-level test architecting, at-speed design practices, scan compression, memory self-test, debug and repair, test interface standardization efforts such as IEEE Std 1149.1 (JTAG) and IEEE Std. 1500, and integration for System-on-Chip level and beyond. Actual industrial experiences will be shared with the audience whenever possible.