Estimation of Statistical Variation in Temporal NBTI Degradation and its Impact on Lifetime Circuit Performance

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Abstract—Negative bias temperature instability (NBTI) in MOSFETs is one of the major reliability concerns in sub-100nm technologies. So far, studies of NBTI and its impact on circuit performance have assumed an average behavior of the degradation process. However, in very short channel devices, finite number of Si–H bonds in the channel can induce a statistical random variation of the degradation process. This results in significant random \( V_t \) variations in PMOS transistor. The NBTI induced variation depends on operating temperature and the effective stress period for the specific device. In this paper, we analyze the impact of stochastic temporal NBTI variations and propose a compact circuit level \( V_t \) model. Using the proposed model, we show how temporal \( V_t \) variations can affect the lifetime performance of different circuit topologies including 6T SRAM cell and random combinational logic circuits.

I. INTRODUCTION

With aggressive scaling of transistor dimension in each technology generation, digital ICs are often exposed to a severe level of stress conditions during its operation even with a nominal workload. Some of these stress conditions including elevated operating temperature and increased vertical oxide field have brought up a serious lifetime reliability concern in sub-100nm MOSFETs known as the negative bias temperature instability (NBTI) [1], [2]. NBTI is a PMOS specific aging effect which particularly increases the transistor threshold voltage (\( V_t \)) and reduces the drive current with time. A set of experiments and corresponding analysis [3]–[5] has shown that NBTI is a result of continuous trap generation in Si–SiO\(_2\) interface of transistor. These traps originate from Si–H bonds in negatively biased channel, generating traps in the channel interface. However, with time, these bonds break during stressed operating conditions (i.e., ON-state, negative gate bias under elevated temperature) and generate interfacial traps which contribute to an increase in \( V_t \). Such changes in transistor \( V_t \) can significantly affect the lifetime performance (i.e., power, speed and failure rate) of digital circuits, and in the worst case, result in a complete parametric failure of a system. As a result, it has now become essential to accurately estimate the impact of NBTI at different phases of design cycle so that proper corrective actions can be easily taken.

Recently, number of works have been proposed in the literature to analyze and quantify the impact of NBTI degradation in lifetime circuit performance. In [6], it was shown that the maximum circuit delay degradation due to NBTI closely follows the same fractional power dependency to time as the \( V_t \) degradation with an appropriate scale factors. The authors in [7] have further improved the circuit compatible NBTI model to consider technology dependent parameters and AC relaxation effects. Authors from [8] have proposed an efficient AC NBTI model for circuit simulations. In [9], [10], it was shown that the NBTI degradation in memory circuits can increase the failure rate of the system.

Though these previous efforts efficiently addressed the circuit performance impact under NBTI degradation, they all commonly neglect one of the key features of the NBTI mechanism – the statistical variation of the degradation process. Similar to the random dopant fluctuation (RDF) effects [11], in very short channel devices, the number of Si–H bonds in the device (average number of Si–H bonds \( N_{Si-H} \) in bulk CMOS is \( \sim 10^{12}/cm^2 \)) are few, ranging from tens to hundreds of pairs depending on the specific technology. Due to the finite number of Si–H bonds, breaking and re-passivation of Si–H bonds can experience a significant statistical fluctuation during the degradation process [12], [13]. Such statistical variation of NBTI process results in an additional random variation of \( V_t \) on top of the nominal degradation (i.e., static NBTI) and needs to be considered during the performance analysis of digital circuits. Unlike the random variations due to RDF, NBTI induced \( V_t \) variations depend on the operating temperature and the effective stress period that a particular transistor experiences. Hence, there is a need to develop effective compact circuit-level \( V_t \) model that considers such NBTI variation.

In this paper, for the first time, we analyze the impact of random NBTI variations in the lifetime circuit performance. Specifically, we first propose a compact \( V_t \) model considering the temporal NBTI variation in short channel devices. Then using the proposed model, we analyze the impact of NBTI variation in various circuit topologies including 6T SRAM cell and random logic circuits. Finally, we show that the impact of random NBTI variations on top of the nominal degradation can result in a reduced circuit lifetime which needs to be considered during the initial design phase.

The rest of the paper is organized as follows. In section 2, we introduce the nominal NBTI model using the reaction diffusion (RD) framework. We further improve the RD based temporal \( V_t \) model to incorporate the impact of statistical NBTI variation. In section 3, using the proposed statistical NBTI model, we analyze the impact of random NBTI variation in lifetime circuit performance for different applications. We conclude the paper in section 4.

II. TRANSISTOR \( V_t \) MODEL UNDER NBTI

In this section, we introduce temporal \( V_t \) model under NBTI degradation considering the statistical variation in the number of generated traps in the channel interface. First, we review the nominal \( V_t \) degradation model using the reaction diffusion (RD) framework. Based on the nominal model, we setup a statistical NBTI model in the later part of the section.

A. Nominal \( V_t \) model using RD framework

NBTI results in temporal increase of threshold voltage due to the generation of traps at Si–SiO\(_2\) interface in negatively biased PMOS transistors at elevated temperature. Numerous researchers have discussed the mechanism of NBTI in terms of reaction diffusion model (RD) [2]–[4]. RD model interprets NBTI as a consequence of interaction of inversion layer holes with hydrogen-passivated Si...
atoms. Under negative gate bias condition, cold holes from the inversion layer can break $Si-H$ bonds, creating interfacial traps (in donor-like state) and neutral $H$ atoms. Generated interface traps account for an increase in device threshold voltage as follows,

$$\Delta V_t(t) = \frac{qN_{IT}}{C_{ox}} = \frac{\mu}{C_{ox}} \times K_{DC} \times \epsilon^n$$

where $N_{IT}$ is the density of interfacial traps and $C_{ox}$ is the oxide capacitance. Solution of RD model produces a fractional power law model of NBTI shown in the right hand side of Eq. (1) with a fixed time exponent of $n$. The value of $n$ depends on the specific process mechanism. In our work, assuming $H_2$ diffusion [18] mechanism, we have employed the time exponent value of 1/6. $S_p$ denotes the signal probability of the transistor (i.e., effective ON time of PMOS transistor), and is used to identify the AC relaxation effect of the NBTI process. AC dependency function $f_{AC}$ can be computed using the RD framework [3], [7], [8]. $K_{DC}$ is a temperature dependent constant and can be expressed as follows [3]–[5], [7].

$$\Delta K_{DC} \propto \beta \times E_{ox}^{\frac{3}{2}} \times e^{\frac{K_{Ac}}{E_{ox}}} \times e^{-\frac{E_{Ac}}{K_{T}}}$$

(2)

where $\beta$, $E_{ox}$, $E_{Ac}$, and $E_{Ac}$ are the constant factor, vertical oxide field, activation energy, field acceleration factor, and the thermal voltage ($kT/q$), respectively. $K_{DC}$ describes the temperature, bias, oxide thickness, and other technology dependent factors associated with NBTI degradation.

B. Statistical $V_t$ model

The RD based $V_t$ model introduced in the previous section assumes nominal degradation without considering the statistical variation in the underlying degradation process. In reality, due to the finite number of $Si-H$ bonds in the channel, breaking and re-passivation of these bonds experience stochastic fluctuations. This phenomenon is similar to the random $V_t$ variation induced by the number and the placement of dopant atoms in the channel, known as the random dopant fluctuation (RDF) effect. General framework of NBTI variation has been proposed by Stewart in [13]. They have modeled the number of broken bonds $N_{IT}$ in the channel as a Poisson random variable. Under this assumption and using Eq. (1), we can write,

$$\sigma^2_{N_{IT}} = \mu_{N_{IT}} = \frac{C_{ox} \mu_{\Delta V_t}}{q} = \frac{C_{ox} \mu_{\Delta V_t}}{q^k}$$

where $\sigma^2_{N_{IT}}$ and $\sigma_{N_{IT}}$ represent the mean and the standard deviation (STD) of $N_{IT}$. $\mu_{\Delta V_t}$ is the nominal (mean) $V_t$ degradation due to the NBTI, given by Eq. (1). $A_C$ is the effective channel area. From the relationship given by Eqs. (1) and (3), we can derive STD of $\Delta V_t$ ($\sigma_{\Delta V_t}$) as follows,

$$\sigma^2_{\Delta V_t} = \mu^2_{\Delta V_t} \left( \frac{q}{C_{ox}} \right)^2 = \frac{q^2 \mu_{\Delta V_t}}{C_{ox}} \Rightarrow \sigma_{\Delta V_t} \approx \frac{1}{12}$$

(4)

Eq. (4) shows that since nominal $V_t$ degradation follows a fractional power law (Eq. (1)), $\sigma_{\Delta V_t}$ also maintains a power relationship with respect to temperature with a fixed exponent of 1/12. Note that unlike the nominal $V_t$ degradation (i.e., $\mu_{\Delta V_t}$, Eq. (1)), NBTI induced $V_t$ STD depends on the transistor dimension $A_C$ with a reverse square relationship.

The existence of this temporal variation effect can incur a significant error in estimating the lifetime $V_t$ degradation if not considered. Fire 1(a) plots the temporal change of $V_t$ under NBTI variations for 3 years operating time at 125°C. An AC stress signal with a fixed 50% signal probability is assumed. For this particular simulation, a minimum size PMOS transistor from 32nm Predictive Technology Node (PTM) [14] was referred for extracting all relevant technology dependent parameters. The three curves in Fig. 1(a) represent the nominal ($\mu_{\Delta V_t}$), STD ($\sigma_{\Delta V_t}$), and 99% CDF point of the $V_t$ change. When the operating time reaches 10^8 seconds (∼3 years), STD of $V_t$ is approximately 15.1mV (∼7.7% of nominal $V_t$). It can be also observed that due to the increase in $V_t$ STD with time, statistical limit (e.g., 99% CDF plot) of NBTI variation can be larger than the nominal degradation by more than 34% in 3 years lifetime.

Note that due to the size ($A_C$) dependency of temporal STD degradation, NBTI variation can have more severe impact in scaled technologies. Fig. 1(b) shows the NBTI variations after 3 years stress at three different predictive technology nodes - 22nm, 32nm, and 45nm nodes. Relative magnitude (%) of mean NBTI shift ($\mu_{\Delta V_t}$) and STD of NBTI induced $V_t$ variation ($\sigma_{\Delta V_t}$) is plotted. Though the nominal shift remains near constant throughout different technologies (mainly due to relaxed oxide scaling), the relative magnitude of $V_t$ variation increases with technology scaling. We can conclude that the estimation of $V_t$ degradation should always consider the variation in NBTI degradation process in order to obtain its realistic limit. In the following section, we will further show how this variation can impact the lifetime circuit performance under NBTI degradation.

III. PERFORMANCE VARIATION OF DIGITAL CIRCUITS UNDER NBTI DEGRADATION

In the previous section, we developed a compact statistical NBTI model considering the random nature of the $Si-H$ bond breaking in scaled transistors. Using this model, in this section, we explore the impact of NBTI variation in lifetime circuit performance. Note that from the circuit level perspective, NBTI variation closely resembles the nature of RDF induced $V_t$ variation in a sense that it has a complete randomness even among the transistors that are closely
placed in the same chip. Hence, in our work, we will consider both the RDF and the NBTI induced $V_t$ variation ($\sigma_{RDF}$ and $\sigma_{NBTI}$, respectively) at the same time as follows,

$$\sigma_{V_t} = \sqrt{\sigma_{RDF}^2 + \sigma_{NBTI}^2(t)}$$  

(5)

where $\sigma_{V_t}$ represents the total $V_t$ variation after time $t$. Note that in Eq. (5), we have neglected the possible correlation between RDF and NBTI. For example, if $V_t$ is skewed by RDF variation, oxide field and doping concentration also changes, which could have a non-negligible effect in the scale factor $K_{DC}$ of temporal $V_t$ model. In our work, for simplicity, we have not considered the impact of this correlation during the analysis. However, we believe it would be a part of our future work to establish a more accurate NBTI model.

32nm and 22nm PTM files were applied to extract relevant technology parameters for Eq. (5) and to design our example circuits. Specifically, using the $V_t$ model given by Eq. (5), we analyze the impact of NBTI variations in, 1) 6T SRAM array for statistical READ and WRITE failures, and 2) random logic circuits for timing variations.

A. READ & WRITE stability degradation in 6T SRAM cell

In [15], it was shown that the impact of random intra-die variation within different transistors in a single cell can significantly affect the parametric yield of large size SRAM arrays. In this section, we revisit the issues of random process variations in SRAM arrays under the impact of statistical NBTI variations. Fig. 1(c) depicts the schematic diagram of a 6T SRAM cell. For our analysis, we have applied a size ratio of 1:2 between pull-up (PL, PR) and pull-down (NL, NR) transistors, while using a ratio of 1:2 between access (AXL, AXR) and pull-down transistors. Signal probabilities at node $V_L$ and $V_R$ are noted as $S_{PL}$ and $S_{PR}$ (where $S_{PL} + S_{PR} = 1$), respectively.

Impact of random variations in SRAM can be mainly divided into statistical READ and WRITE failures [9], [15]. Weaker PMOS transistors (due to NBTI) can manifest itself to increased READ failures. On the other hand, it also enables faster WRITE operation, reducing statistical WRITE failure probability [9]. Sets of Monte-Carlo (MC) analysis based on HSPICE simulation were employed to observe the impact of statistical READ and WRITE failure probability under NBTI variations.

1) READ stability: In our work, we defined the statistical READ failure event as a cell having a READ static noise margin (SNM) [16] value less than a predefined limit, $SNM_F$. Under such notation, READ failure probability of an SRAM cell can be defined as,

$$P_{RF}(t) = \int_{SNM_F}^{\infty} f_{SNM(t)}(x) dx = \Phi\left(\frac{SNM_F - \mu_{SNM}(t)}{\sigma_{SNM}(t)}\right)$$  

(6)

where $f_{SNM}(t)$ represents the probability density function (PDF) of SNM at time $t$, and can be approximated as a Gaussian random variable. $\mu_{SNM}(t)$ and $\sigma_{SNM}(t)$ are the mean and the STD of SNM at time $t$ and can be extracted from the HSPICE MC simulation, respectively. Fig. 2(a) shows the READ failure probability computed using Eq. (6) for 3 year NBTI stress with different $SNM_F$ values.

Equal signal probabilities of 0.5 are assumed for both $S_L$ and $S_R$. The results were obtained for three different conditions: a) does not consider the NBTI effect and only assumes RDF, b) applies a static NBTI shift while assuming RDF, and c) applies statistical NBTI variation combined with RDF (Eq. (5)). Comparison between condition b) and c) shows that the impact of NBTI variation can significantly increase the READ failure probability of an SRAM cell. Hence, there is a need to consider NBTI variation for temporal SNM analysis. The impact of NBTI variation also applies for different signal probabilities. Fig. 2(b) plots the 99% CDF point of SNM distribution for various signal probability pairs. As explained in [9], [10], SNM distribution shows the largest value when the signal probabilities at PL and PR are equal. Also, we can observe that the impact of NBTI variation can reduce the SNM values.

For further insight, the degradation of SNM (both the mean and the STD) shown in Fig. 2(a) can be modeled in an empirical form. In [9], it was shown that the degradation in mean SNM closely follows the power law with fixed exponent of 1/6. Following a similar analysis, we can derive a compact form for the STD of SNM under NBTI variation. First, SNM can be written in a canonical form as follows,

$$SNM(t) = SNM_0 + \sum_{i \in NM} n_i V_{tn,i} + \sum_{i \in PM} p_i V_{tp,i}(t, S_{p,i})$$  

(7)

where $SNM_0$ represents the nominal SNM value at time 0. $n_i$ and $p_i$’s are the independent linear sensitivity coefficients of $SNM$ with respect to $V_{tn}$’s of different NMOS and PMOS transistors, respectively. $NM$ and $PM$ represent the set of NMOS and PMOS transistors in a cell, respectively. $V_{tn}$ and $V_{tp}$’s are the random variables representing the deviation of NMOS and PMOS transistor $V_{tn}$’s from its nominal values, respectively. Note that PMOS $V_{tp}$’s have a time and signal probability dependency given by Eq. (1), which also incorporates both RDF and NBTI variation effects as shown in Eq. (5) (i.e., while $V_{tn}$ only has the RDF component). From Eq. (7), STD of time dependent $SNM$ can be computed as,

$$\sigma_{SNM}(t) = \sqrt{\sum_{i \in NM} n_i^2 \sigma_{V_{tn,i}}^2 + \sum_{i \in PM} p_i^2 \sigma_{V_{tp,i}}^2(t, S_{p,i})}$$  

(8)

where $\sigma_{V_{tn}}$ and $\sigma_{V_{tp}}$ represent the STD of NMOS and PMOS (Eq. (5)), respectively. Using Eqs. (1), (5), and (8), one can derive the
relative change in SNM STD (\(R_{SNM}(t)\)) with time as follows,
\[
R_{SNM}(t) = \frac{\sigma_{SNM}^2(t) - \sigma_{SNM}^2(0)}{\sigma_{SNM}^2(0)} = K_{SNM} \times \sqrt{\left(p_{AC}^2 \mu_{AC}(S_{P+}) + p_{RC}^2 \mu_{AC}(S_{P-})\right) \times t^{1/2}}
\]
where we can clearly observe that the relative change in SNM STD also follows a power law model with a fixed time exponent of 1/2.

Note here that for relative change standard (\(R_{SNM}\)), we applied a squared deviation (square root of relative change in variance) from its nominal value. Power law behavior of performance parameters are of importance when one tries to characterize its behavior from early post-silicon measurements. For example, in [19], authors proposed a SRAM SNM characterization method based on an \(I_{DDQ}\) measurement, where they have utilized the fact that mean SNM decreases in a power law under NBTI degradation [9]. Fig. 2(c) shows the comparison of our model and the HSPICE simulation results. It can be observed that both \(\mu\) and \(\sigma\) of the SNM can be predicted using our model. Combined with Eq. (6), one can also estimate the READ failure probability for a given time period.

2) WRITE stability: In contrast to the READ operation, WRITE function of an SRAM cell usually benefits from the NBTI degradation. Due to NBTI, PMOS pull-up transistor PL (Fig. 1(c)) becomes weaker compared to the access transistor AXL, leading to a faster WRITE operation. However, with the impact of NBTI variation, distribution of WRITE can change with time. Fig. 3(a) shows the temporal change of mean and the STD of WRITE access time under NBTI. In our work, WRITE access time is defined as a delay from the 50% rising time at the word line to the 50% falling time at the data node storing 1 (i.e., \(V_L\) in Fig. 1). The results were obtained using a Monte-Carlo based HSPICE simulation. Though the mean access time reduces with time, STD of access time increases due to the impact of temporal NBTI variation. Fig. 3(b) plots the signal probability dependence of WRITE access time under NBTI variation. Here, 3 year degradation under 125\(^\circ\)C is assumed. The mean trend in WRITE access time shows that WRITE performance degrades under unbalanced signal probability. However, the relative variation of access time is minimized when signal probabilities are more unbalanced.

Similar to the analysis applied to the temporal SNM variation in the last section, access time of SRAM cell can be also modeled in a fractional power law model. Following the same analysis introduced in Eqs. (7)~(9), relative change in mean and the STD of WRITE access time can be modeled as shown in Fig. 3(c). Mean and the STD of WRITE access time were modeled as a power law model and compared with the HSPICE simulation result. As can be observed, time exponent of the mean and the STD are 1/6 and 1/12, respectively.

### B. Delay degradation and leakage reduction in random logic

In random logic circuits, the impact of NBTI degradation is most evident in the increase of delays of critical timing paths [6] and reduction of subthreshold leakage current [19]. In this section, we will show how the NBTI variation impacts the circuit delay and circuit leakage variations.

Fig. 4(a) represents the histogram of a simple inverter gate delay with/without the impact of NBTI variation assuming 3 year stress. MC based HSPICE simulation was applied to obtain the result using 32nm PTM file. Since PMOS’s are mainly affected by NBTI, rising delay of the gate was measured. As can be observed from the two curves on the right, with an added impact of NBTI, the variability of gate delay can increase significantly. For this specific example, 99% CDF point of the rising delay has been pushed out by 5.8%.

Table 1 summarizes the simulation result showing the impact of NBTI variations in different circuits designed at 22nm and 32nm technology nodes. \(\mu_{init}\) and \(\mu_{life}\) are the mean delay at time 0 and after 3 year NBTI stress at 125\(^\circ\)C, respectively. \(\sigma_{RDF}\) and \(\sigma_{NBTI}\) are the STD of the delay considering only RDF and both RDF and statistical NBTI variation at the same time, respectively. As can be observed in the 7th column, the STD of delay can change significantly due to the impact of NBTI variation. The result shown in the 8th column is the overall delay increase in 99% CDF point after 3 year stress considering the NBTI variation. Compared to the standard gate level results, circuit level results (e.g., invch5 and invch9) only show minimal change in delay variation. This is due to the variation canceling effect between different gates in the same timing path, and becomes more significant in circuits with large logic depth. Comparison between 32nm and 22nm node shows that the impact of NBTI variations will grow larger in scaled technology as predicted from Fig. 1(b).

It is important to note that in reality, the variation of circuit delays are mostly dominated by lower granularity sources such as inter-die variations [17]. And as a result, random \(V_T\) variation induced by NBTI degradation will usually take only a small portion of the overall delay variations.

Similar effects can be observed in the subthreshold leakage variation under NBTI degradation. Fig. 4(b) represents the histogram plot of inverter leakage. Since PMOS’s are mainly affected by NBTI, leakage at logic HIGH input was measured. As can be observed, due to the NBTI, leakage current reduces. However, the two curves on the left side show that the increased variability of \(V_T\) due to NBTI can lead to a more variation in leakage. Table 2 summarizes the leakage distribution results for various simple gates and inverter chains (invch). As predicted, statistical variation of NBTI generates increased level of leakage variation with time.
IV. SUMMARY & CONCLUSION

In very short channel devices, finite number of Si-H bonds in the Si-SiO₂ interface can result in a statistical variation in NBTI degradation process in different devices. In this paper, we proposed and modeled the impact of statistical NBTI variation on lifetime circuit performance. First, we derived a compact $V_t$ model for circuit level simulation. The model describes the increase in the STD of $V_t$ ($\sigma_{V_t}$) as a fractional power law with a fixed exponent of 1/12. Using this model, we explored the impact of NBTI variation in the READ and WRITE stability of SRAM cells and delay variation in random logic circuits. We have shown that the NBTI-induced $V_t$ variation, on top of static degradation shift can result in a significant reduction of circuit reliability with time.

V. ACKNOWLEDGEMENTS

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REFERENCES


![Graph showing variation in WRITE access time under temporal NBTI variation](image)

**Fig. 3.** (a) Variation in WRITE access time under temporal NBTI variation, (b) variation in WRITE access time for various $S_p$ under 3 years NBTI stress, and (c) Temporal WRITE access time modeling. $\mu$ and $\sigma$ of WRITE access time has time exponent of 1/6 and 1/12.

**TABLE II**

| Circuit | In # | RISING DELAY DEGRADATION DUE TO NBTI VARIATIONS.
INVCH is a nominal size inverter chain. |
<table>
<thead>
<tr>
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<tr>
<td>32nm (GHz)</td>
<td>22nm (GHz)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RISING DELAY (ps)</td>
<td>$\Delta$(%)</td>
</tr>
<tr>
<td></td>
<td>$\mu_{\text{init}}$</td>
<td>$\mu_{\text{life}}$</td>
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