Impact of NBTI on the Temporal Performance Degradation of Digital Circuits

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Abstract—Negative bias temperature instability (NBTI) has become one of the major causes for reliability degradation of nanoscale circuits. In this letter, we propose a simple analytical model to predict the delay degradation of a wide class of digital logic gate based on both worst case and activity dependent threshold voltage change under NBTI. We show that by knowing the threshold voltage degradation of a single transistor due to NBTI, one can predict the performance degradation of a circuit with a reasonable degree of accuracy. We find that digital circuits are much less sensitive (approximately 9.2% performance degradation in ten years for 70 nm technology) to NBTI degradation than previously anticipated.

Index Terms—Negative bias temperature instability (NBTI), performance degradation, threshold voltage degradation.

I. INTRODUCTION

With the continuous scaling of transistor dimensions, the reliability degradation of circuits has become an important issue. Due to an increasing electric field across the thin oxide, the generation of interface traps under negative bias temperature instability (NBTI) in pMOS transistors has become one of the most critical reliability issues that determine the lifetime of CMOS devices [1], [2]. Due to NBTI, the threshold voltage (Vth) of the transistor increases with time resulting in the reduction in drive current [3], which in turn results in temporal performance degradation of circuits. Reliability verification is therefore necessary in the early design phase to ensure the functionality of circuits for a desired period of time. A good model for estimating the performance degradation due to NBTI, hence, is urgently needed. While several efficient models have been proposed to estimate Vth degradation [4], [5], only a few qualitative discussions are available in the literature on the drive current and delay degradation due to NBTI [6]–[8].

In this letter, for the first time, we propose an analytical model to predict the performance degradation of large digital circuits based on Vth degradation of a pMOS transistor due to NBTI. We show that the degradation in Vth and the corresponding circuit delay have the same power-law dependency on time. We also find that the percentage degradation in circuit performance is much lower than that of Vth.

We use this model to calculate the performance degradation of several ISCAS benchmark circuits, which represent a wide range of digital circuits. Results show that using the proposed model, the performance degradation of a circuit due to NBTI can be predicted with a reasonably high degree of accuracy.

II. THEORETICAL ANALYSIS

A. Vth Degradation Model

NBTI is the result of trap generation at Si/SiO2 interface in negatively biased pMOS transistors at elevated temperatures. The interaction of inversion layer holes with hydrogen-passivated Si atoms can break the Si–H bonds, creating an interface trap and one H atom that can diffuse away from the interface (through the oxide) or can anneal an existing trap. The interface trap generation is modeled successfully in the Reaction–Diffusion framework [4]. In this model, interface trap density (ΔNT) is expressed as

\[ \Delta N_{IT}(t) = \sqrt{\frac{k_f N_0}{k_r}} (D_{IT} t)^{0.25} \]  

(1)

where \( k_f \) and \( k_r \) are the bond-breaking and hydrogen annealing rates, respectively, \( N_0 \) is the maximum available Si– density and \( D_{IT} \) is the diffusion coefficient. The bond-breaking rate depends on the accumulation of holes in the inversion layer and the tunneling of the holes into the oxide to dissociate the Si– bonds [10]. Thus, \( k_f \) depends on the hole density \( p \), hole capture cross-section \( \sigma_0 \), tunneling coefficient \( T_p \), and the bond dissociation coefficient \( B \), and can be expressed as \( k_f \propto B \sigma_0 T_p \), where \( p = C_{ox}(V_g - V_{th}) \propto E_{ox} \) and \( T_p \propto e^{(E_{ox}/E_0)} \) depend on the electric field \( E_{ox} \) across the oxide, \( E_0 \) is the field acceleration factor, \( B \), \( \sigma_0 \), and \( k_r \) are assumed to have weak field dependence [10]. Substituting \( k_f \), (1) can be simplified to

\[ \Delta N_{IT}(E_{ox}, t) = \sqrt{E_{ox}} \left( \frac{E_{ox}}{E_0} \right)^{0.25} \]  

(2)

where \( \chi \) represents the field independent terms. Furthermore, the interface traps increase scattering resulting in mobility degradation. The mobility degradation can be expressed as an additional \( V_{th} \) shift [8]. The effective threshold voltage degradation can be expressed as

\[ \Delta V_{th}(E_{ox}, t) = (1 + m) \frac{q \Delta N_{IT}(E_{ox}, t)}{C_{ox}} \]  

(3)

where \( m \) accounts for for excess \( V_{th} \) shift due to mobility degradation.
is a constant. The delay of a gate can be approximately
degradation. Therefore, by monitoring the
is the load capacitance and
will linearly change with
is close to
, (6)
is the supply voltage.

\[ \frac{\Delta V_{th}}{V_{th}} = (1 + n) \log \frac{E_{ox} e^{\frac{qV_{th}}{kT}}}{C_{ox}}. \]  

B. Gate Delay Degradation Model

The drain current of a transistor in the saturation region can be approximately represented as

\[ I_d = \beta (V_g - V_{th})^\alpha, \quad \beta = \frac{\mu C_{ox} W_{eff}}{L_{eff}} \]  

(4)

where \( \alpha \) is a constant. The delay of a gate can be approximately expressed as [7] and [8]

\[ \tau = \frac{C_L V_{dk}}{I_d} = \frac{K_1}{(V_g - V_{th})^\alpha} \]  

(5)

where \( C_L \) is the load capacitance and \( V_{dk} \) is the supply voltage. Differentiating (5) with respect to \( V_{th} \), we get

\[ \frac{\Delta \tau}{\tau} = \frac{\alpha \Delta V_{th}}{(V_g - V_{th})^\alpha}. \]  

(6)

Substituting \( \Delta V_{th} \) from (3) in the form of \( Al^n (n = 0.25) \), (6) can be rewritten as

\[ \log \left( \frac{\Delta \tau}{\tau} \right) = n \cdot \log(t) + \log \left( \frac{\alpha A}{V_g - V_{th}} \right) \]

\[ A = (1 + n) q \sqrt{E_{ox} e^{\frac{qV_{th}}{kT}}}. \]  

(7)

The second term in the right-hand side of (7) is not constant because \( V_{th} \) is a function of time. However, due to the logarithmic dependency, this term can be treated as constant for a specific range of time [e.g., ten years, see Fig. 1(a)]. In this period, \( \log(\Delta \tau/\tau) \) will linearly change with \( \log(t) \) with the same slope \( n \) as the \( V_{th} \) degradation. Therefore, by monitoring the threshold voltage degradation, the change in gate delay can be easily estimated with a high degree of accuracy.

Fig. 1(b) shows the degradation of threshold voltage and the corresponding gate (inverter) delay with time. The threshold voltage degradation was obtained using (3). The inverter delay was measured through HSPICE simulation using 70-nm BPTM technology\(^1\) \((V_{dk} = 1 \text{ V})\) [9]. It can be observed that both the threshold voltage and the gate delay degradation have the same slope \((0.25)\) as expected from (7).

It can also be observed from Fig. 1(b) that the degradation in delay is less than the degradation in threshold voltage. This can be understood from (6). Since \( V_g - V_{th} \) is greater than \( V_{th} \) [within the time range shown in Fig. 1(b)] and \( \alpha \) is close to one for short channel transistors, the percentage degradation in delay will be less than that of the threshold voltage and can be quantified as \( \log[\alpha/(V_g - V_{th})] \).

\(^1\)In SPICE simulation we added an appropriate battery to the pMOS gate to replicate the effect of \( V_{th} \) change.
C. Circuit Delay Degradation

The performance degradation of any circuit (considering the activities of individual transistors) can be estimated as follows. The delay of a circuit ($\tau_{ckt}$) is the accumulation of all individual gate delays ($\tau_{g,i}$) in the critical path, which can be expressed as $\tau_{ckt} = \sum_{i=1}^{N} \tau_{g,i}$, where $N$ is the number of gates in the critical path. Using (7), the performance degradation of a circuit can be expressed as

$$\log \left( \frac{\Delta \tau_{ckt}}{\tau_{ckt}} \right) = \log \left[ \sum_{i=1}^{N} \frac{(S_i \cdot t)^n \alpha A_{g,i}}{V_{th}} \right]$$

$$= n \log(t) + \log \left( \sum_{i=1}^{N} \frac{\alpha A_{g,i}(S_i \cdot t)^n \tau_{g,i}}{V_{th}} \right)$$

$$= n \log(t) + \log \left( \sum_{i=1}^{N} \frac{\alpha A_{g,i}(S_i \cdot t)^n \tau_{g,i}}{V_{th}} \right)$$

$$\tau_{g,i} = 0)$$

where $S_i \cdot t$ represents the on-time of a pMOSFET in gate $i$, based on its switching activity. Note that $S_i$ is typically calculated over a period of time and shows negligible change. Hence, the slope ($n$) of $\log(\Delta \tau_{ckt}/\tau_{ckt})$ versus $\log(t)$ will not change.²

The performance degradation of a nine-stage ring oscillator, as expected, shows [Fig. 1(b)] the same slope as $\Delta V_{th}$ (also observed experimentally [11]). Further, the percentage degradation is half of that of a single gate because in digital circuits a low-to-high (l-h) switching is always followed by a high-to-low (h-l) switching. While a l-h switching is affected due to NBTI, the h-l switching is not affected.

III. SIMULATION RESULTS

We simulated several ISCAS benchmark circuits to estimate their performance degradation due to NBTI. We considered the following two cases: 1) $\Delta V_{th}$ of all pMOS transistors are the same (worst case condition) and 2) $\Delta V_{th}$ of all individual pMOS transistors are different depending on their on-time ($V_{gs} = -V_{th}$). The on-time is calculated based on the switching activity of each individual gate assuming 50% signal switching probability at primary inputs. Circuit delays are calculated through static timing analysis [12].

The performance degradation of an ISCAS C432 circuit, as expected, shows [Fig. 2(a)] the same time exponent as $\Delta V_{th}$ for both case 1 and 2. Furthermore, despite a wide variation in $\Delta V_{th}$ [Fig. 2(b)], the performance degradation is almost comparable to the worst case degradation [Fig. 2(a)]. Hence, estimating performance degradation with a worst case assumption will not result in a significant over estimation. Table I shows the percentage delay degradation of several ISCAS benchmark circuits with time under both worst case ($S_i = 1$) and activity dependent ($S_i < 1$) NBTI stress. The expected average delay degradation is about 9.2% (worst case) in ten years, approximately four times less than $V_{th}$ degradation.

IV. CONCLUSION

In this letter, we proposed a simple analytical model to estimate the temporal delay degradation of digital circuits due to NBTI. Since the performance degradation has the same time exponent as $V_{th}$, the conventional burn-in tests will be effective to predict the degradation due to NBTI and we do not need to test individual transistors. Hence, this analysis will significantly help in designing reliable digital circuits.

REFERENCES


²In this letter, NBTI recovery due to ac operation is not included. However, this can be included by modifying $k_f$ in (1) by a constant factor, which makes a linear shift in percentage $V_{th}$ degradation [4] and will not change the time exponent.

²Sequential circuits will also have the similar effect due to NBTI as combinational logic and can be similarly predicted.