A Geometrical Unification of the Theories of NBTI and HCI Time-Exponents And Its Implications for Ultra-Scaled Planar and Surround-Gate MOSFETs

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Abstract
A unification of time-exponents for Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI) is established under the geometric interpretation of interface trap generation. Resolving the fundamental inconsistencies, a numerical reaction-diffusion (R-D) model that agrees with recent measurements is developed. The implications regarding the degradations of future sub-100 nm planar and surround-gate MOSFETs are presented.

Introduction
Although the two fundamental degradation modes for MOSFETs - NBTI and HCI at peak I	extsubscript{E}	extsubscript{Ub} condition - differ in many respects, they both involve breaking of Si-H bonds at the Si-oxide interface followed by H	extsubscript{2} diffusion into the oxide. Therefore, it is not surprising that the time-exponents of interface trap density (N	extsubscript{IT}) of both these phenomena (e.g., NBTI - t\textsuperscript{nB} and HCI - t\textsuperscript{nH}, in Fig. 1) have always been described by the same reaction-diffusion (R-D) model [1,2]. In this paper, however, we show that the 30-year-old classic analysis of HCI and NBTI time exponents by R-D model is flawed and cannot be sustained in view of recent experiments [3]. We reconcile this inconsistency by re-evaluating the geometry dependence of the R-D model for NBTI and HCI degradation.

Background
The classical R-D model [2] predicts five interface trap (N	extsubscript{IT}) generation regimes (- f, n=1, 0, ¼, ½, 0 in Fig. 2) [4]:

\[ \frac{dN_{IT}}{dt} = k_f [N_0 - N_{IT}] \frac{N_{IT}}{N_{IT}^{0.5}} \]

\[ \frac{dN_{IT}}{dt} = D_{H} \frac{d^2 N_{IT}}{dy^2} \]

Fig. 2. Classical R-D model results in five regions whose time behaviors are governed by the equations in the inset. D	extsubscript{H} is the diffusion constant and k	extsubscript{f} and k	extsubscript{r} are forward dissociation rate and reverse annealing rate of Si-H bonds, respectively.

Fig. 3. Finite diffusion velocity in the gate yields a time-exponent less than ½ (i.e., n < ½). This conflicts the assumption of the infinite diffusion velocity in the poly-silicon gate. Data from [3] with T=125°C, T=2.6 nm, E=9.1 MV/cm.

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This negates the fundamental presumption (i.e., instantaneous hydrogen diffusion in poly) invoked to interpret the HCI data as represented in Fig. 1b. Moreover, the $n^{th}$ to $n^{th}$ transition has never been observed in HCI measurements.

It is natural to ask, therefore, if this failure to interpret the HCI exponents signals a fundamental inadequacy of the R-D model in describing $N_{IT}$ generation — thereby invalidating the broad range of modeling work for NBTI based on the R-D model [2,6].

**Analytical Results**

The resolution of the above discrepancy lies in the obvious fact that NBTI is a 1-D problem and HCI is a 2-D phenomenon; the interface trap distribution is uniform over the channel in NBTI whereas in HCI, traps are generated near the drain only as in Fig. 4, therefore the R-D model must reflect this geometry dependence, something the classic analysis does not do. Since breaking of a Si-H bond creates one H atom per trap, at any time $t$, $N_{IT}(t)=1/A_{dr}N_{IT}(r,t)dr$ ($A_{dr}$ area of degraded interface region), and since the diffusion front in the oxide moves as $(D_{it})^{1/2}$, therefore,

$$N_{IT}^{(NBTI)}(t) = \sqrt{\frac{\pi}{2A_{dr}}} \int_0^t \frac{N_{IT}(r,t)dr}{(D_{it})^{1/2}}$$

$$= \sqrt{\frac{\pi}{2A_{dr}}} \int_0^t \left[ 1 - \frac{r}{\sqrt{D_{it}}} \right] A_{dr}dr$$

$$= \left( \frac{1}{2} \right) \sqrt{\frac{\pi}{2A_{dr}}} \int_0^t \left[ 1 - \frac{r}{\sqrt{D_{it}}} \right] A_{dr}dr$$

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Assuming, $dN_{IT}/dt \sim 0$ compared to the bond breaking and the annealing terms (inset, Fig. 2), $N_{IT}N_{IT}^{(0)} \sim constant$.

So,

$$N_{IT}^{(NBTI)}(t) \sim \sqrt{\frac{k_{IT}^{(NBTI)}N_{IT}^{(0)}}{k_{IT}}} \cdot (D_{it})^{1/2}$$

and

$$N_{IT}^{(HCI)}(t) \sim \sqrt{\frac{k_{IT}^{(HCI)}N_{IT}^{(0)}}{k_{IT}}} \cdot (D_{it})^{1/2}$$

Unlike the classical analysis, the exponent $n=\frac{1}{2}$ arises naturally as a consequence of 2-D hydrogen diffusion during HCI degradation. Moreover, $n=\frac{1}{2}$ exponent is no longer expected for HCI and the model no longer requires that the diffusion velocity in poly be infinite, thereby removing two basic objections against the R-D model for HCI data.

**Numerical/Experimental Verification**

Fig. 5 illustrates the results of the numerical solutions for 1-D and 2-D geometries of NBTI and HCI degradation, respectively. The time-exponents predicted by our geometry-dependent R-D model for DC HCI stress are reasonably consistent with experimental data as shown in Fig. 6.

![Fig. 5. Replot of Fig. 2 when the geometry dependence of the R-D model is accounted for. Note that while the NBTI degradation regimes remain unchanged, the HCI degradation shows only $n=\frac{1}{2}$ regime — indicating fundamental modification in interface trap generation rates due to geometrical effects.](image)

For AC stress, the traps generated during the ON state by dissociation of Si-H bonds are annealed by $H_2$ in the oxide during the OFF state, with corresponding decrease in $N_{IT}$. Our model can successfully predict the NBTI relaxation by 1-D simulation in Fig. 7b. Likewise, as shown in Fig. 7a, the 2-D R-D model can yield relaxation as well as post-stress generation during the OFF conditions in HCI [7,8].

![Fig. 6. HCI time exponents, $n$, reported in the literature [11-14] and the simulation exponents form our geometry-dependent R-D model. Simulation covers $n$ from 0.3 to 0.5 (hatched region).](image)
2. \( N \)

Fig. 1. Suess and passivation cycles during the ON and OFF states of AC bias. (a) The new model predicts insignificant relaxation for HCI degradation (Fig. 8 for explanation). HCI post-stress trap generation reported in the literature can also be simulated. (b) NBTI relaxation agrees well with measurements \[9,15\] with \( T=100^\circ C, T_{oa}=1.3nm, V_D(ON)=-2.7V, V_T(OFF)=0V \). During OFF state, \( k_T = 0 \) for HCI relaxation, and \( k_T = k_Te^{+t} \) for post-stress with \( t \) being the average trapped-hole release time.

The model for post-stress \( N_{IT} \) generation assumes that holes are captured by the oxide traps during the ON phase. During the OFF phase, these holes are gradually released from the hole traps, and a fraction of them can interact with the Si-H bonds at the interface. This interaction eventually leads to breaking of Si-H bonds and generation of interface traps.

Finally, Fig. 8 explains why HCI relaxation is always less than NBTI relaxation: the reaction surface for annealing in HCI is reduced significantly due to the localized degradation near the drain end.

Implications

Given this consistency with existing experiments, consider the implications of the geometrical R-D model for several scaling scenarios. First, if the HCI degraded region \( (AL) \) remains relatively independent of channel length, \( L_C \) (assuming similar lateral electrical field), our model predicts that the HCI exponent will be independent of \( L_C \) scaling as in Fig. 9: the \( H_2 \) released from the drain side can not probe the source boundary within the measurement window, therefore cannot be affected by it. Second, Fig. 10 shows that if \( AL \) increases with drain voltage (for peak \( I_{on} \) condition) for a given \( L_C \) at a particular technology node, there will be gradual decrease in the HCI exponents, with important implications for lifetime projection at operating conditions based on data taken at higher voltages. Third, continuing further down the Moore's curve, Fig. 12 compares trap generation and the time-exponents for the cylindrical gate MOSFET structure of Fig. 11 with several radii. The curvature of the oxide-semiconductor interface effectively increases the diffusion rate while slowing down the annealing as the inner radius of the oxide is reduced. A similar scaling effect is expected for transistors with rectangular channel cross sections such as the triple-gate MOSFET shown in Fig. 13. Shrinking the

Fig. 7. Stress and passivation cycles during the ON and OFF states of AC bias. (a) The new model predicts insignificant relaxation for HCI degradation (Fig. 8 for explanation). HCI post-stress trap generation reported in the literature can also be simulated. (b) NBTI relaxation agrees well with measurements \[9,15\] with \( T=100^\circ C, T_{oa}=1.3nm, V_D(ON)=-2.7V, V_T(OFF)=0V \). During OFF state, \( k_T = 0 \) for HCI relaxation, and \( k_T = k_Te^{+t} \) for post-stress with \( t \) being the average trapped-hole release time.

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![Fig. 8. Hydrogen profile in the oxide during relaxation of HCI damage (see Fig. 4b). A pocket is formed near the drain end due to the annealing of the interface traps. The grayscale on the right shows the density of \( H_2 \) (cm\(^{-3}\)).](image)

![Fig. 9. R-D model predicts that the time exponent of HCI degradation is independent of the channel length, \( L_C \) provided the degradation area, \( AL \), remains constant.](image)

![Fig. 10. Time exponents decrease as the damaged region, \( AL \), occupies greater fraction of the channel length. This implies that the time-exponents at lower voltages may be larger than those at higher voltages, invalidating the traditional assumption that \( n \) is independent of the stress voltage.](image)

5.3.3 IEDM 04-115
width, $W$, increases the NBTI damage in Fig. 14b; scaling the transistor shifts the hydrogen diffusion from 1-D to 2-D, which in turn increases the trap generation. Purely based on geometrical considerations, our model implies worsened NBTI degradation for surround-gate devices like VRG, FINFET, and Si-nanowire transistors.

![Schematic of the cylindrical gate oxide.](image)

**Fig. 11.** Schematic of the cylindrical gate oxide. A planar oxide can be imagined as $R_{inner} \to \infty$. Such geometries could be idealized representations of VRG, and Si-nanowire transistors.

![Graph showing NBTI time exponent for different $R_{inner}$.](image)

**Fig. 12.** For large radius, the NBTI time exponent shows typical n = 4 values. However, as the radius shrinks, the NBTI diffusion profiles for these devices begin to resemble the HCI-like 2-D characteristics (compare Fig. 11 with Fig. 4b) and the time-exponent increases rapidly. Therefore, higher NBTI degradation is expected for such surround-gate geometries.

![Schematics of the triple-gate MOSFET.](image)

**Fig. 13.** Schematics of the triple-gate MOSFET. Channel width and height of $W$ are assumed. The gate modules three surfaces. The channel direction determines the crystal orientation of the oxide/semiconductor interface planes which define the trap density $N_T$ (see Fig. 2) and thus the NBTI degradation. (a) $<100>$ channel direction with $W$ side surfaces, (b) $<110>$ channel direction with $W$ and $W$ sides. From [16].

![Graph showing NBTI time exponent for different $R_{inner}$.](image)

**Fig. 14.** $\Delta N_T$ of (a) $<100>$ and (b) $<110>$ channel directions with $W = 3.6$ nm (solid lines) and 30 nm (dotted lines). R-D modeling of thicker channels agrees well with experiments from [16]. Scaling of $W$ suggests larger degradation due to the geometric effect for the triple-gate MOSFET. In addition, (100) surfaces of Fig. 13a have less degradation than (110) of Fig. 13b, because the latter has higher trap density, $N_T$.

**Conclusions**

The geometry-aware R-D model provides a unified framework to interpret the HCI and NBTI time-exponents and firmly re-establishes the validity of R-D model to analyze interface trap generation. Our approach resolves several longstanding inconsistencies of the classical analysis and successfully explains the existing experimental data, provides realistic lifetime projections, and anticipates modified degradation rates for future generations of planar and surround-gate devices.

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**References**