# ECE 255, Frequency Response, Contd.

24 April 2018

## 1 Introduction

In this lecture, we will study the internal capacitances and their effects on the high-frequency response of a circuit. It is based on Section 10.2 to Section 10.5 of the textbook.

## 2 Internal Capacitive Effects of MOSFET

Any two pieces of conductive materials can make a capacitor. Hence, when two pieces of conductors are brought to close proximity of each other, due to that unlike charges attract, charges will accumulate on them. Then electric field is set up in between them, giving rise to electric energy stored. Electric energy stored corresponds to energy storage in a capacitor. These equivalent capacitors are called internal capacitors or parasitic capacitors. They are shown in Figure 1 and Figure 2.

These internal capacitors gives rise to the modification to the small-signal model. This modification is shown in Figure 3(a). Here, $C_{gs}$, $C_{gd}$, $C_{sb}$, and $C_{db}$ are the gate-to-source, gate-to-drain, source-to-body, and drain-to-body capacitances, respectively. But when the source terminal is connected directly to the body, $C_{sb}$ is shorted out, and then the model can be simplified as that shown in Figure 3(b). By further ignoring $C_{db}$ the drain-to-body capacitor, which is small since drain can be quite far from the body, the model simplifies to that show in Figure 3(c) and (d).

*Printed on April 25, 2018 at 19 : 51: W.C. Chew and S.K. Gupta.*

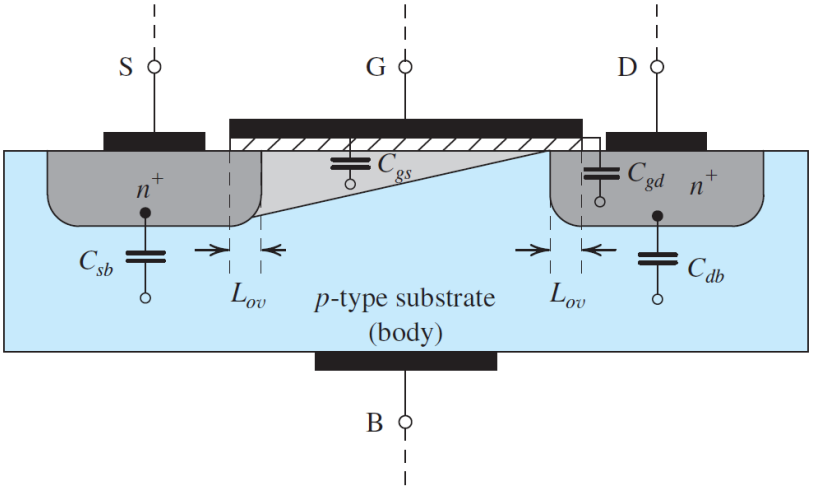



Figure 1: Internal capacitors in a MOSFET. Any two pieces of conductive materials separated by an insulator (or a region of low conductivity) will have a capacitance between them. This figure shows the internal capacitances as $C_{gs}$, $C_{gd}$, $C_{sb}$, and $C_{db}$ (Courtesy of Sedra and Smith).

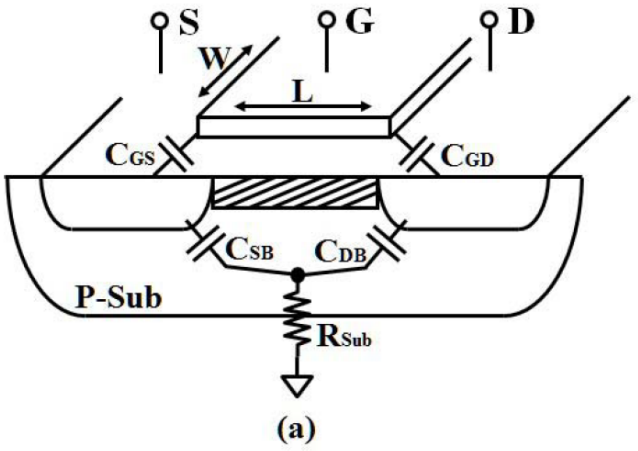



Figure 2: Internal capacitors of a MOSFET (Courtesy of Zhang, Najafi, Taghivand, Rudel, MTT 2017).

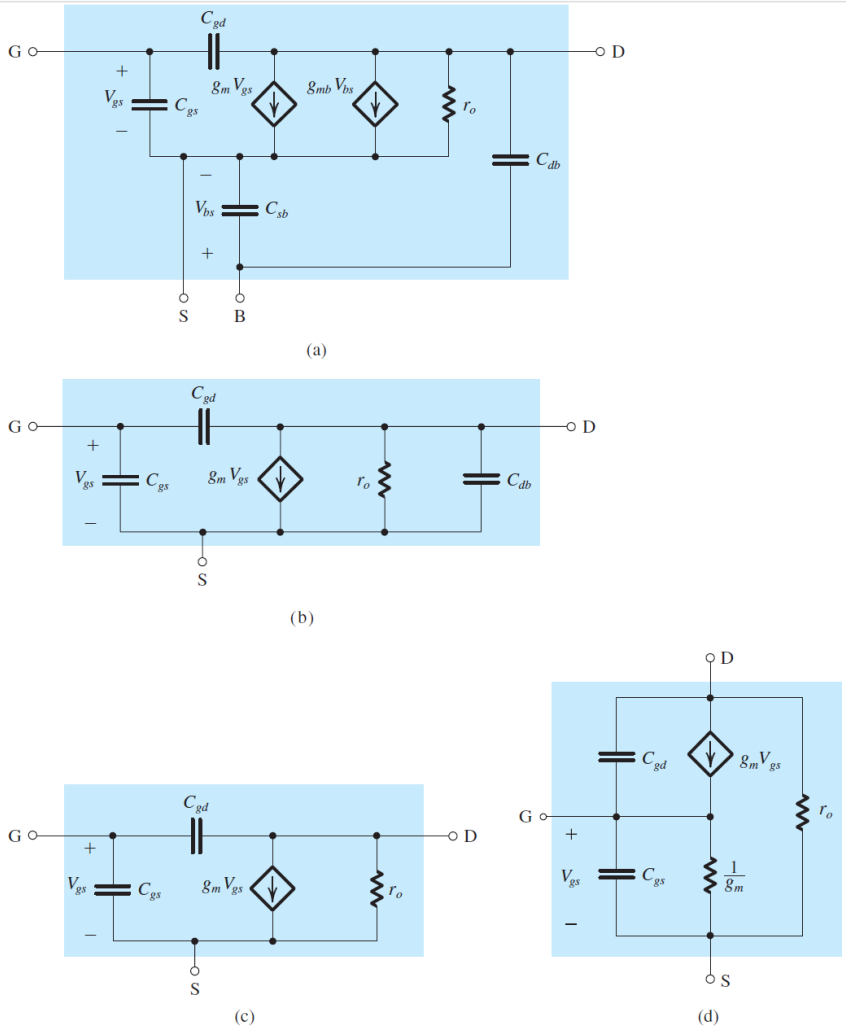



Figure 3: (a) High-frequency equivalent circuit of a MOSFET. (b) The simplified case where the source terminal is connected to the body. (c) Further simplification by ignoring $C_{db}$, which is usually small. (d) The simplified T model equivalent circuit (Courtesy of Sedra and Smith).

## 2.1 The MOSFET Unity-Gain Frequency $f_T$

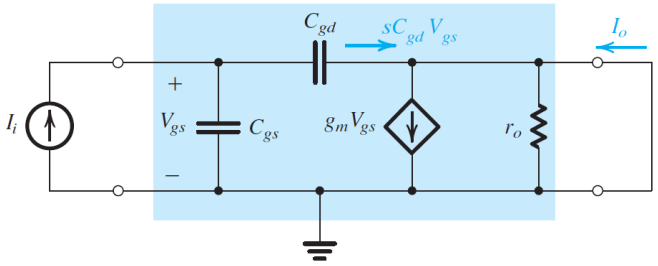



Figure 4: Model for determining the short-circuit current gain (Courtesy of Sedra and Smith).

The presence of the internal capacitances degrades the performances of the amplifier at high frequencies. As the frequency increases, these capacitances become short circuits, and the gain of the amplifier drops and its performance deteriorates. The amplifier becomes useless again when its gain drops below one. Therefore, it is prudent to ascertain the frequency at which the short-circuit current gain becomes one. This frequency is usually denoted as $f_T$, or called the **transition frequency**. Beyond this frequency, the transistor is rendered useless due to the shorting behavior of these internal capacitances.

To determine the short-circuit current gain using the model shown in Figure 4, one injects a current $I_i$ into the input port of the amplifier. Then the output current $I_o$, ignoring the current through $r_o$, is[1]

$$I_o = g_m V_{gs} - sC_{gd}V_{gs} \tag{2.1}$$

Since the capacitance $C_{gd}$ is small, because the distance between the gate and the drain is large, one can approximate this current as just

$$I_o \approx g_m V_{gs} \tag{2.2}$$

Furthermore, since the output is shorted, both $C_{gs}$ and $C_{gd}$ have their other terminals connected to ground, and hence, they are connected in parallel with respect to the input current $I_i$. Thus one finds $V_{gs}$ as

$$V_{gs} = \frac{I_i}{s\,(C_{gs} + C_{gd})} \tag{2.3}$$

Consequently, multiplying (2.3) by $g_m$ to obtain $I_o$ from (2.2), one gets

$$\frac{I_o}{I_i} = \frac{g_m}{s\,(C_{gs} + C_{gd})} \tag{2.4}$$

[1]Using KCL which is valid for complex impedances as well.

By letting $s = j\omega$, one has

$$\left|\frac{I_o}{I_i}\right| = \frac{g_m}{\omega\left(C_{gs} + C_{gd}\right)} \tag{2.5}$$

The above formula reflects the effect of these internal capacitances: the current gain drops as the frequency increases as expected.

The above becomes unity at

$$\omega = \omega_T = g_m / \left(C_{gs} + C_{gd}\right) \tag{2.6}$$

Using $f_T = \omega_T / 2\pi$ yields

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gd}\right)} \tag{2.7}$$

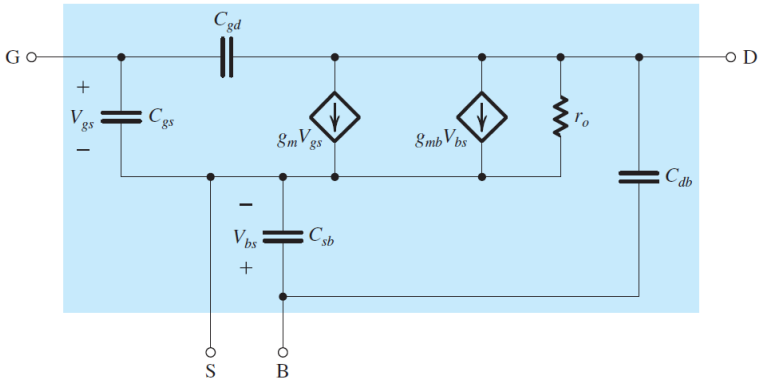
It is seen that the smaller the internal capacitances, the larger is $f_T$. Typically, $f_T$ ranges from 100 MHz for older technologies (5-$\mu$m CMOS) to many GHz for newer high-speed technologies (0.13-$\mu$m CMOS).[2]

The smaller the device, the smaller are the internal capacitances, since capacitance is simply given by the formula $\epsilon A/d$. Making a device 10 times smaller makes the area 100 times smaller, while the separation becomes 10 times smaller. Hence, the capacitance becomes ten times smaller.

[2]Now it is possible to make transistors operating at 100 GHz.

**Table 10.1** The MOSFET High-Frequency Model

**Model**




**Model Parameters**

$$g_m = \mu_n C_{ox} \frac{W}{L} |V_{OV}| = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{|V_{OV}|}$$

$$C_{sb} = \frac{C_{sb0}}{\sqrt{1 + \frac{|V_{SB}|}{V_0}}}$$

$$g_{mb} = \chi g_m, \quad \chi = 0.1 \text{ to } 0.2$$

$$r_o = |V_A| / I_D$$

$$C_{db} = \frac{C_{db0}}{\sqrt{1 + \frac{|V_{DB}|}{V_0}}}$$

$$C_{gs} = \frac{2}{3} WLC_{ox} + WL_{ov} C_{ox}$$

$$C_{gd} = WL_{ov} C_{ox}$$

$$f_T = \frac{g_m}{2\pi (C_{gs} + C_{gd})}$$

# 3 Internal Capacitive Effects of BJT

As before, the simple hybrid-$\pi$ model of the BJT has to be modified accordingly due to the presence of internal or parasitic capacitances.

## 3.1 The High-Frequency Models for BJT

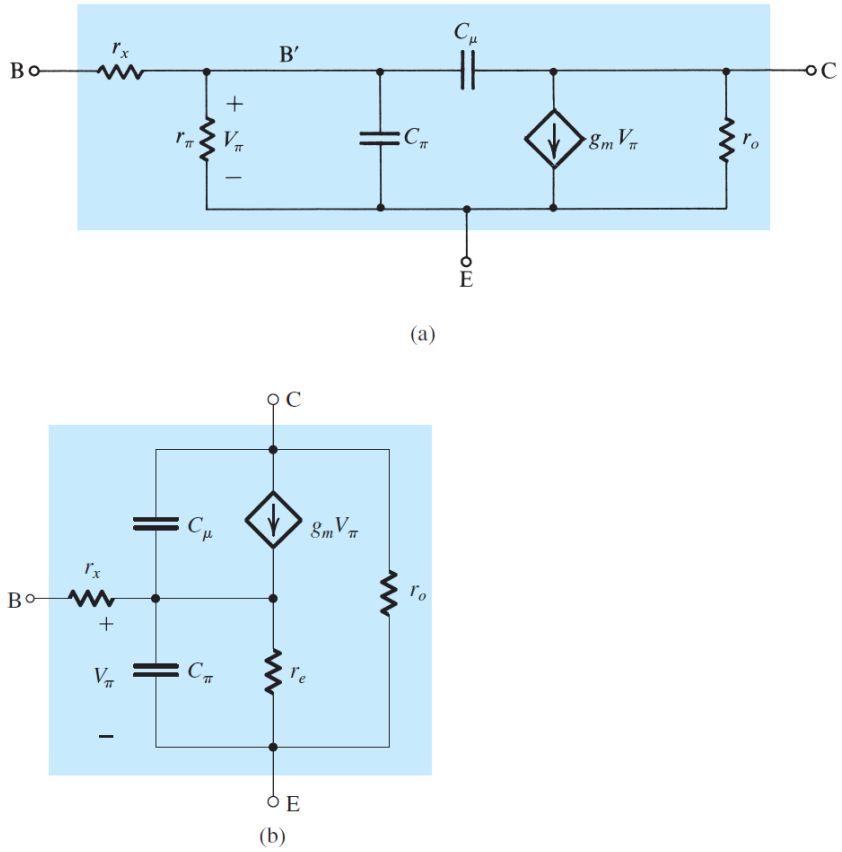



Figure 5: The high-frequency model for BJT both in hybrid-$\pi$ model in (a), and the T model in (b) (Courtesy of Sedra and Smith).

Because of the internal capacitances of the BJT, the high-frequency model is shown in Figure 5 where $C_\pi = C_{de} + C_{je}$, and $C_\mu$ is the parasitic capacitance between the base and the collector. Here, $C_\pi$ is a few to a few tens of picofarads, while $C_\mu$ is a fraction to a few picofarads. In general, $C_\mu \ll C_\pi$. They get increasingly smaller with progress in technology. A resistor $r_x$ is used here to model an intrinsic silicon material resistance. The reasons for the existence of these internal capacitances will be discussed next.

## 3.2 The Base-Charging or Diffusion Capacitance $C_{de}$

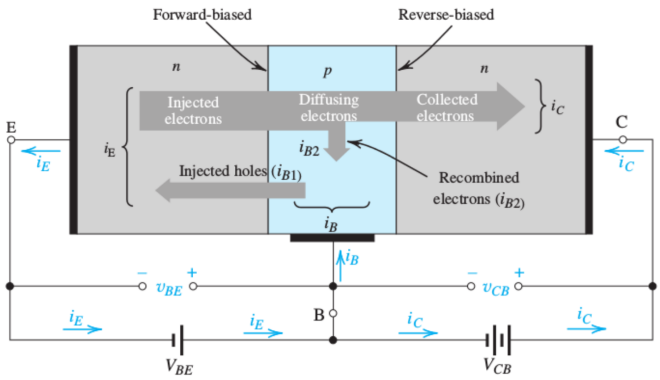



Figure 6: Revisit of the BJT model for current flow (Courtesy of Sedra and Smith).

Parasitic capacitances slow down the switching speed of a transistor, since they have to be charged and discharged. The slowness of these charge and discharge processes makes the capacitor look like a short circuit at high frequency.

It will be prudent to study various charge storage mechanisms in a transistor. For an *npn* transistor, shown again from previous lectures in Figure 6, as the current diffuses across the base region, the charge stored in the base region can be expressed as

$$Q_n = \tau_F i_C \tag{3.1}$$

where $\tau_F$ is the **forward base-transit time**, the average time a charge carrier (electron) takes in diffusing across the base. It is typically about 10 ps to 100 ps. On the average, this amount of charge will reside in the base region.

Since $i_C$ is dependent on $v_{BE}$, $Q_n$ will similarly depend on $v_{BE}$. And $C = Q/V$, a **small-signal diffusion capacitance**, or **incremental capacitance** $C_{de}$ can be derived to be

$$C_{de} = \frac{dQ_n}{dv_{BE}} = \tau_F \frac{di_C}{dv_{BE}} \tag{3.2}$$

Here, the small-signal transconductance $g_m = di_C/(dv_{BE})$ resulting in

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{V_T} \tag{3.3}$$

We have used the formula that $g_m = I_C/V_T$, which has been derived in previous lectures.

## 3.3 The Base-Emitter Junction Capacitance $C_{je}$

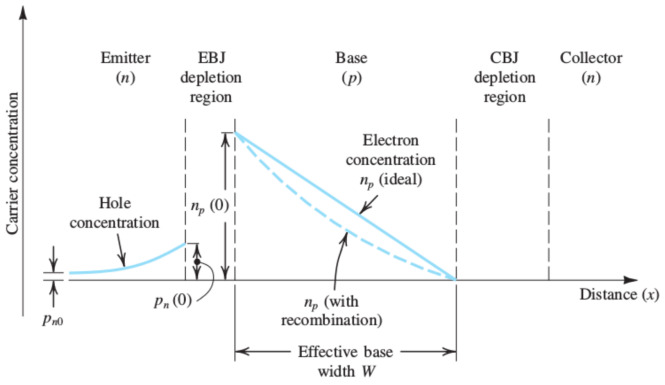



Figure 7: Revisit of the BJT model current flow with depletion layers denoted (Courtesy of Sedra and Smith).

In addition to the base-charging diffusion capacitance, there are capacitances at the depletion layers at the junctions as shown in Figure 7. The emitter-base junction (EBJ) is forward biased when the transistor is in active mode. This junction can store charges, and the charges are separated by the depletion layer. The more the forward biased voltage is, the thinner is the depletion layer at this EBJ, hence giving rise to a larger capacitance at this junction.

For the EBJ, this capacitance is assumed to be

$$C_{je} \approx 2C_{je0} \tag{3.4}$$

where $C_{je0}$ is the value of $C_{je}$ at zero EBJ voltage or with no biasing. Hence, it is assumed that the junction capacitance is twice larger than its quiescent value with no biasing. This is only an empirical rough estimate of the junction capacitance.

## 3.4 The Collector-Base Junction Capacitance $C_\mu$

Since in the active mode, the collector-base junction (CBJ) is reverse biased, there is a **depletion capacitance** $C_\mu$. Since this depletion layer is much thicker than that in the EBJ, the capacitance associated with it is much smaller. It is empirically given by

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m} \tag{3.5}$$

where $C_{\mu 0}$ is the quiescent value when no biasing voltage appears across the CBJ. Here, $V_{CB}$ is the magnitude of the CBJ reverse-bias voltage, and $V_{0c}$ is

the CBJ built-in voltage around 0.75 V, and $m$ is typically around $0.2 - 0.5$. It is noted that this capacitance decreases under reverse biasing due to that the depletion layer becoming thicker.

## 3.5 The BJT Unity-Gain Frequency

Figure 8 can be used to find the short-circuit current gain of a BJT at high frequency. The collector current, ignoring the effect of $r_o$, is

$$I_c = (g_m - sC_\mu)V_\pi \tag{3.6}$$

Furthermore, one can show that

$$V_\pi = I_b \left(r_\pi \parallel C_\pi \parallel C_\mu\right) = \frac{I_b}{1/r_\pi + sC_\pi + sC_\mu} \tag{3.7}$$

Thus, a frequency dependent current amplification factor $\beta$, called $h_{fe}$,[3] is given as

$$h_{fe} = \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{1/r_\pi + s(C_\pi + C_\mu)} \tag{3.8}$$

Since $C_\mu$ is small, one can assume that $\omega C_\mu \ll g_m$, then the above can be approximated as

$$h_{fe} \approx \frac{g_m r_\pi}{1 + s(C_\pi + C_\mu)r_\pi} \tag{3.9}$$

Thus,

$$h_{fe} = \frac{\beta_0}{1 + s(C_\pi + C_\mu)r_\pi} \tag{3.10}$$

where $\beta_0 = g_m r_\pi$ is the low-frequency value of $\beta$. Writing

$$h_{fe} = \frac{\beta_0}{1 + s/\omega_\beta} = \frac{\beta_0}{1 + j\omega/\omega_\beta} \tag{3.11}$$

where

$$\omega_\beta = \frac{1}{(C_\pi + C_\mu)r_\pi} \tag{3.12}$$

then the 3-dB point is at $\omega = \omega_\beta$.

Next, one needs to ascertain when the current gain of this amplifier becomes unity. It can be seen that when

$$\omega = \omega_T \approx \beta_0 \omega_\beta \tag{3.13}$$

the current gain then becomes

$$h_{fe} = \frac{\beta_0}{1 + j\beta_0} \tag{3.14}$$

[3] $f$ stands for frequency-dependent forward gain, while $e$ means common emitter configuration.

the gain is approximately unity when $\beta_0$ is large. Thus

$$\omega_T \approx \frac{g_m}{C_\pi + C_\mu} \tag{3.15}$$

and

$$f_T \approx \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{3.16}$$

Again, as in the MOSFET case, the smaller the internal capacitances, the large $f_T$ is.

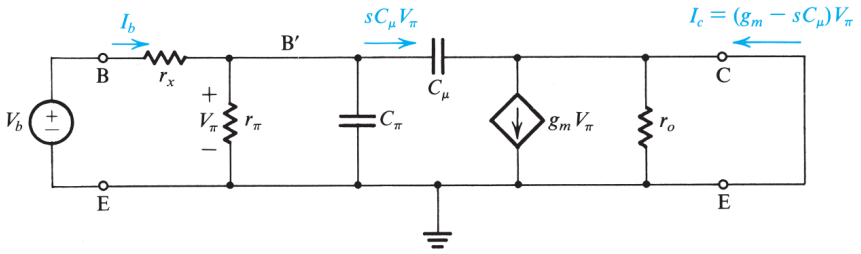



Figure 8: Circuit model for deriving $h_{fe}$ (Courtesy of Sedra and Smith).

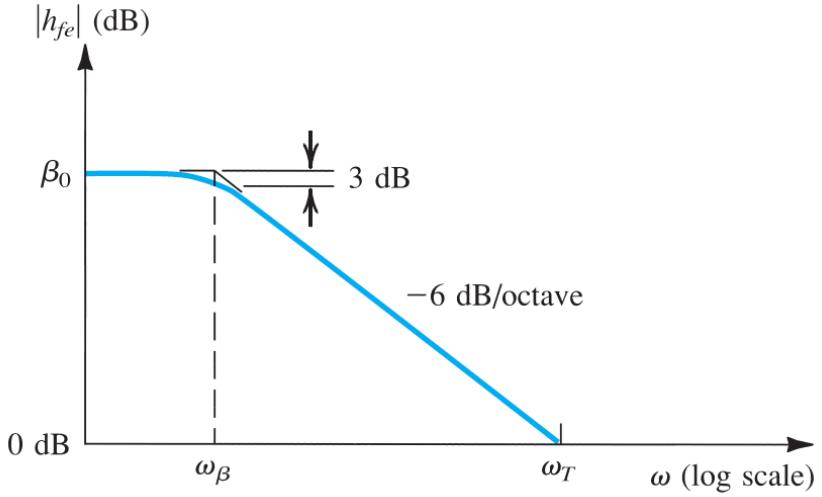
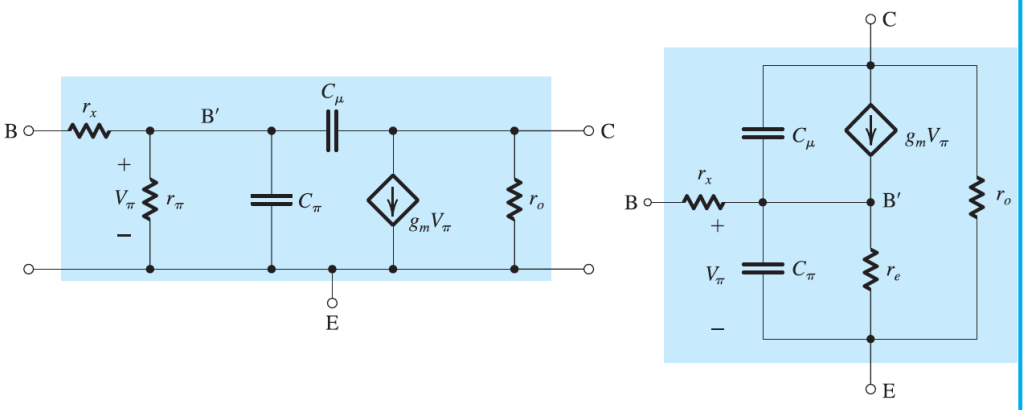



Figure 9: Bode plot for $|h_{fe}|$. In the above, 6 dB/octave is the same as 20 dB/decade, since an octave is equivalent to the doubling of frequency (Courtesy of Sedra and Smith).

**Table 10.2** The BJT High-Frequency Model




$g_m = I_C/V_T$ $\quad r_o = |V_A|/I_C$ $\quad r_\pi = \beta_0/g_m$ $\quad r_e = r_\pi/(\beta+1)$

$C_\pi + C_\mu = \dfrac{g_m}{2\pi f_T}$ $\quad C_\pi = C_{de} + C_{je}$ $\quad C_{de} = \tau_F g_m$ $\quad C_{je} \simeq 2C_{je0}$

$C_\mu = C_{jc0} \Big/ \left(1 + \dfrac{|V_{CB}|}{V_{0c}}\right)^m$ $\quad m = 0.3\text{–}0.5$

# 4 High-Frequency Response of the CS and CE Amplifier with Miller Effect

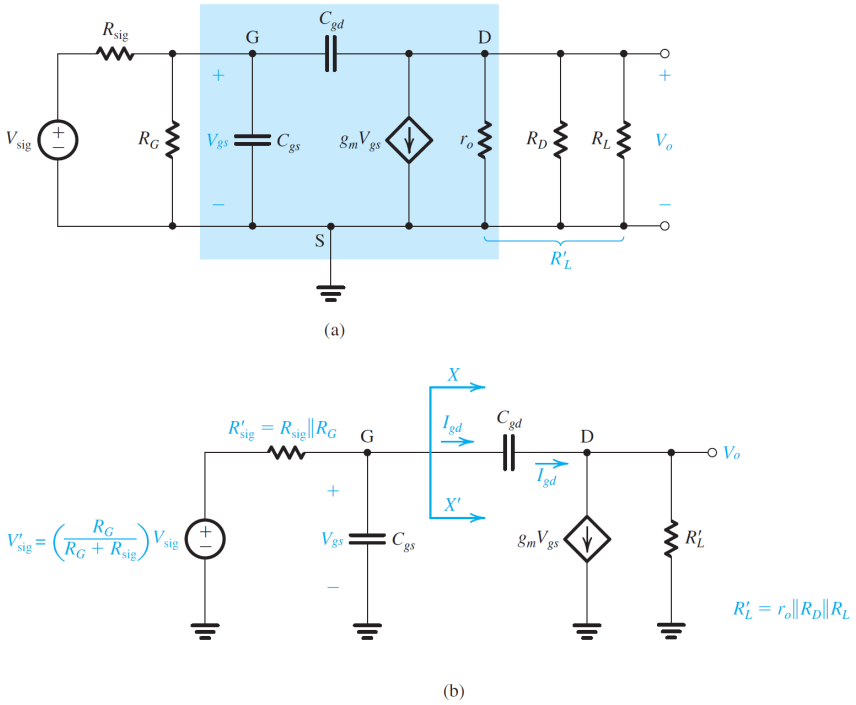



Figure 10: Models for the high-frequency response of a CS amplifier. (a) Equivalent circuit. (b) A simplified circuit by consolidation (Courtesy of Sedra and Smith).

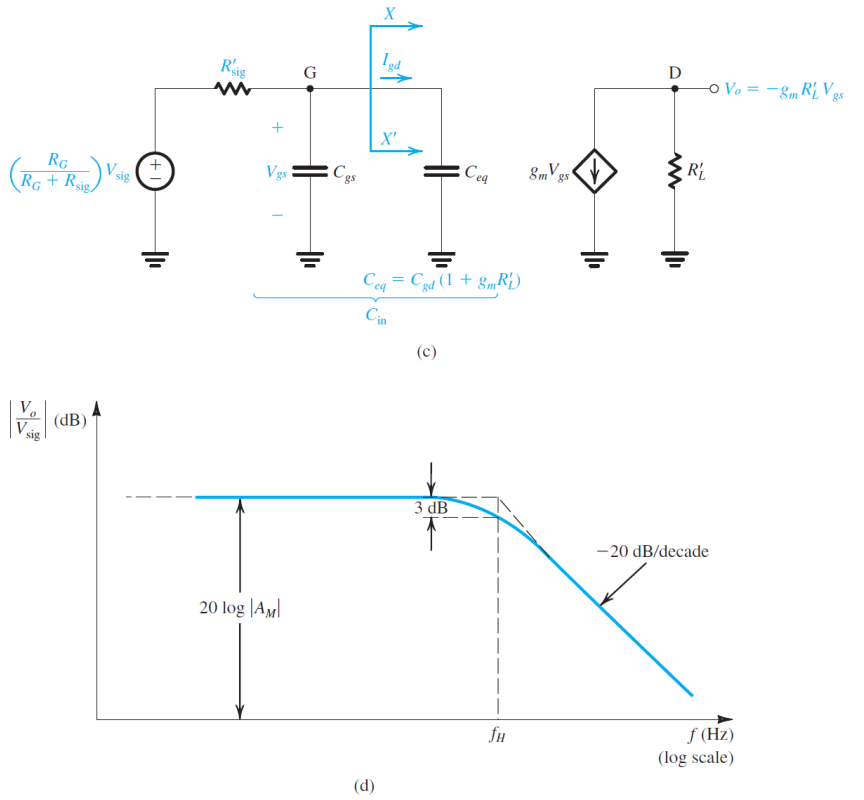



Figure 11: Continuation of the previous Figure 10. (c) Further simplification by using $C_{eq}$. (d) A single-time-constant frequency response Bode plot (Courtesy of Sedra and Smith).

Figure 10 shows the small-signal equivalence of a CS amplifier. The overall voltage gain is given by

$$A_M = \frac{V_o}{V_{\text{sig}}} = -\frac{R_G}{R_G + R_{\text{sig}}}(g_m R'_L) \tag{4.1}$$

In order to simplify the circuit, it can be consolidated using Thévenin theorem so that the source is modeled by only two elements as shown in Figure 10(b). Also, $R'_L$ consolidates the three resistances at the output end.

One further simplification is to replace the capacitor $C_\mu$ with an equivalence capacitor $C_{eq}$ as shown in Figure 10(c). To this end, we shall calculate the load current, in accordance with Figure 10(b), which is given by $(g_m V_{gs} - I_{gd})$. Then the output voltage is given by

$$V_o = (g_m V_{gs} - I_{gd}) R'_L \approx -g_m R'_L V_{gs} \tag{4.2}$$

Again, one assumes that $g_m V_{gs} \gg I_{gd}$. In the above, $R'_L = r_o \parallel R_D \parallel R_L$. The current $I_{gd}$ can now be found as

$$I_{gd} = sC_{gd}(V_{gs} - V_o) \approx sC_{gd}\left[V_{gs} - (-g_m R'_L V_{gs})\right] = sC_{gd}(1 + g_m R'_L)V_{gs} \quad (4.3)$$

Now, one can assume that this extra current $I_{gd}$ is due to an equivalent capacitor $C_{eq}$ connected in parallel to $C_{gs}$ as shown in Figure 11. The current that flows into this equivalent capacitance $C_{eq}$ is

$$sC_{eq}V_{gs} = sC_{gd}(1 + g_m R'_L)V_{gs} \quad (4.4)$$

The above results in that

$$C_{eq} = C_{gd}(1 + g_m R'_L) \quad (4.5)$$

This equivalent capacitance $C_{eq}$ is much larger than $C_{gd}$, and this effect is known as the **Miller effect**, and the factor $(1 + g_m R'_L)$ is the **Miller multiplier**. Hence, the larger the gain of the amplifier is, the larger is this effect.

One can see that $C_{eq}$ is much larger than $C_{gd}$ because when a positive $V_{gs}$ is applied a the gate, the negative voltage $V_o$ is generated at the output node according to (4.2). This negative $V_o$ siphons more current from the gate to the drain as result, increasing $I_{gd}$ in accordance with (4.3).

One has to be reminded that the above derivation is predicated on the assumption that $g_m V_{gs} \gg I_{gd}$. However, it is seen that the Miller effect amplifies $I_{gd}$ as shown in (4.3). Hence, the $g_m V_{gs} \gg I_{gd}$ has to be checked when one uses the above simplified formula for the equivalence capacitance $C_{eq}$.