ECE 255, Differential Amplifiers, Revisited

10 April 2018

In this lecture, we revisit differential amplifiers. Differential amplifiers are preferred in op amp designs because of their high immunity to noise, and the absence of coupling and bypass capacitors. Even though more transistors are needed, they are easily done in IC designs. This lecture is a summary of Sections 9.4, 9.5, and 9.6 of Sedra and Smith.

1 DC Offsets

In the previous lectures, we have studied the common-mode rejection ratio (CMRR) of differential amplifiers. For a matched differential amplifier, there is no DC output, but in reality, the transistor pairs are not matched perfectly giving rise to a DC output which we call the DC offset.

These offset values can be easily derived using perturbation or Taylor series expansion in the circuit analysis. Any mismatch of the transistor pair gives rise to V_O, the **output DC offset voltage** as shown in Figure 1(a). Then one can define an equivalent **input offset voltage**, for the matched case, V_{OS}, that gives rise to the output offset voltage. To this end, one defines

$$V_{OS} = V_O/A_d \tag{1.1}$$

where A_d is the differential gain of the amplifier. A negative V_{OS} applied to the input as shown in Figure 1(b) for the unmatched case gives rise to zero output.

1.1 Resistor Mismatch

A mismatch can come from the drain resistor R_D as shown in Figure 1. First,

$$R_{D1} = R_D + \frac{\Delta R_D}{2}, \qquad R_{D2} = R_D - \frac{\Delta R_D}{2} \tag{1.2}$$

Then

$$V_{D1} = V_{DD} - \frac{I}{2}\left(R_D + \frac{\Delta R_D}{2}\right), \qquad V_{D2} = V_{DD} - \frac{I}{2}\left(R_D - \frac{\Delta R_D}{2}\right) \tag{1.3}$$

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And

$$V_O = V_{D1} - V_{D2} = \frac{I}{2}\Delta R_D \tag{1.4}$$

where $A_d = g_m R_D$ has been used. The offset voltage then is

$$V_{OS} = \frac{V_O}{A_d} = \frac{V_O}{g_m R_D} \tag{1.5}$$

But from previous lectures, the transconductance is

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2(I/2)}{V_{OV}} = \frac{I}{V_{OV}} \tag{1.6}$$

where V_{OV} is the overdrive voltage. Using this in the above, one gets

$$V_{OS} = \frac{V_{OV}}{2}\frac{\Delta R_D}{R_D} \tag{1.7}$$

1.2 Geometry Mismatch

When the mismatch comes from the geometry of the MOSFET in W/L, similar analysis follows. One let

$$\left(\frac{W}{L}\right)_1 = \frac{W}{L} + \frac{1}{2}\Delta\left(\frac{W}{L}\right), \qquad \left(\frac{W}{L}\right)_2 = \frac{W}{L} - \frac{1}{2}\Delta\left(\frac{W}{L}\right) \tag{1.8}$$

Then

$$I_1 = \frac{I}{2}\left[1 + \frac{\Delta(W/L)}{2(W/L)}\right], \qquad I_2 = \frac{I}{2}\left[1 - \frac{\Delta(W/L)}{2(W/L)}\right] \tag{1.9}$$

and

$$I_1 - I_2 = \frac{I}{2}\frac{\Delta(W/L)}{2(W/L)}, \qquad V_O = (I_1 - I_2)R_D \tag{1.10}$$

Using $V_{OS} = V_O/A_d = V_O/(g_m R_D)$, one gets the input offset voltage as

$$V_{OS} = \frac{V_{OV}}{2}\frac{\Delta(W/L)}{(W/L)} \tag{1.11}$$

1.3 Threshold Voltage V_t Mismatch

When the mismatch comes from the threshold voltage V_t, then letting

$$V_{t1} = V_t + \frac{\Delta V_t}{2}, \qquad V_{t2} = V_t - \frac{\Delta V_t}{2} \tag{1.12}$$

Then

$$I_1 = \frac{1}{2}k_n'\frac{W}{L}\left(V_{GS} - V_t - \frac{\Delta V_t}{2}\right)^2 = \frac{1}{2}k_n'\frac{W}{L}\left(V_{GS} - V_t\right)^2\left(1 - \frac{\Delta V_t}{2(V_{GS} - V_t)}\right)^2 \tag{1.13}$$

Using the fact that

$$\frac{1}{2}k_n'\frac{W}{L}\left(V_{GS}-V_t\right)^2=\frac{I}{2} \tag{1.14}$$

then using the fact that $(1+x)^n \approx 1+nx$ when x is small, one gets

$$I_1 \approx \frac{I}{2}\left(1-\frac{\Delta V_t}{V_{GS}-V_t}\right), \qquad I_2 \approx \frac{I}{2}\left(1+\frac{\Delta V_t}{V_{GS}-V_t}\right) \tag{1.15}$$

Subsequently, one has

$$\Delta I=\frac{I}{2}\frac{\Delta V_t}{V_{GS}-V_t}=\frac{I}{2}\frac{\Delta V_t}{V_{OV}} \tag{1.16}$$

and arrives at

$$V_{OS}=\Delta V_t \tag{1.17}$$

The three kinds of DC offsets are then

$$V_{OS,\text{resistor}}=\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}, \tag{1.18}$$

$$V_{OS,\text{geometry}}=\frac{V_{OV}}{2}\frac{\Delta(W/L)}{(W/L)}, \tag{1.19}$$

$$V_{OS,\text{threshold voltage}}=\Delta V_t \tag{1.20}$$

Assuming that the offset voltages are random and uncorrelated, the root mean square (RMS) offset voltage is

$$V_{OS}=\sqrt{\left(\frac{V_{OV}}{2}\frac{\Delta R_D}{R_D}\right)^2+\left(\frac{V_{OV}}{2}\frac{\Delta(W/L)}{(W/L)}\right)^2+\left(\Delta V_t\right)^2} \tag{1.21}$$

where one assumes that the average value of the cross terms are zero as there are no cross-correlation between them.[1] The right-hand sideis also called the root-mean square value.

[1]This follows from that if we have two random variables x_1 and x_2, and their sum $x_T = x_1 + x_2$, then $x_T^2 = x_1^2 + x_2^2 + 2x_1x_2$. Then the average of their sum squared is $\langle x_T^2\rangle = \langle x_1^2\rangle + \langle x_2^2\rangle + 2\langle x_1x_2\rangle$, but $\langle x_1x_2\rangle = 0$ if x_1 and x_2 are uncorrelated. Or average of their sum squared is the sum of the average of their squares. Taking the square root of their sum squared yields $\sqrt{\langle x_T^2\rangle} = \sqrt{\langle x_1^2\rangle + \langle x_2^2\rangle}$.

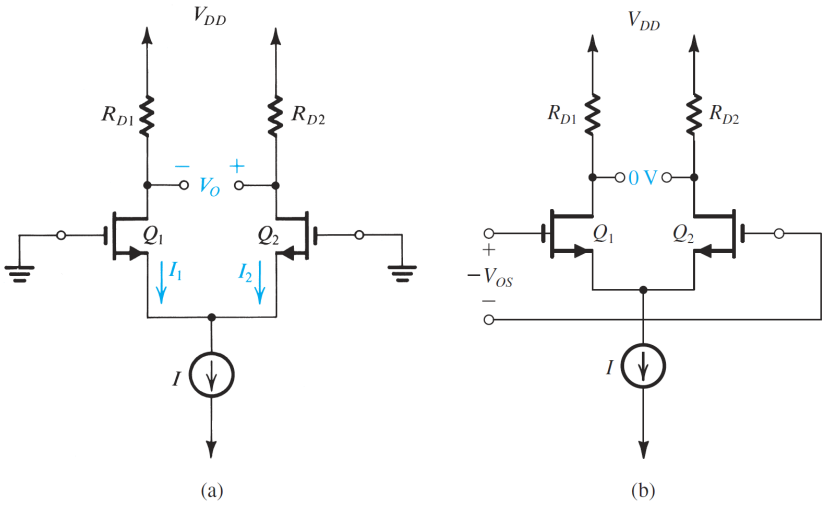

Figure 1: (a) MOS differential pair with inputs grounded to emulate a common mode operation, but yet a residual V_O results due to mismatch. (b) Application of a negative input offset voltage nulls the output offset (Courtesy of Sedra and Smith).

For BJT amplifiers, the mismatch can come from the collector resistor R_C giving rise to

$$|V_{OS}| = V_T \frac{\Delta R_C}{R_C} \tag{1.22}$$

where V_T is the thermal voltage.

When the mismatch comes from the saturation or scale current I_S, then

$$|V_{OS}| = V_T \frac{\Delta I_S}{I_S} \tag{1.23}$$

When the offset parameters are uncorrelated random variables, then

$$V_{OS} = V_T \sqrt{\left(\frac{\Delta R_C}{R_C}\right)^2 + \left(\frac{\Delta I_S}{I_S}\right)^2} \tag{1.24}$$

When the β values of the transistors are mismatched, the offset current is

$$I_{OS} = I_B \frac{\Delta \beta}{\beta} \tag{1.25}$$

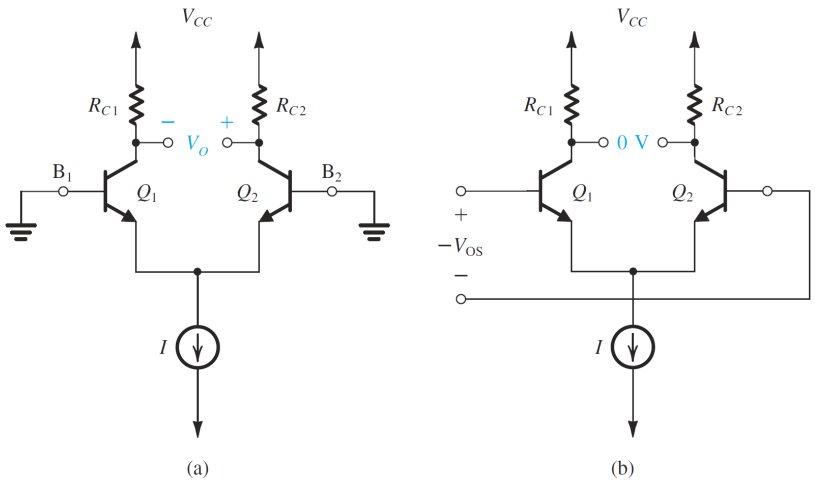

Figure 2: Analogous to the previous figure, but drawn here for BJT amplifiers (Courtesy of Sedra and Smith).

2 Current-Mirror Load for Differential Amplifiers

Differential amplifiers with differential outputs have three distinct advantages:

1. It reduces the common-mode gain and increases the common-mode rejection ratio (CMRR).

2. It reduces the input offset voltage since inherent cancelation exists in the design.

3. It increases the differential gain by a factor of 2 when the output is taken across two transistors.

Because of the cancelation effect of differential amplifiers at the input ports, it rejects most noise due to coupling to remnant electromagnetic signals. These signals can be due to the 60 Hz power line, or AM or FM radio signals in the room. These signals have relatively long wavelength compared to the electronic gadgets. For example, for FM 101.3, the frequency is close to 100 MHz. Using the formula that wavelength is proportional to c/f where $c = 3. \times 10^8$ m/s is the speed of light, a 100 MHz signal has wavelength of about 3 meters. This is still much larger than the size of our cell phone for instance. Hence, a differential input will pick up very little of this signal.

But for practical purposes, one needs to convert a differential output to a single-ended output as shown in Figure 3.

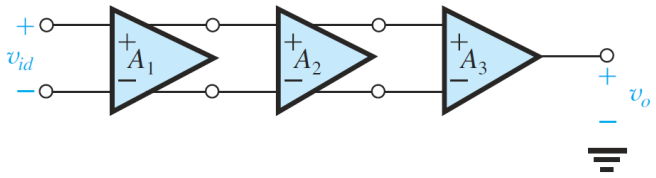

Figure 3: Multi-stage differential amplifier ending in a single-ended stage output for practical applications (Courtesy of Sedra and Smith).

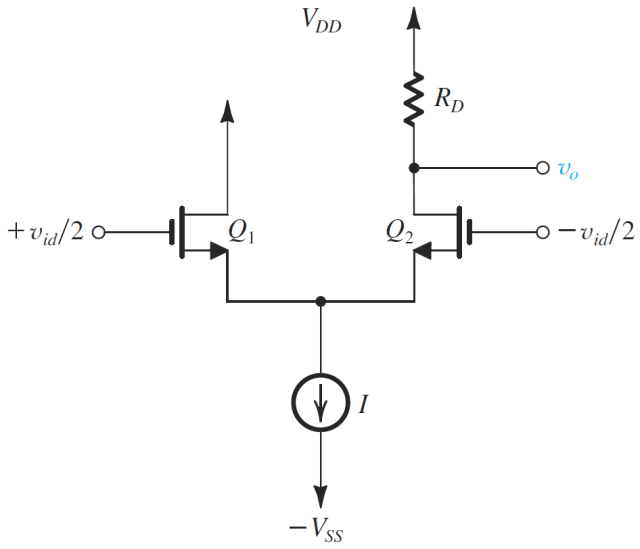

Figure 4: An inefficient way of converting to a single-ended output in a differential amplifier (Courtesy of Sedra and Smith).

An inefficient way of doing this is shown in Figure 4. We will discuss how to achieve this conversion more efficiently next. This is achieved by loading the differential amplifier with a current-mirror load.

2.1 Differential-to-Single-Ended Conversion

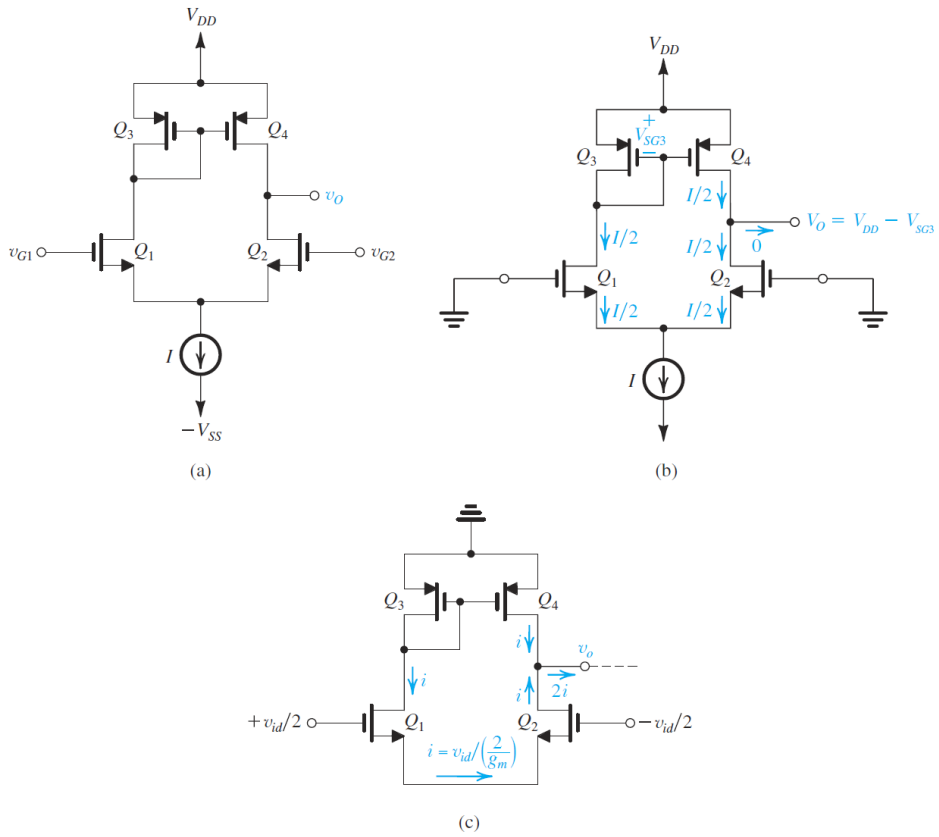

Figure 5: (a) The current-mirror loaded MOS differential pair to enhance its output efficiency. (b) The perfect matching case with common-mode input. (c) The small-signal differential mode input case (Courtesy of Sedra and Smith).

To achieve an efficient conversion from a differential output to a single-ended output, a current mirror is used as a load is shown in Figure 5(a).

To see how this works, consider a common mode input as shown in Figure 5(b). Assuming Q_3 ia matched to Q_4, then the drain currents of the two transistors are equal since in the ideal case, the drain current of a MOSFET depends only on its gate voltge. If Q_1 and Q_2 are matched as well, then by symmetry, no current flows out of the output port, and the drain voltages of the transistor pairs should be equal to each other. Hence, $V_O = V_{DD} - V_{SG3}$, as expected and no current flows out of the output port. This is an idealization as we assume that Q_3 and Q_4 act like ideal current sources where their drain currents depend

only on their gate voltages.

Now assume that a small-signal differential voltage is being applied, and the small-signal model of Figure 5(c) can be used. The bottom two transistors are imbalanced, while the top two transistors are still balanced. This asymmetry causes the current to double up at the output port as shown. Therefore the use of a current mirror helps to double this current or the gain of this design compared to that in Figure 4.

In actuality, when the drain of Q_4 is connected to a load, its voltage will change from the value of $V_O = V_{DD} - V_{SG3}$ due to the Early effect, and that additional current will flow through the output resistance of Q_4. Thus mismatch occurs and the output voltage is not as ideal as shown.

2.2 Differential Gain of the Current-Mirror-Loaded MOS Pair

The differential gain of this amplifier can be represented by Figure 6. A detail analysis is given in the textbook, but we can cut through the chaste and give an intuitive argument to arrive at the answer.

First, one assumes that the transistors Q_1 and Q_2 are matched so that $g_{m1} = g_{m2} = g_m$. Then the transconductance of the model shown in Figure 6 is given by

$$G_m = g_m \tag{2.1}$$

The output resistance is given by

$$R_o = r_{o2} \parallel r_{o4} \tag{2.2}$$

Thus the differential voltage gain is

$$A_d = \frac{v_o}{v_{id}} = G_m R_o = G_m(r_{o2} \parallel r_{o4}) = g_m(r_{o2} \parallel r_{o4}) \tag{2.3}$$

If one further assumes that $r_{o2} = r_{o4} = r_o$, then $(r_{o2} \parallel r_{o4}) = r_o/2$, and

$$A_d = \frac{1}{2} g_m r_o = \frac{1}{2} A_o \tag{2.4}$$

where A_o is the gain of one MOS transistor.

Had the current mirror not being there as a load, the gain of the differential amplifier as shown in Figure 4 is just $\frac{1}{2} g_m R_L$. Now that a current mirror is added that causes current doubling, then the differential gain is $g_m R_L$. In this case, the load resistance $R_L = (r_{o2} \parallel r_{o4}) = r_o/2$ is just the output resistance of Q_4 in parallel connection with Q_2, since the output current will flow through these two resistors if it is open circuited.

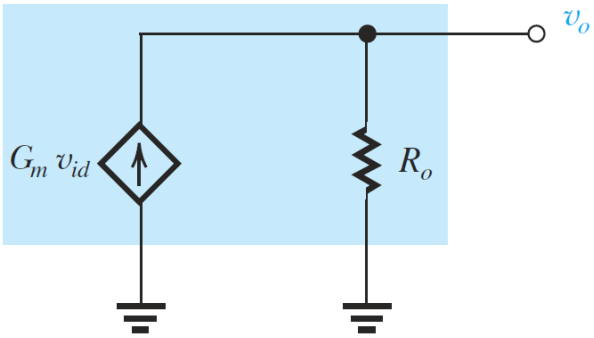

Figure 6: Output equivalent circuit of the amplifier in the previous figure (Courtesy of Sedra and Smith).

2.3 A Two-Stage CMOS Op Amp

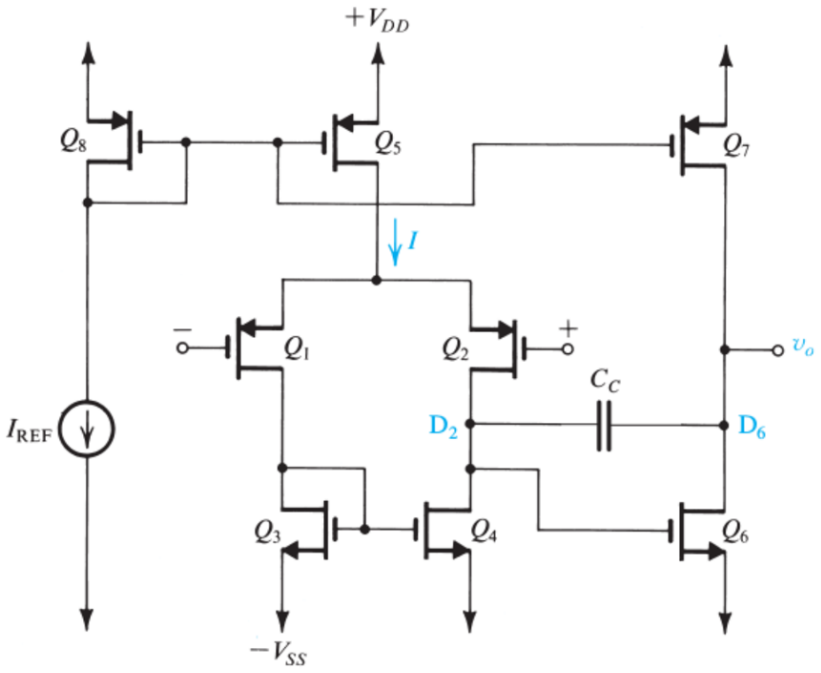

Figure 7: A two-stage CMOS op-amp design (Courtesy of Sedra and Smith).

Given the background knowledge, we are ready to study a two-stage CMOS op amp as shown in Figure 7. Given the diminishing dimensions of these devices nowadays, the biasing voltage becomes increasing smaller, reaching a fraction of volt.

The first stage consists of a differential amplifier formed by Q_1 and Q_2. A current-steering circuit formed by Q_8 and Q_5 supplies the needed current to drive the first stage. Moreover, the current mirror, Q_3 and Q_4 are used as the load to the first stage amplifier. Notice that Q_1 and Q_4 are PMOS's while Q_3 and Q_4 are NMOS's.

The second stage of the amplifier is formed by Q_6 which is a common-source amplifier, loaded with a current source Q_7. A coupling capacitor C_C is included but its function is outside the scope of this course. However, one can see that at high frequency, the capacitor acts like a short, connecting v_o directly to the output of Q_2. This reduces the gain of the amplifier, and hence has a negative feedback.

The output resistance of this op amp is $(r_{o6} \parallel r_{o7})$ which is high. Therefore, this circuit is good for driving high-impedance load such as a small capacitor.

2.3.1 Voltage Gain

The voltage gain of the first stage of this amplifier is

$$A_1 = -g_{m1}(r_{o2} \parallel r_{04}) \tag{2.5}$$

Notice the negative sign because of a PMOS being used here. Since the second stage is current source loaded, the common-source amplifier voltage gain of this stage is

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7}) \tag{2.6}$$

The open-circuit or open-loop voltage gain is the product of A_1 and A_2.

2.3.2 Input Offset Voltage

There are two kinds of voltage offsets in an op amp design. One is due to the imprecision of the fabrication process giving rise to random dimensions. This is known as **random offset** or **random error**.

Random errors actually become an increasingly important effect as device dimensions become smaller. It becomes increasingly harder to fabricate devices to the prescribed dimensions because of technology barriers in the lithographic process. The uncertainty in the dimensions of the fabricated devices gives rise to a field known as **uncertainty quantification**.

Another is due to design errors giving rise to **systematic offset** or **systematic error**. For instance, in the design shown in Figure 7, when a common mode input is assumed, there should be no output voltage. But design errors may cause this not to be so. Again, in an ideal circuit, Q_3 is matched to Q_4, with the drain current of Q_4 being $I/2$. Also, ideally, Q_3 and Q_4 should have the same drain voltage due to their matching. So when the drain voltage of Q_4 is used to drive Q_6, Q_6 should have the same drain current as Q_4, except for geometry variation. This can be expressed as

$$I_6 = \frac{(W/L)_6}{(W/L)_4}\frac{I}{2} \tag{2.7}$$

But Q_7 is suppose to mirror the currents of Q_5 or Q_8. This can be expressed as

$$I_7 = \frac{(W/L)_7}{(W/L)_5} I \tag{2.8}$$

Not knowingly to the designer, if I_6 is not equal to I_7, a mismatch will result giving rise to nonzero output current in the common-mode operation. This nonzero output current will produce a voltage at the load. A systematic error will result. To avoid this, one chooses

$$\frac{(W/L)_6}{(W/L)_4} = 2\frac{(W/L)_7}{(W/L)_5} \tag{2.9}$$

so that $I_6 = I_7$.